XDF XILINX DEVELOPER FORUM

Embedded Software Strategy & Development

Presented By

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XILINX

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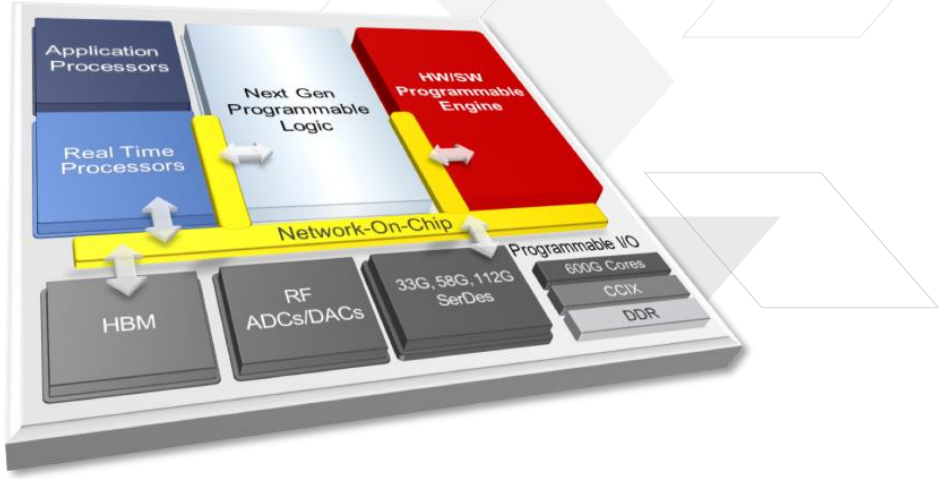
If Microsoft ever does applications for Linux it means I've won.

-Linus Torvalds, 1998

When software developers drive hardware design it means adaptable SoC's have won.

-Xilinx, 2018



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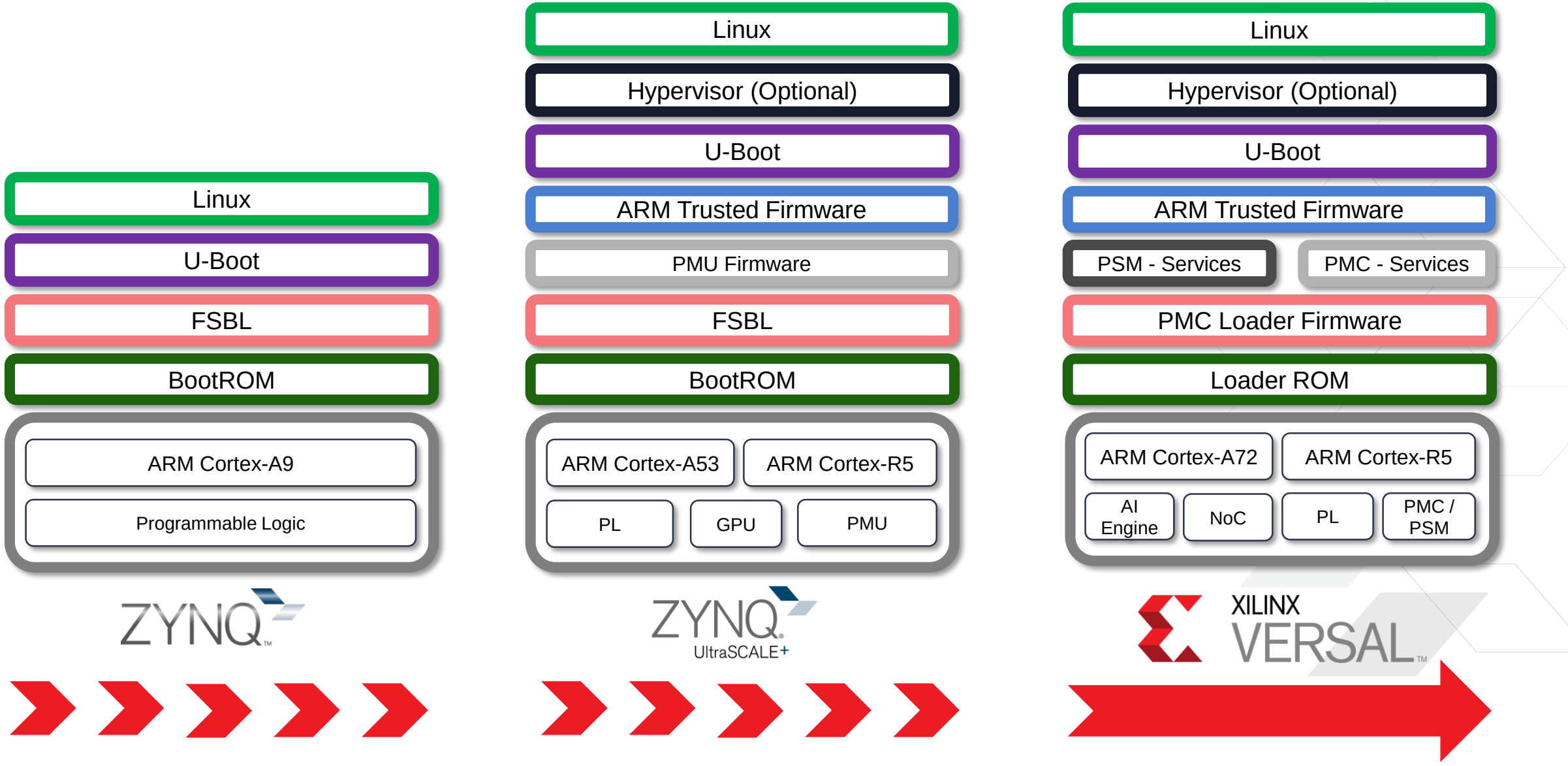

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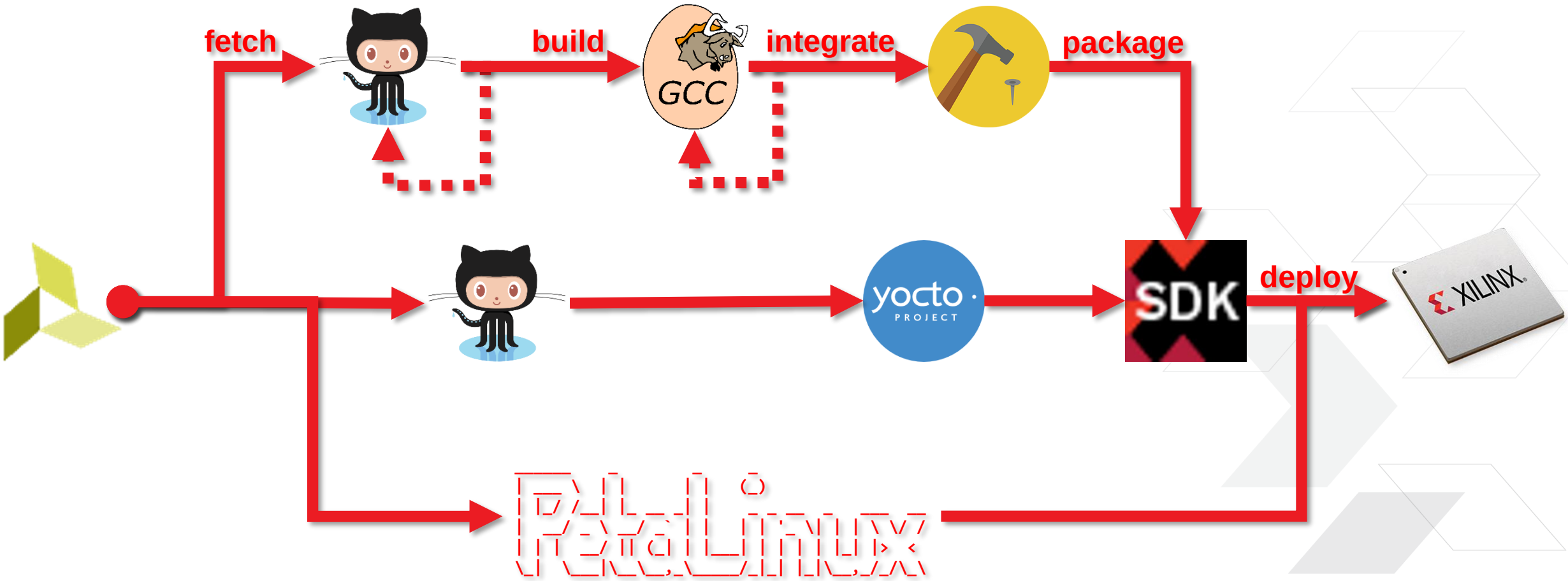
How Do You Want to Do This?



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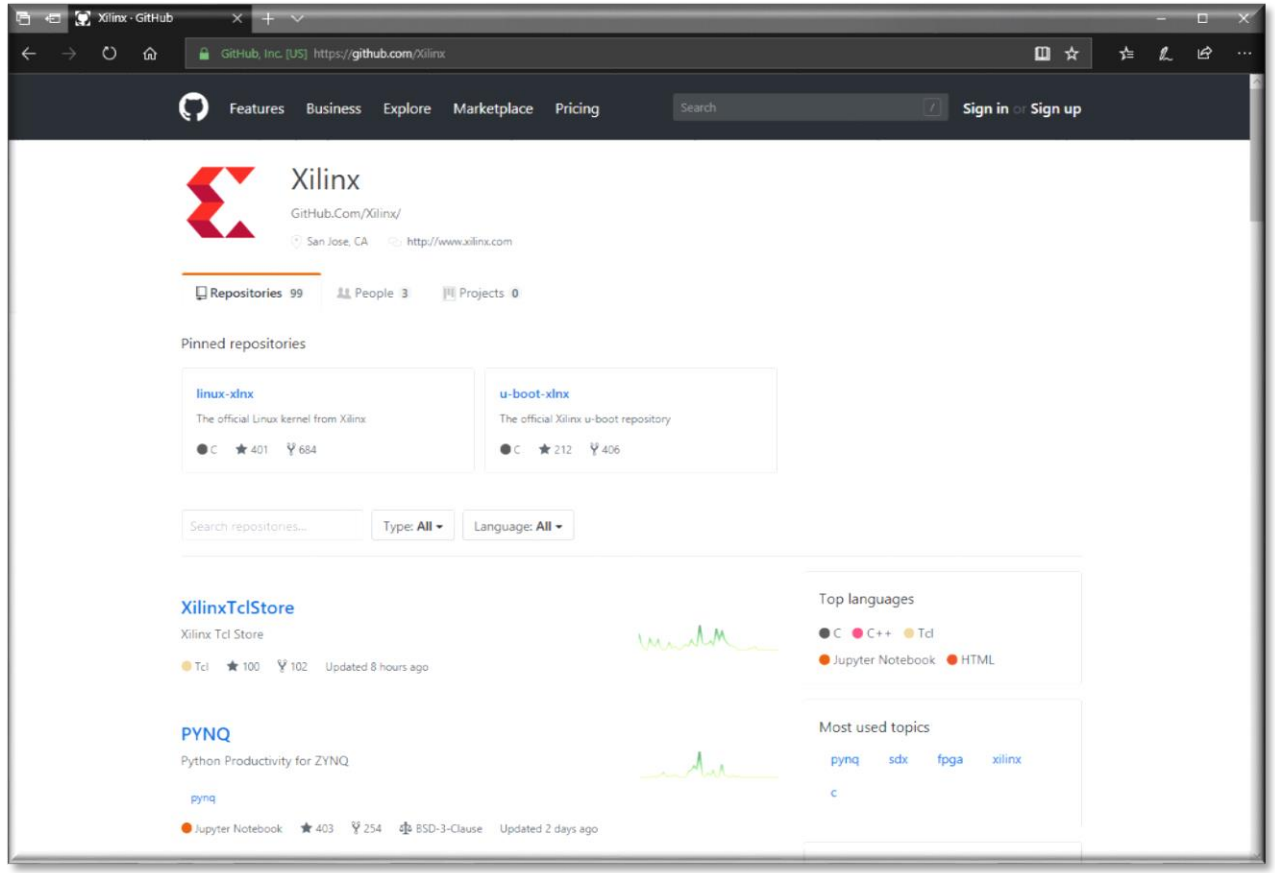
Open and Public Code



- GitHub.com/Xilinx
- Nearly 100 repositories
- All of our embedded software stack
- All of our Yocto recipes
- Scripts for Vivado
- Tutorials and Examples

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Staying Up-to-Date

ATF v1.6

v4.11

v2.6 (Thud)

v2019.01

v4.19

The same for every device family!

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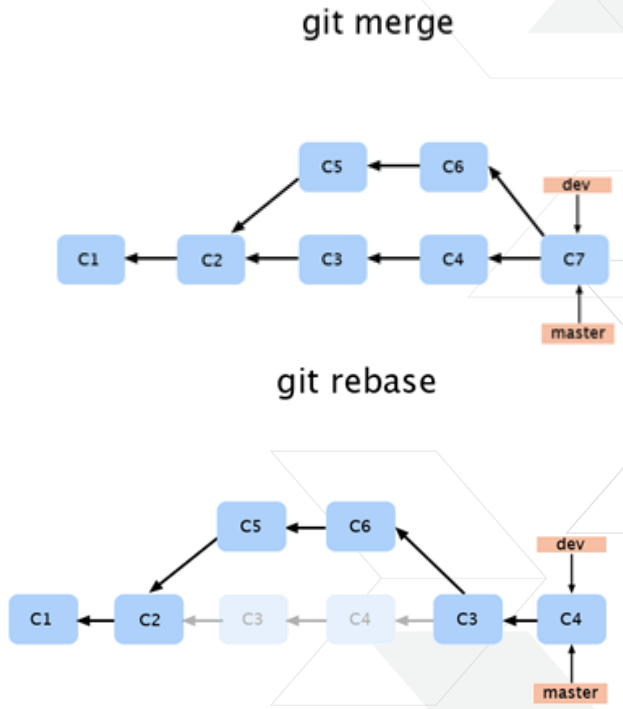
Rebase Kernel Tree

- **Merge-Tree**
  - Merges two separate branches into a single new branch going forward
  - Lose the history of what was different between the branches
- **Rebase Tree**
  - Creates a series of patches that can be applied cleanly to the HEAD node
  - Maintain history of development in the separate development paths



- **Single upstream kernel version per year**
- **Rebase patchsets with Vivado releases**
- **Rolling merge tree**

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Compilers and Toolchains

- AArch32 – ARMv7 – Zynq-7000
- AArch64 – ARMv8 – Zynq UltraScale+, Versal
- Cortex-R5 – ARMv7 – Zynq UltraScale+, Versal

Linaro GCC 7.3.1

- MicroBlaze – MMU / Linux Configuration
- MicroBlaze – Microcontroller Configuration

crosstool-NG GCC 7.3.1

GCC 8 Support in 2019

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Enabling Yocto

> **meta-xilinx** – BSP support for Xilinx device families

> **meta-xilinx-tools** – Yocto infrastructure to interface with Xilinx tools

> **meta-petalinux** – Infrastructure to replicate the default PetaLinux root filesystem

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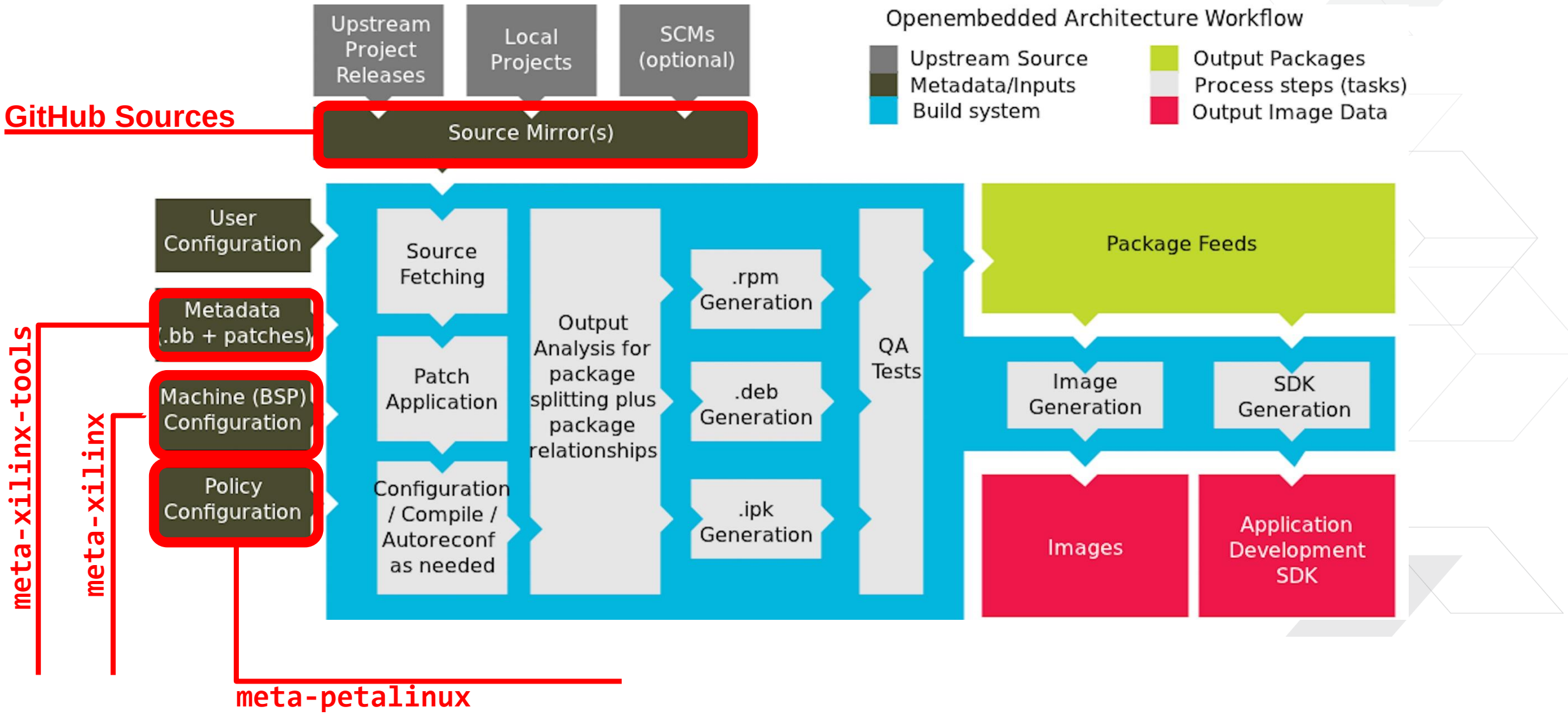
Integrating with Yocto



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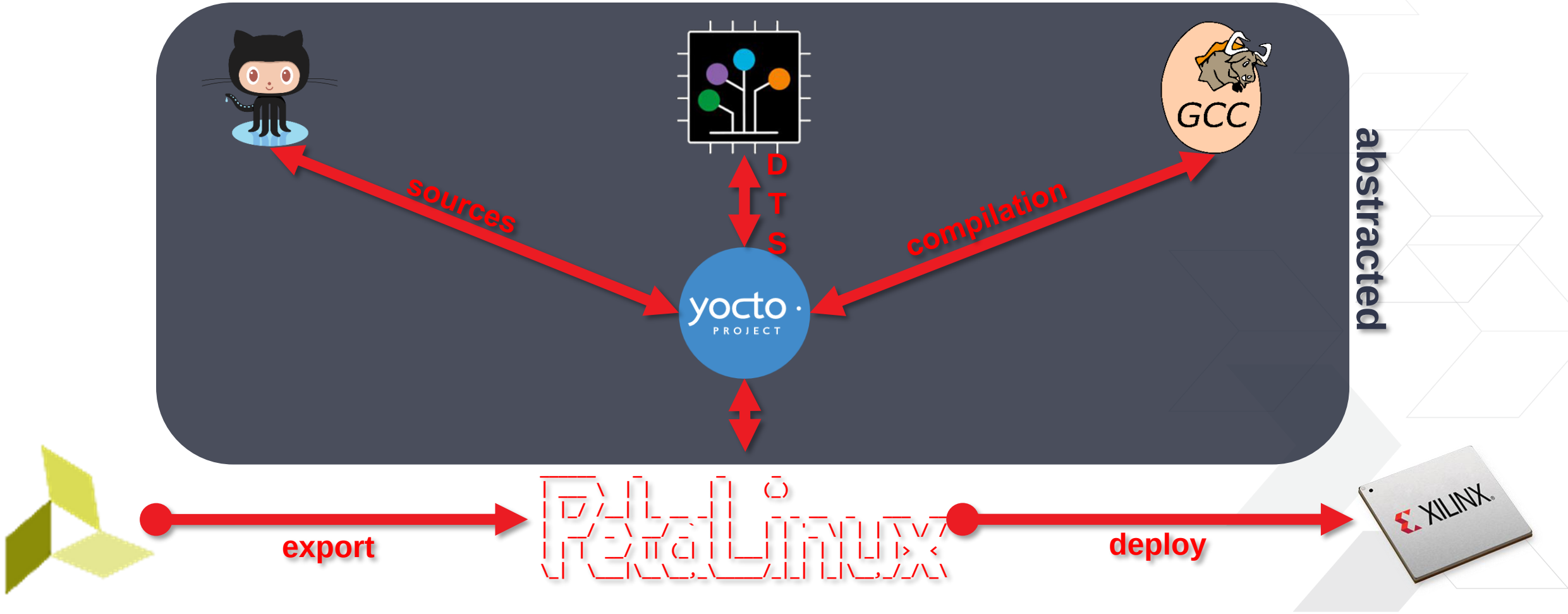
Abstracting Yocto



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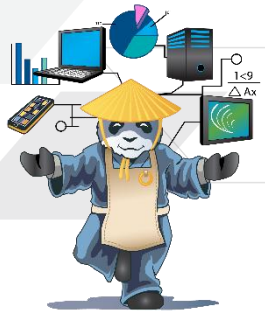
Multiprocessing with Xen

> Reducing code Size

> Working toward certifiability

> Dom0-less boot

> Automatic static partitioning



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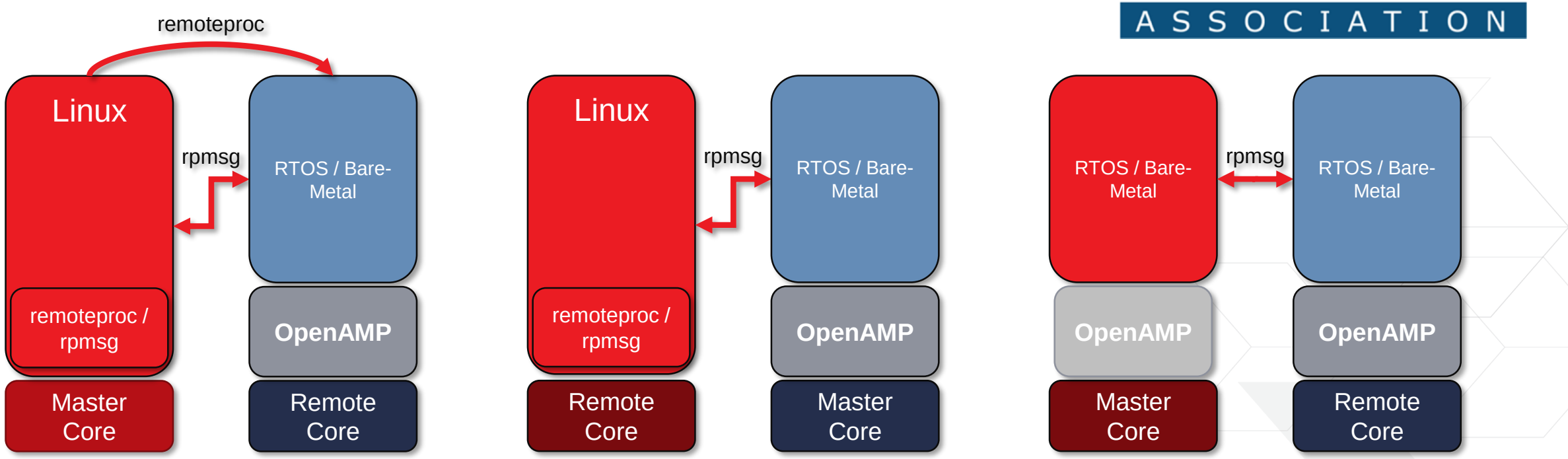
OpenAMP and Interprocessor Comms



- **Built on standard `remoteproc` and `rpmsg` infrastructure**

- **Open and public on GitHub.com/OpenAMP**

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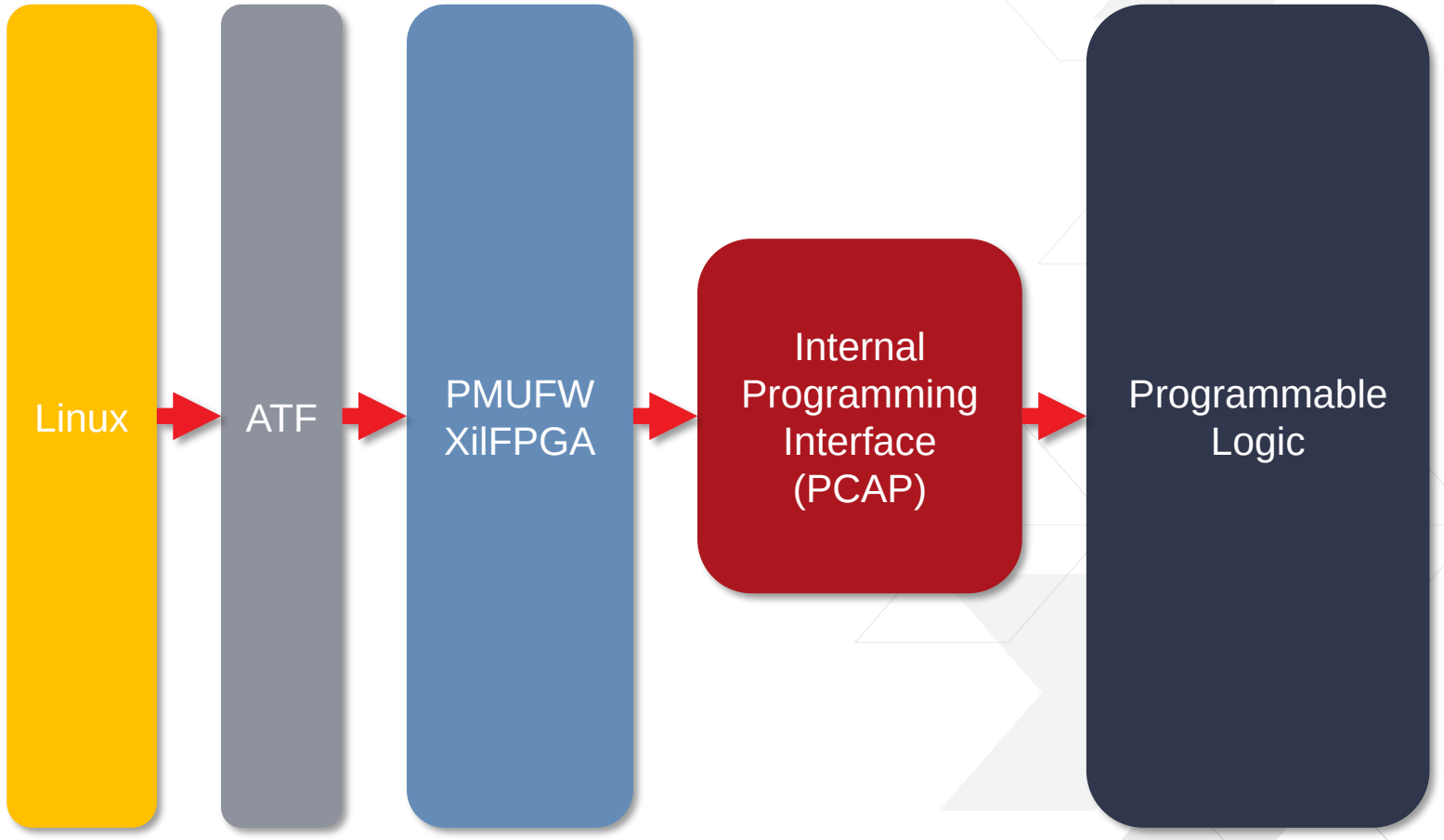
FPGA Manager

```
--- FPGA Configuration Framework
<*>   FPGA Region
< >   Lattice iCE40 SPI
< >   Altera Arria-V/Cyclone-V/Stratix-V CvP FPGA Manager
< >   Altera FPGA Passive Serial over SPI
< >   Xilinx Configuration over Slave Serial (SPI)
<*>   FPGA Bridge Framework
< >   Altera Partial Reconfiguration IP Core
< >   Xilinx LogiCORE PR Decoupler
```

```
$ /sys/class/fpga_manager/fpga0/
```



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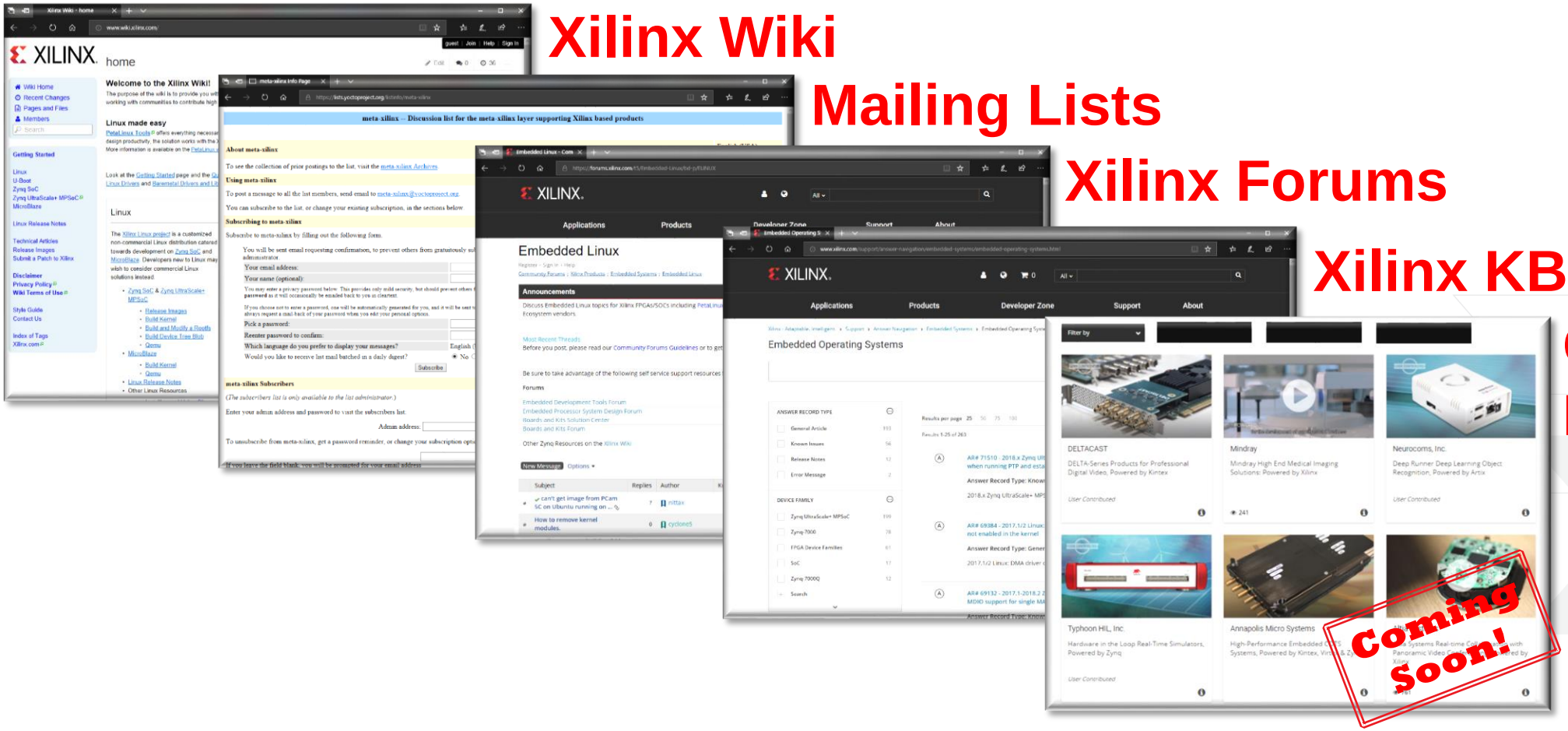
Open Support



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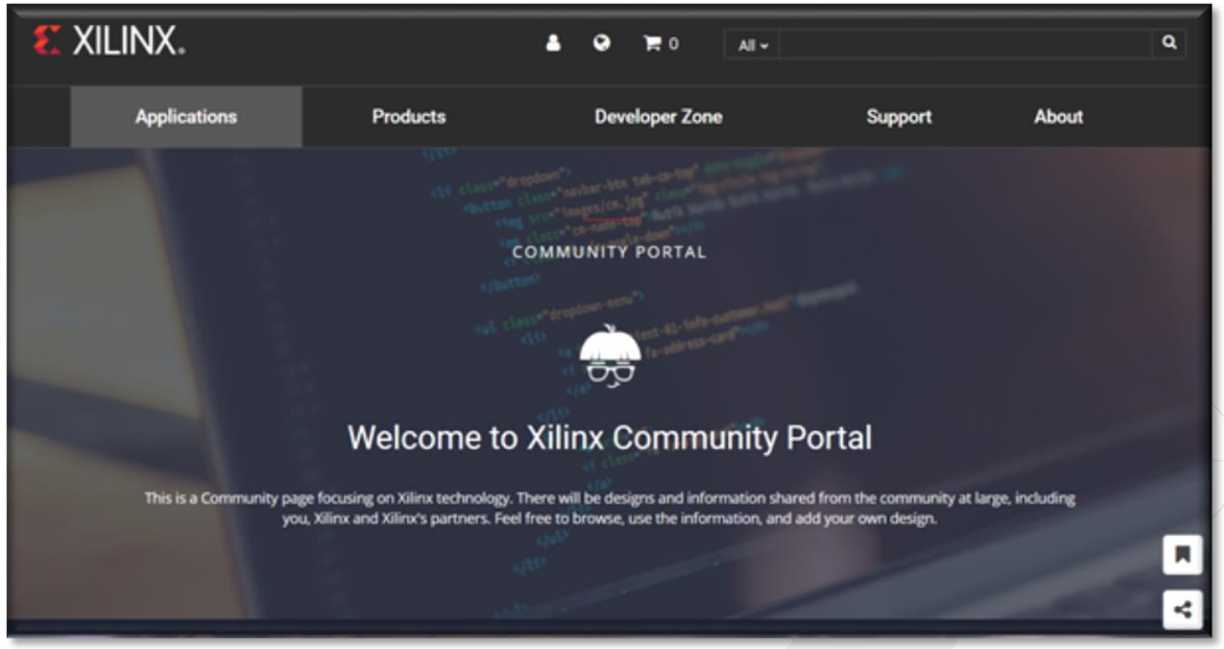
New Community Portal

- **Centralized Clearinghouse**
  - References other resources, doesn't replace them
- **Increasing number of developers use Open Source Content**
  - Converge content and make navigation to desired location easier
- **Xilinx has lots of Open Source content to filter**
  - GitHub, AWS, Wiki, Ultra96



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One more thing…

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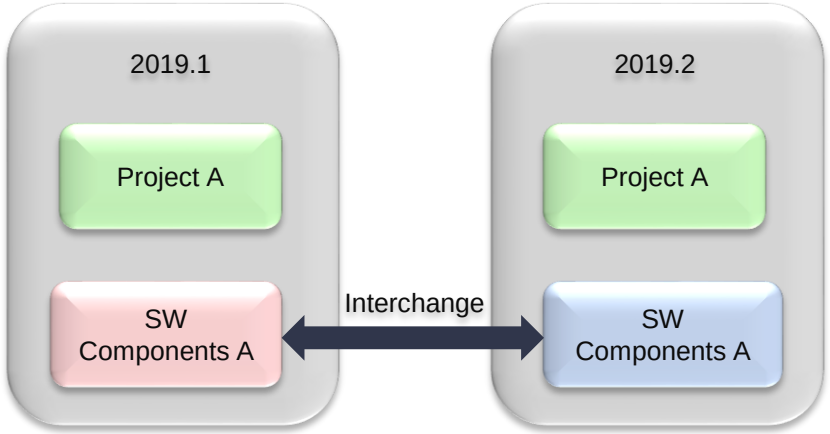
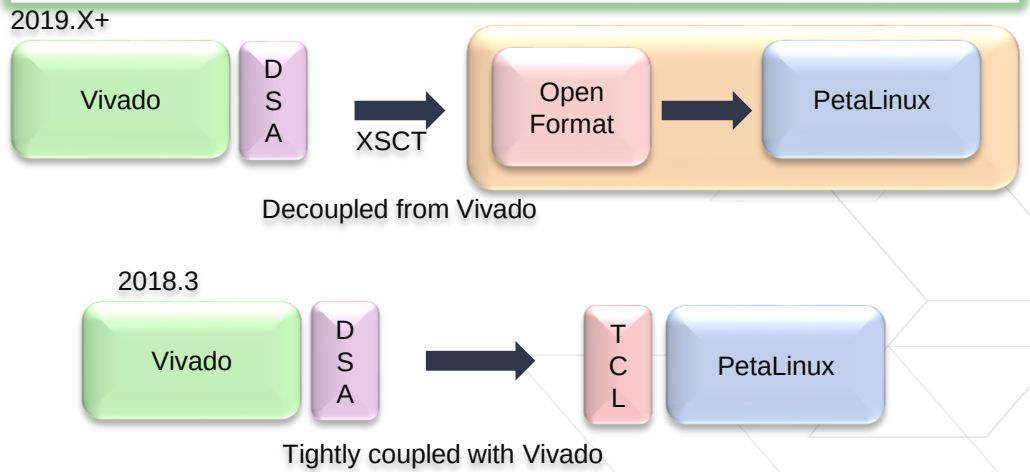
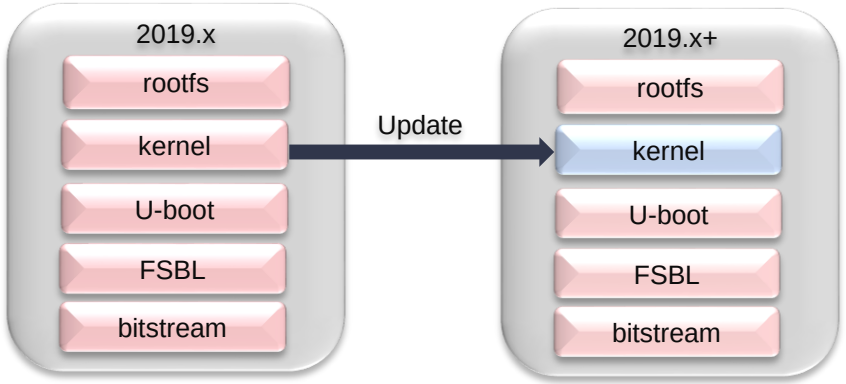
Decoupling PetaLinux Projects



Decoupling Linux from Vivado



Decoupling Runtime Components



Decoupling Packages from Each Other

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