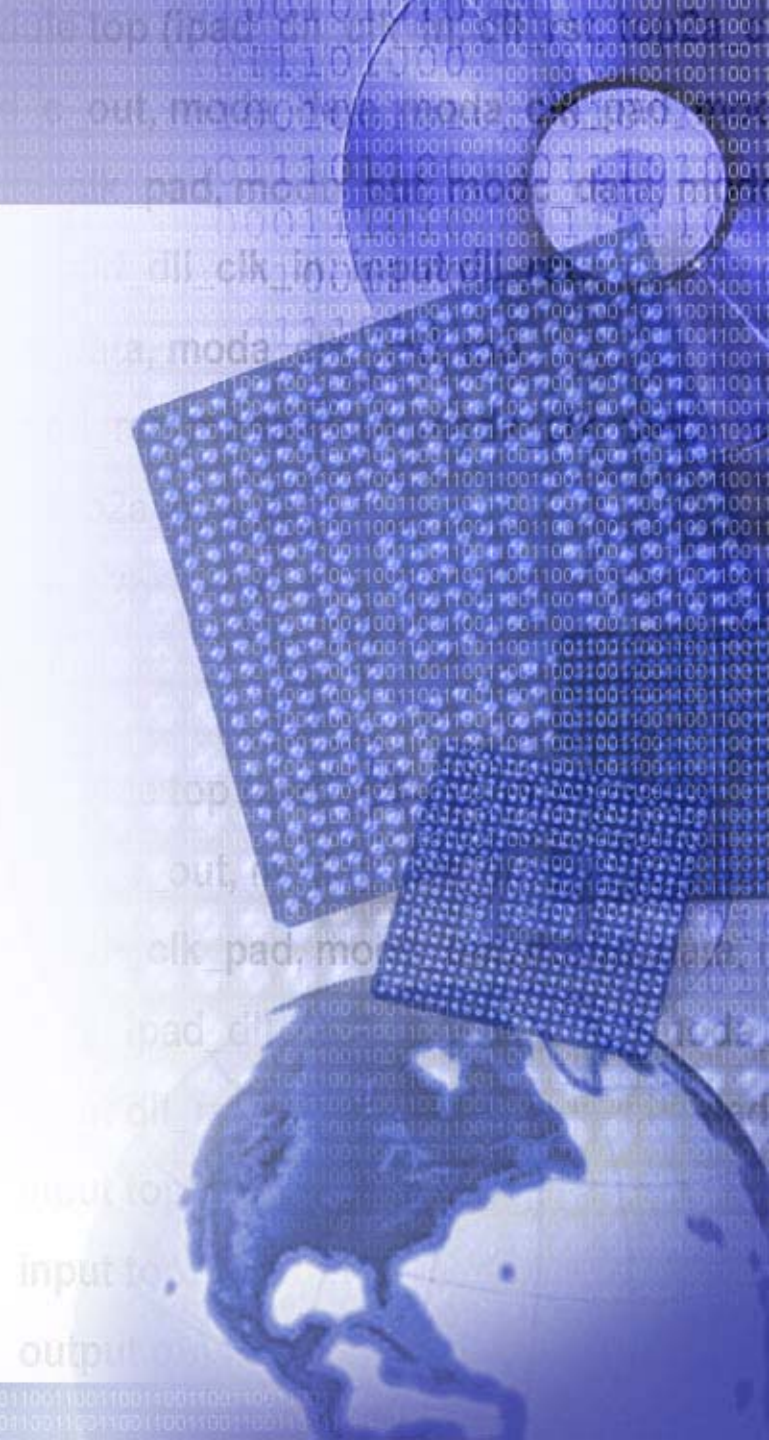




Digital TVs

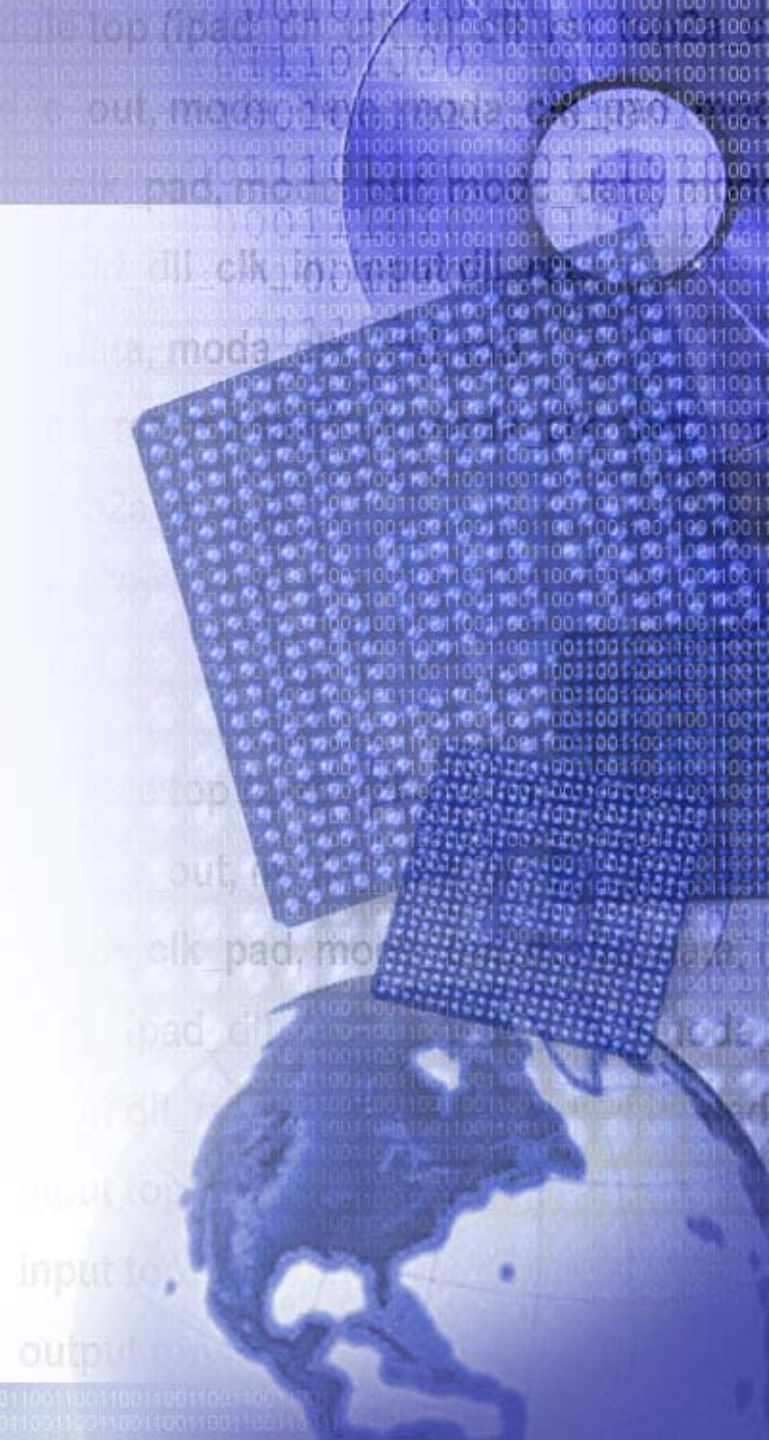


Agenda

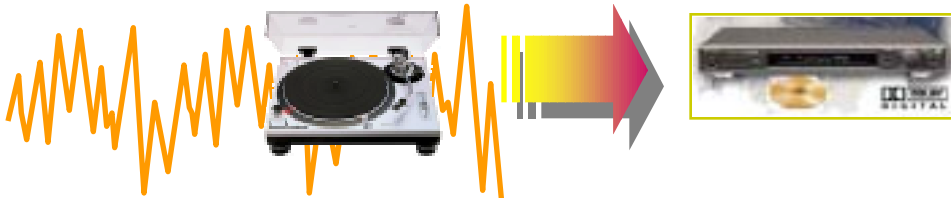
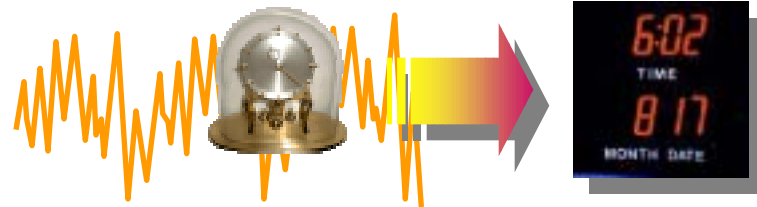
- Introduction and market overview
- System overview
- Xilinx value proposition for Digital TV
 - Forward Error Correction
 - MPEG
 - Memory Interface
 - IEEE-1394
 - USB 2.0
 - PCI
 - Data Encryption
 - Color Space Conversion
 - LVDS
 - Clock Generation/Distribution
- Summary



Introduction & Market Overview



The Digital Age of Consumer Electronics



1001010100010100100000000
10101101000101101001011
010111101001001010100101
110001011010101010100
010101010111101000
10000000111000010101
10001001010101000
101010111001010000
0101011000000101
0100010001010101
01000101010101
0101000001010
1010101000111

Digital technology brings
Higher accuracy
Higher reliability
Faster speed
Lower power
Lower cost

Digital Logic Spawns New Consumer Products



Digital TV

Revolutionizing the way we watch television



Consumer Satellite Modems

Revolutionizing high speed home Internet access



Smart Card

Revolutionizing the way we purchase products



Desktop Video Editing

Delivering video editing to the home

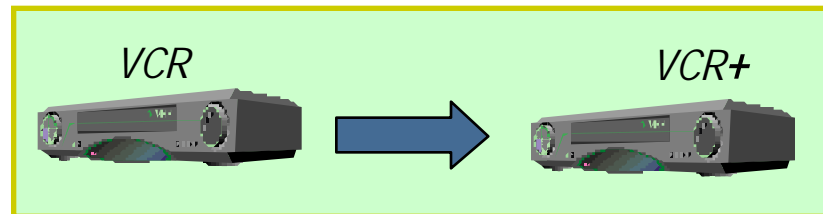
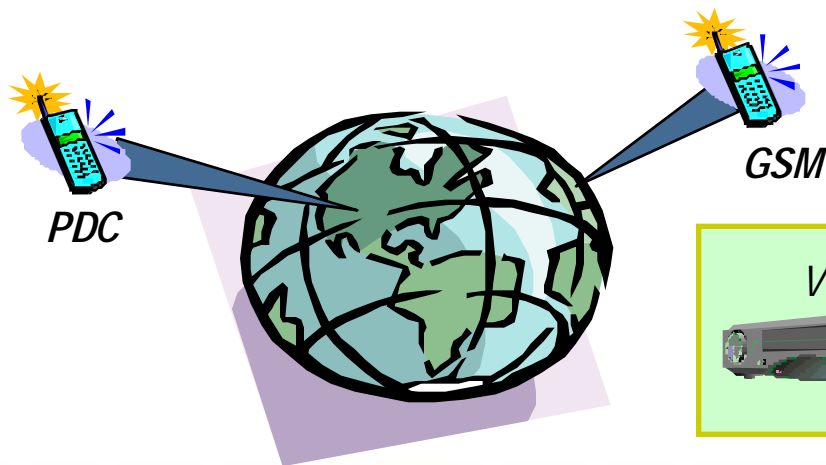
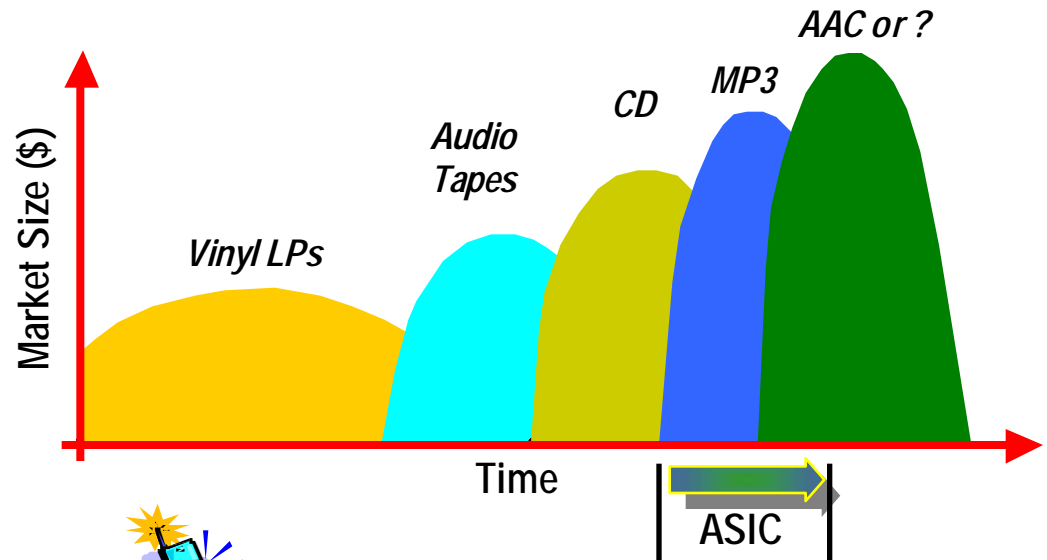


MP3 Players

The new revolution in portable digital music

ASICs & ASSPs Cannot Meet Consumer Market Requirements

- Short Product Life Cycles
- Changing Standards
- Multiple Standards
- Rapidly Evolving Features



Convergence Is Happening!

- Invisible computing embedded within everyday devices
 - Increasing intelligence of everyday appliances
- Digital revolution
 - Infrastructure: Circuit-switched to IP-based networks
 - Analog TV to Digital TV
- Internet is ubiquitous
 - Being deployed within commercial channels
 - Business-to-Business commerce, secure transaction processing, banking
- Deregulation of global infrastructure
 - Multiple industries such as telecom, cable and utilities

Integrated Digital TV (iDTV)

- Currently need either iDTV or set-top box to receive digital television broadcasts
 - iDTV is basically a TV with an integrated set-top box
- Signals received via normal TV aerial, satellite dish or cable
 - Depends on condition and type of antenna
 - Free-to-air and pay channels available
 - Maybe xDSL?
- Connection or return channel for consumer interaction
 - e.g. POTS/ISDN/Cable
- Analog broadcasts WILL switch off at some point in time!
 - Within 10 years?
 - e.g. aiming for end 2006 in US, 2010 in UK
 - High broadcast coverage required to minimize impact on consumers

HDTV

- High Definition Television offers the consumer unprecedented broadcast picture quality and digital surround sound
- Six times the current standard broadcast resolution in U.S!
 - i.e., there are 6 times as many pixels in the same picture space
- HDTV sets are typically large scale, wide-screen, home-cinema, entertainment centers
- Success of HDTV still dependent on attractive content provision and lowering set costs (amongst other things!)

HDTV/EDTV/SDTV

- HDTV - High Definition TV
 - 720p vertical scanning lines or higher
 - 1920x1080i is true HDTV
 - 16:9 aspect ratio
- EDTV - Enhanced Definition TV
 - 480p vertical scanning lines or higher
 - Aspect ratio not specified
- SDTV - Standard Definition TV
 - Digital reception but can be less than EDTV resolution
 - Aspect ratio not specified

Digital TV Display Types



Plasma Display Panel (PDP)
Field Emission Display (FED)
Liquid Crystal Display (LCD)



Cathode Ray Tube (CRT)
Organic Light Emitting Device (OLED)
Liquid Crystal on Silicon (LCOS)
Digital Light Processor (DLP)



Receivers and Monitors

- DTV Receiver
 - Able to decode/process and display DTV broadcasts
 - These sets have an internal tuner circuit which allows it to receive DTV broadcast signals and display them in their standard or high-definition format
- DTV Monitor
 - Has no internal processing so it requires a set-top box or connection to a processing module
 - Is capable of displaying standard or high-definition images as required by DTV standards

Interlace/Progressive Scan

Interlace

First all odd lines scanned (1/60sec)



then all even lines (1/60sec)

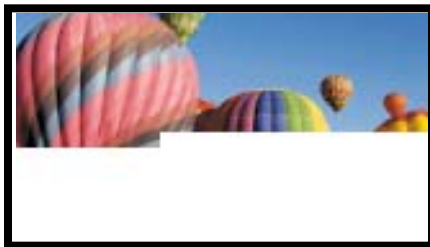


presenting a full picture (1/30sec)



Progressive

All lines scanned in single pass



presenting a full picture (1/60sec)



Aspect Ratio



4:3



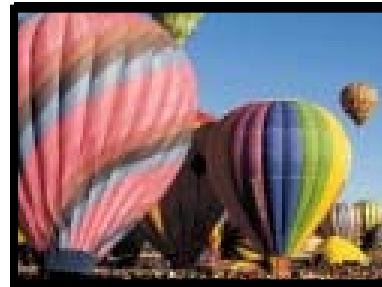
16:9

- The ratio between picture width and height
- 16:9 more closely represents cinema picture formats
- Digital TV receivers must be able to cope with different ratios and automatically present a picture dependent on the display format used
- Aspect Ratio Conversion (ARC) is a common function in modern TV sets

Aspect Ratio Conversion



HDTV Source 16:9



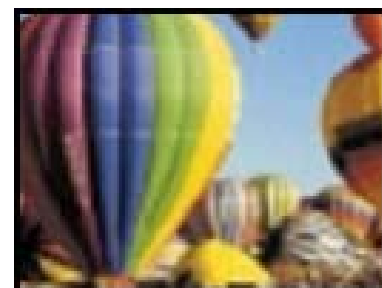
Normal 4:3



Letterbox



Pan & Scan

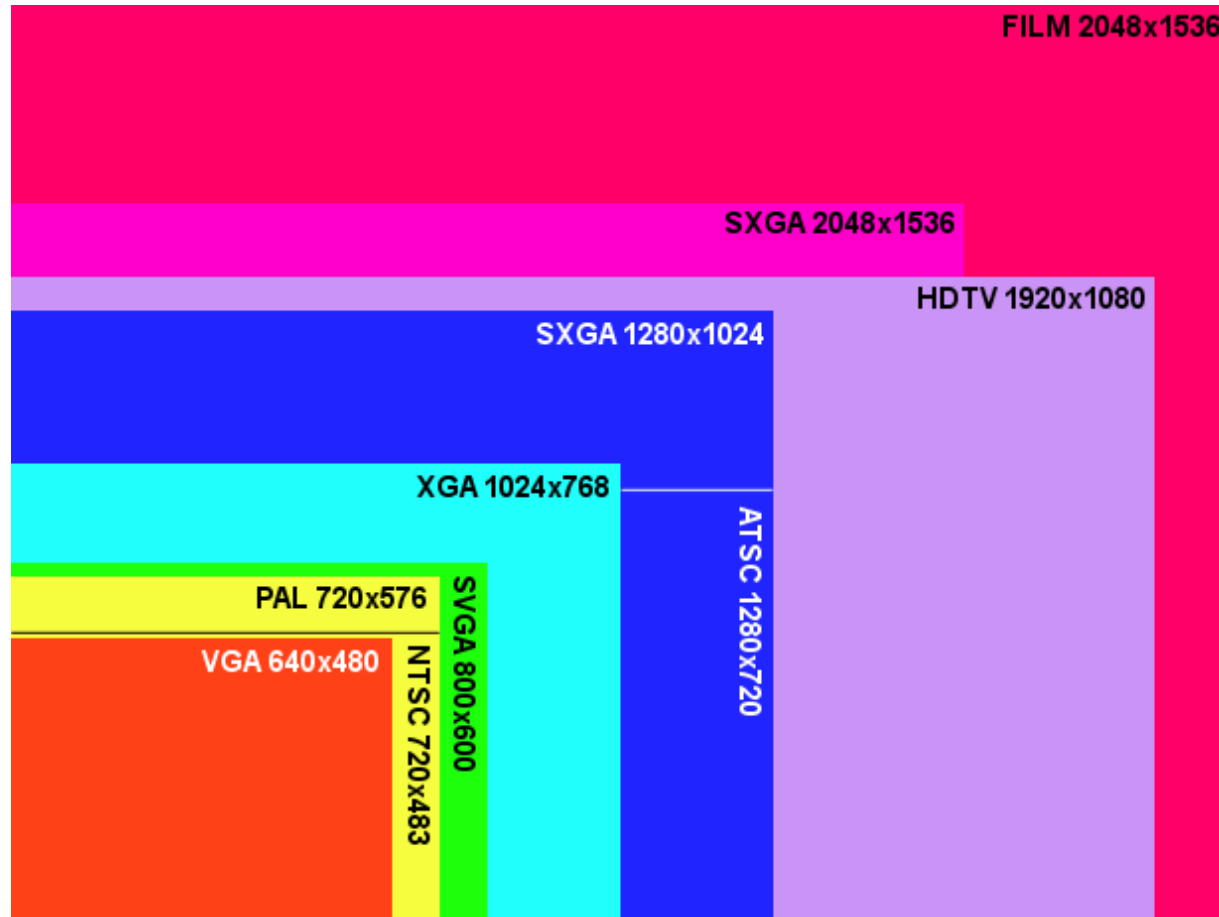


Zoom/Window



Anamorphic

Ratios and Resolutions



Courtesy: Snell & Wilcox



ATSC Table III

Scanning Formats

Definition	Lines/Frame	Pixels/Line	Aspect Ratios	Frame Rates
High (HD)	1080	1920	16:9	23.976p, 24p, 29.97p, 29.97i, 30p, 30i
High (HD)	720	1280	16:9	23.976p, 24p, 29.97p 30p, 59.94p, 60p
Standard (SD)	480	704	4:3, 16:9	23.976p, 24p, 29.97p, 29.97i, 30p, 30i, 59.94p, 60p
Standard (SD)	480	640	16:9	23.976p, 24p, 29.97p, 29.97i, 30p, 30i, 59.94p, 60p

- Table III is well known in the broadcast industry
- List of standard formats from ATSC A.53 DTV Standard
- 36 different formats available!
- Doesn't take into account line doubling, etc.

Displays Driving Performance

- Take an HDTV plasma display panel example:
 - 1920x1080 resolution
 - 24-bit pixels
 - 8-bit Red, Green and Blue values
 - 30 progressive frames per second

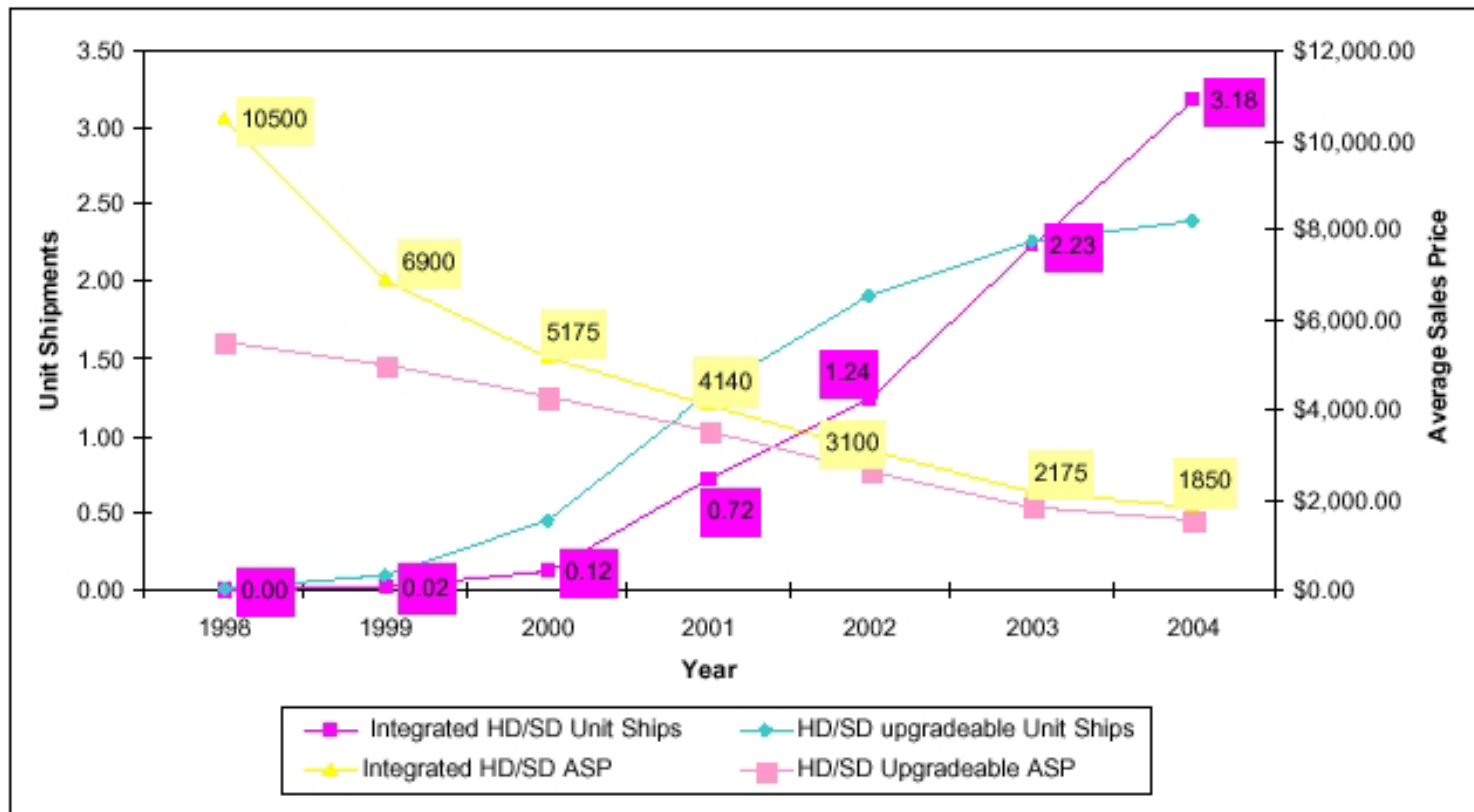
• Bandwidth = $1920 \times 1080 \times 24 \times 30 = 1.49\text{Gbps}$

Market Overview

- Various broadcast standards
 - Support different broadcast standards worldwide
 - DVB-T, ATSC, ISDB-T, (DMB-T?)
 - MPEG-2 predominantly used as DTV compression standard
- Provides improved quality
 - Support for HDTV
 - Clearer, multi-channel sound
 - Allows broadcasters flexibility in terms of bandwidth vs. quality

Worldwide Digital TV Forecast

DTV Unit Shipments and Average Sales Price, 1998-2004



Source: IDC, 2000

Digital TV Trends

- More Channels
 - Increased choices
 - More specialized channels
 - Immediate feedback to broadcasters
 - Maximum use of available bandwidth
- New Services
 - Wide-screen
 - Interactive services
 - New text channels
 - Sophisticated on-screen program information
 - Email facilities
- Improved Quality
 - Support for HDTV
 - No “ghosting” or other interference effects
 - Sharper digital sound
 - Allows broadcasters flexibility in terms of bandwidth vs. quality

DTV and Consumers

- 40% of consumers have no interest in digital TV*
- Happy with the services they already have
- This portion of the market is being targeted by FTA (free-to-air) digital broadcast support
- Analog WILL switch off
- New TVs will inherently support digital services
- Plug-in modules for upgrades?
- Logos appearing to help differentiate digital TVs from analog (for those who are interested)



The Market Continues to Grow Despite Tough Times

THE BIG PICTURE

STILL GOTTA HAVE IT

Despite a slumping economy, consumers are still eager to get their hands on the latest audio and video gear. And why not? It's mostly cheaper now.

CATEGORY	2001 UNIT SALES *	PERCENT CHANGE FROM 2000	2001 AVERAGE SELLING PRICE	PERCENT CHANGE FROM 2000
DIGITAL TELEVISION	325,000	230%	\$2,477	-31%
DVD	3,450,000	94	205	-25
DIGITAL CAMERA	3,500,000	66	286	-19
MP3/DIGITAL MUSIC PLAYER	125,000	59	212	-2
HOME THEATER SYSTEM	425,000	49	483	+22
HOME CD BURNER	125,000	47	374	-20
DIGITAL CAMCORDER	475,000	43	808	-16

*PROJECTED Data: Industry estimates, NPD Intellect Market Tracking

F.C.C. Schedule for HDTV

- 1997 HDTV schedule set and spectrum assigned
- 2002 All commercial stations to broadcast HDTV
- 2003 All non-commercial stations to broadcast HDTV
- 2004 75% of programming to be digitally simulcast
- 2005 100% of programming to be digitally simulcast
- 2006 Analog switch off, but only if 85% of market able to receive HDTV signals

HDTV

Accelerators/Inhibitors

- Accelerators

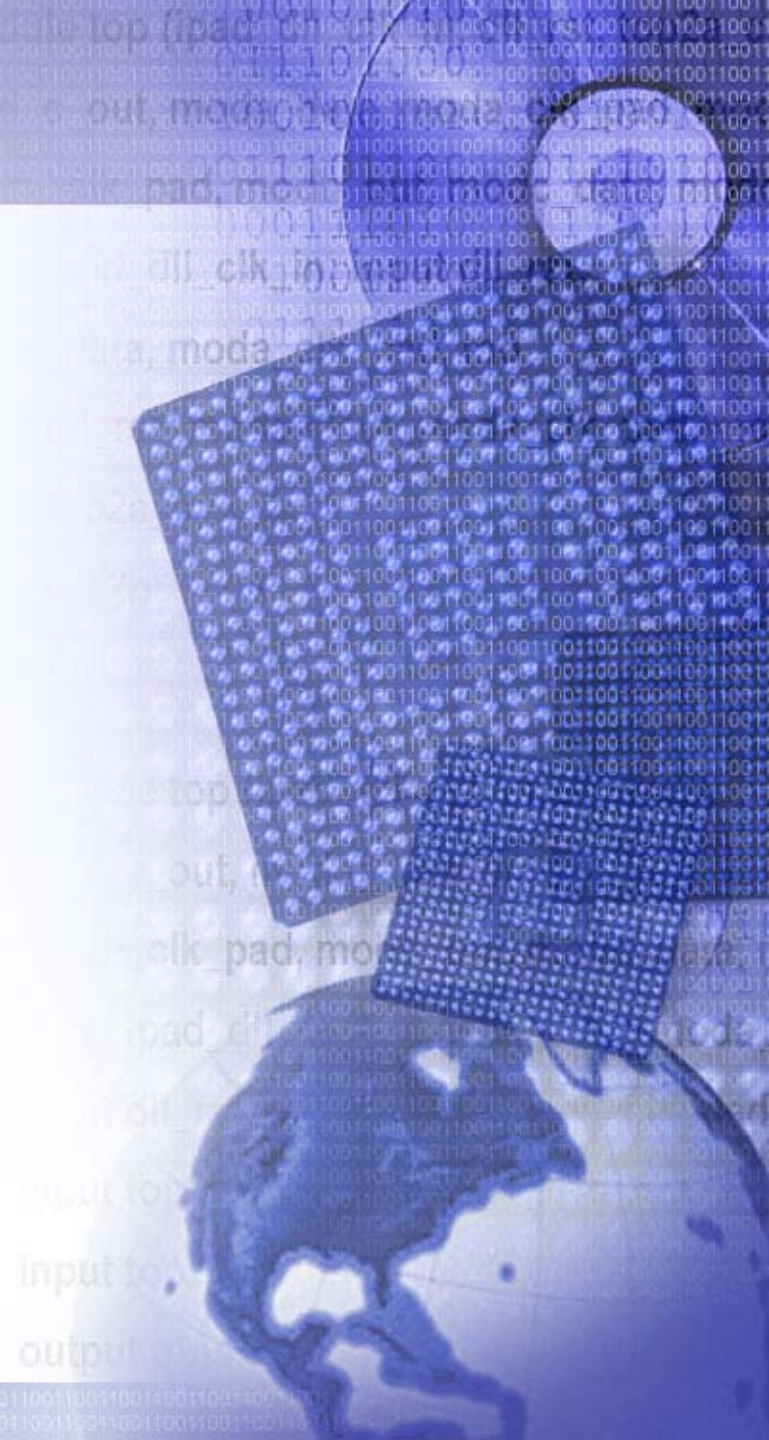
- Higher clarity of pictures (6 times the resolution of NTSC)
- Better color purity
- Better quality, multi-channel sound
- HDTV set costs falling
- HD production costs cheaper than film (in the long run)
- More HD content being produced
- Resolution of modulation scheme debates (8VSB vs. COFDM)

- Inhibitors

- Cost of sets still too high for widespread adoption
- Lack of consumer awareness about HDTV
- Consumer reluctance to change to HD/digital
- Still not enough HD content
- Land coverage of broadcasts
- No guarantees that standards will not change
- Bandwidth resources may be better used for multicasting SDTV content

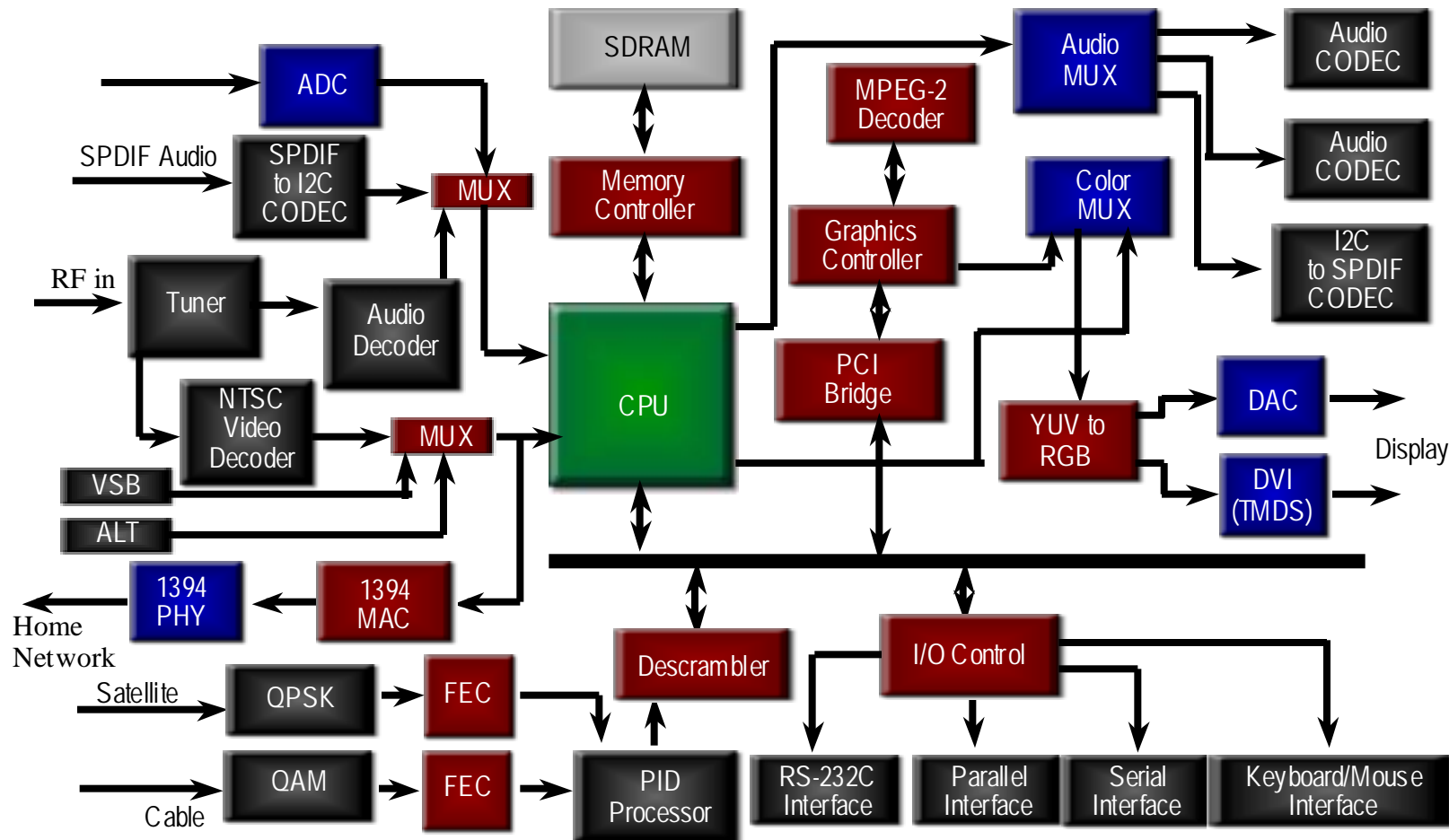


Digital TV System Overview





Digital TV System



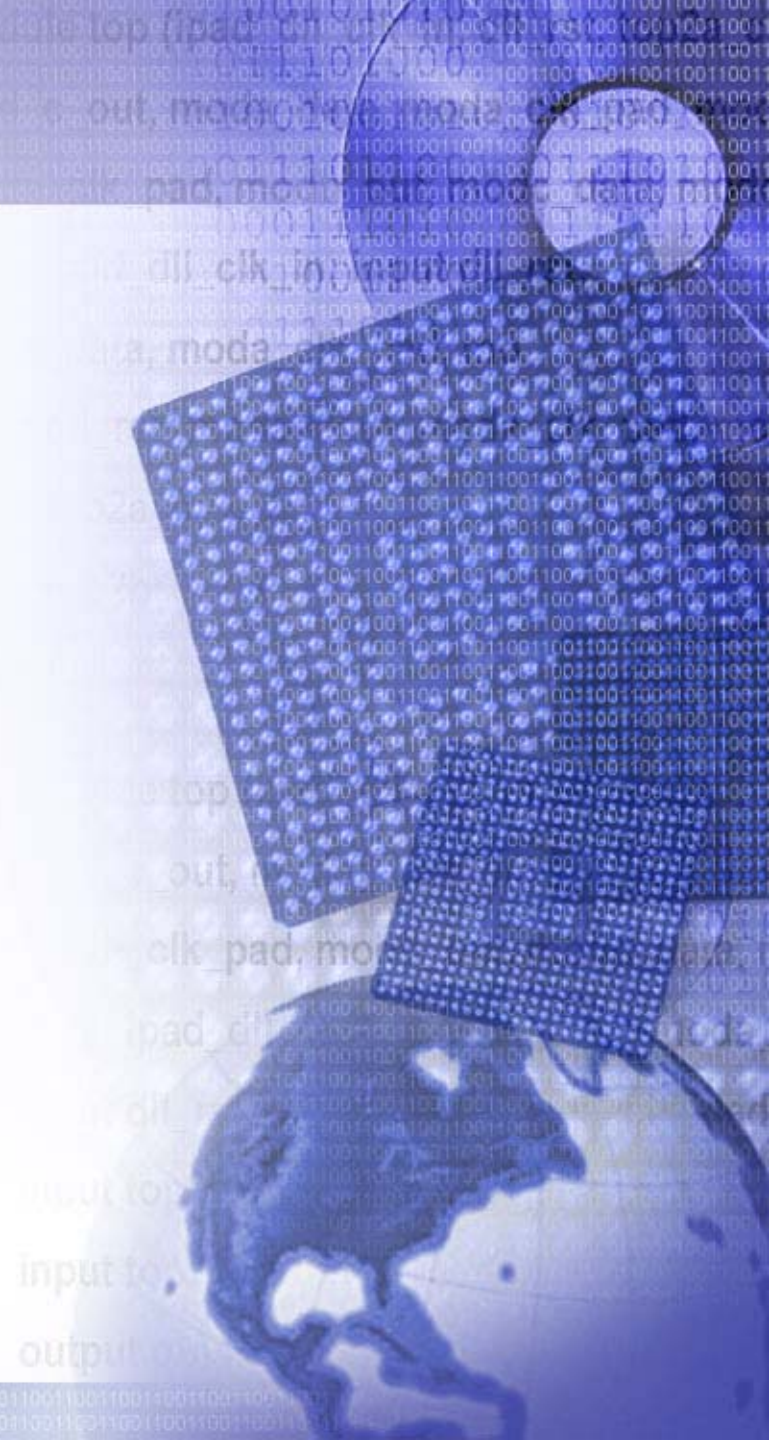
Digital	Memory	Mixed Signal	uP or uC	Programmable	IP Block
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Xilinx Value Proposition

Digital TV / HDTV

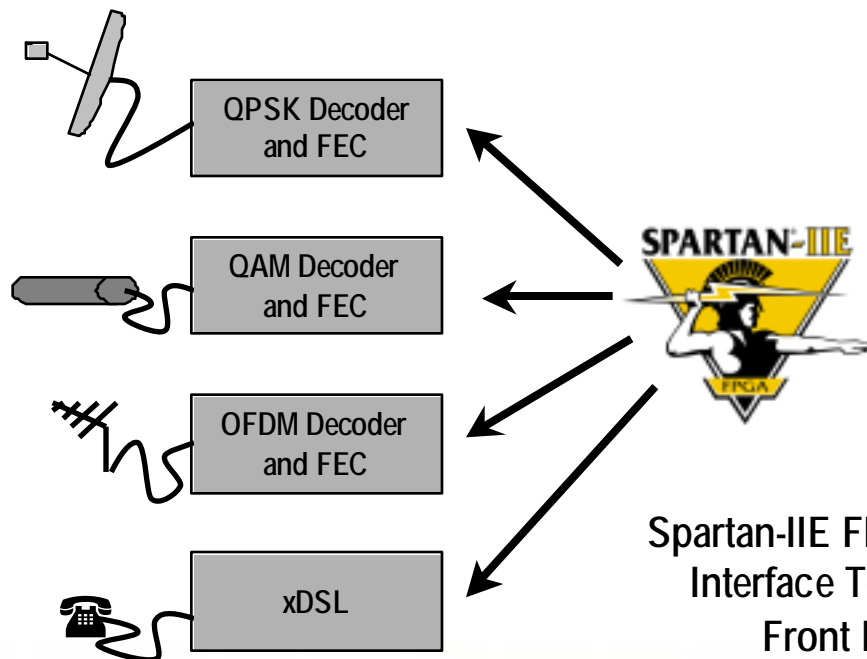


Xilinx Solutions in iDTVs

- Multiple responsibilities within the TV
 - Bridges
 - Enabling different technologies to co-exist
 - Forward Error Correction
 - Reed-Solomon, Viterbi, De-interleaving
 - Enabling broadband local loop in digital modems
 - xDSL, cable, satellite
 - MPEG co-processing
 - DCT/IDCT acceleration
 - Picture quality enhancements allow differentiation
 - Access points
 - Interfaces to broadband and home networks
 - Encryption/Decryption
 - DES, Triple DES, AES

Front End Interface

- Not cost effective to support multiple receivers
 - Cable, terrestrial, satellite and xDSL
 - Requires multiple iDTV designs

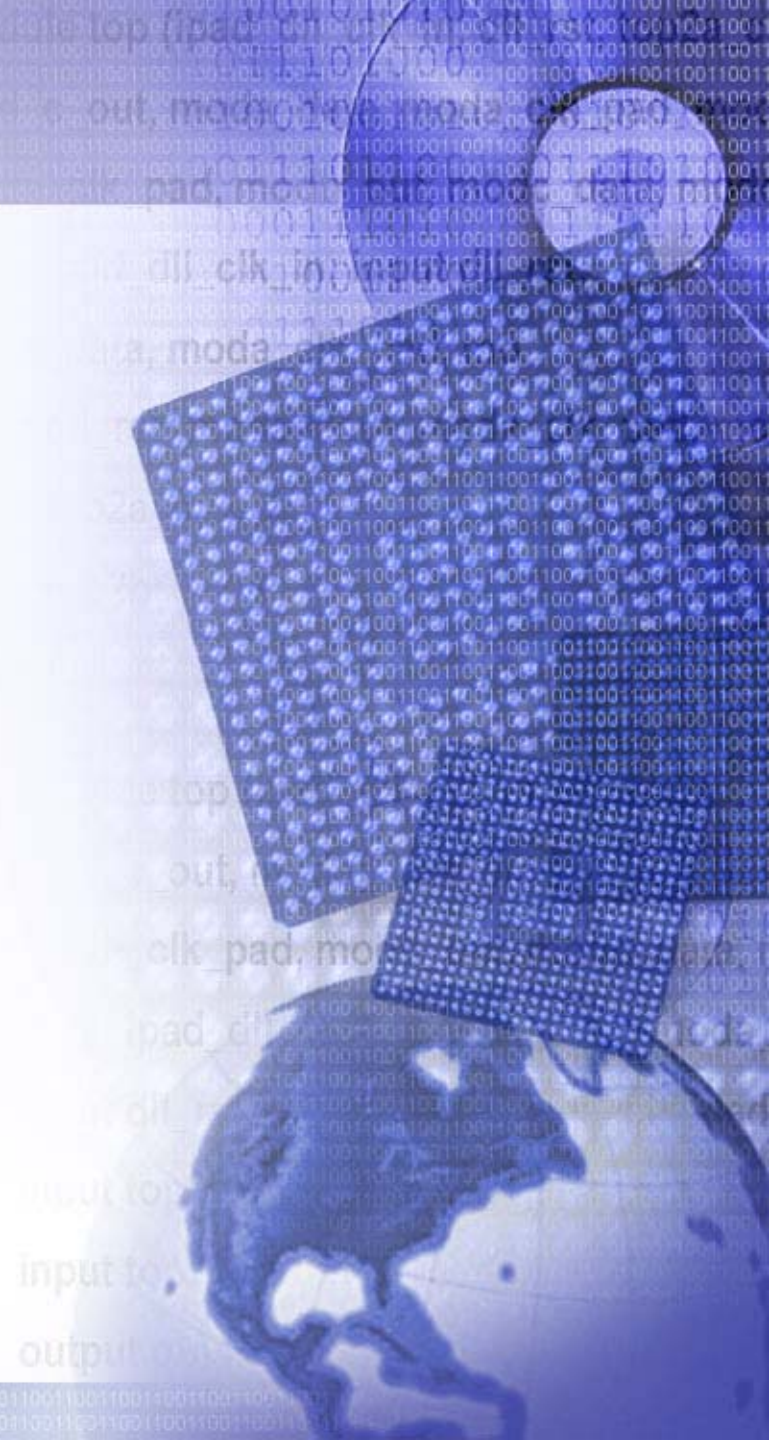


Interface required to support multiple ASSPs
Choice of ASSP influenced by broadcaster features

Spartan-IIE FPGA Allows Interface To Multiple Front Ends



Forward Error Correction



What Does FEC Do?

- Enables the receiver to detect and correct errors automatically without requesting retransmission
- Based on the addition of redundant parity information to the data being transmitted
- One metric of the quality of the communication link is measured in terms of Bit Error Rate (BER)
- Widely used in real-time systems for the transmission of audio and video data

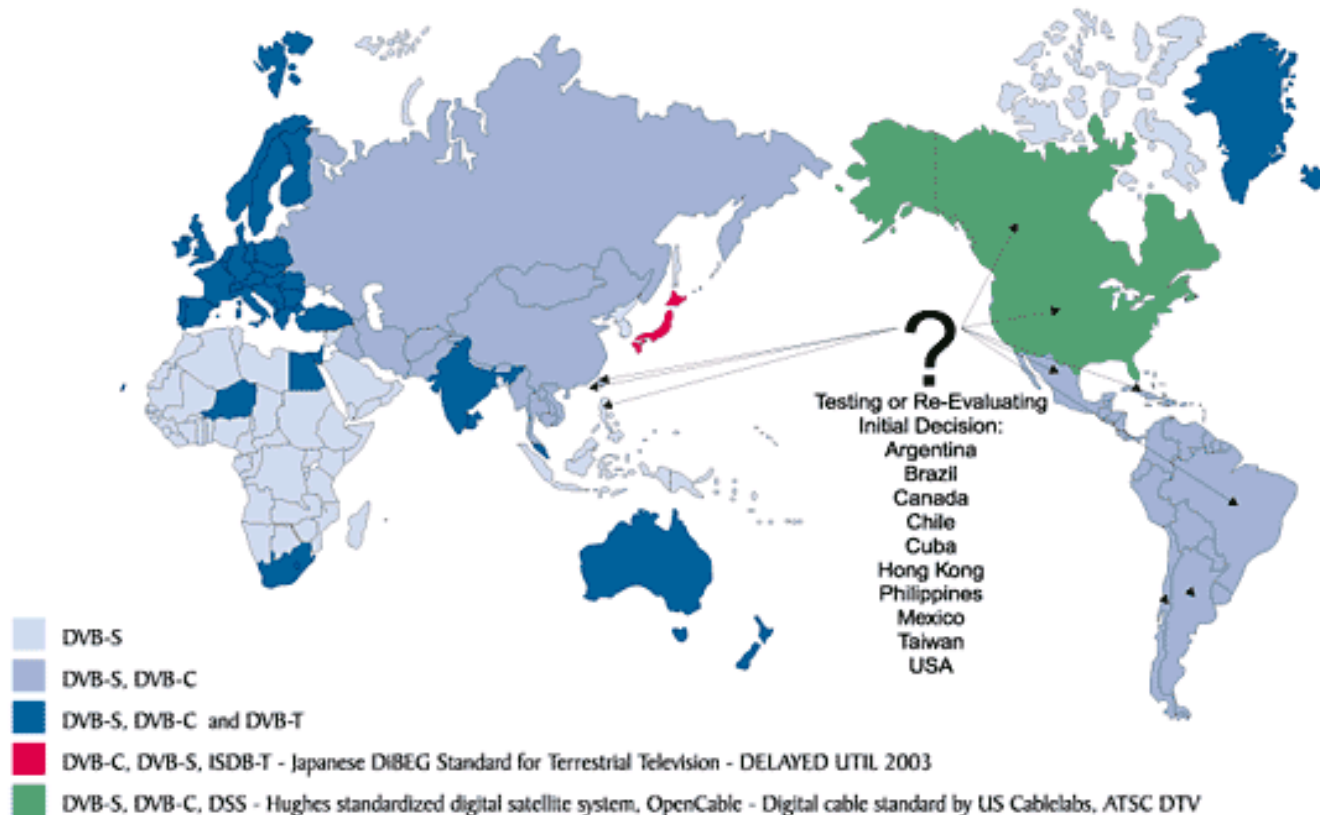
DVB

- Digital Video Broadcasting organization
- Formed in September 1993
- DVB now has more than 300 members
 - Broadcasters
 - Manufacturers
 - Network operators
 - Regulatory bodies
- Mission : “The creation of a harmonious digital broadcast market for all service delivery media”
- Mainly covers Europe but also promoting in U.S. and Japan

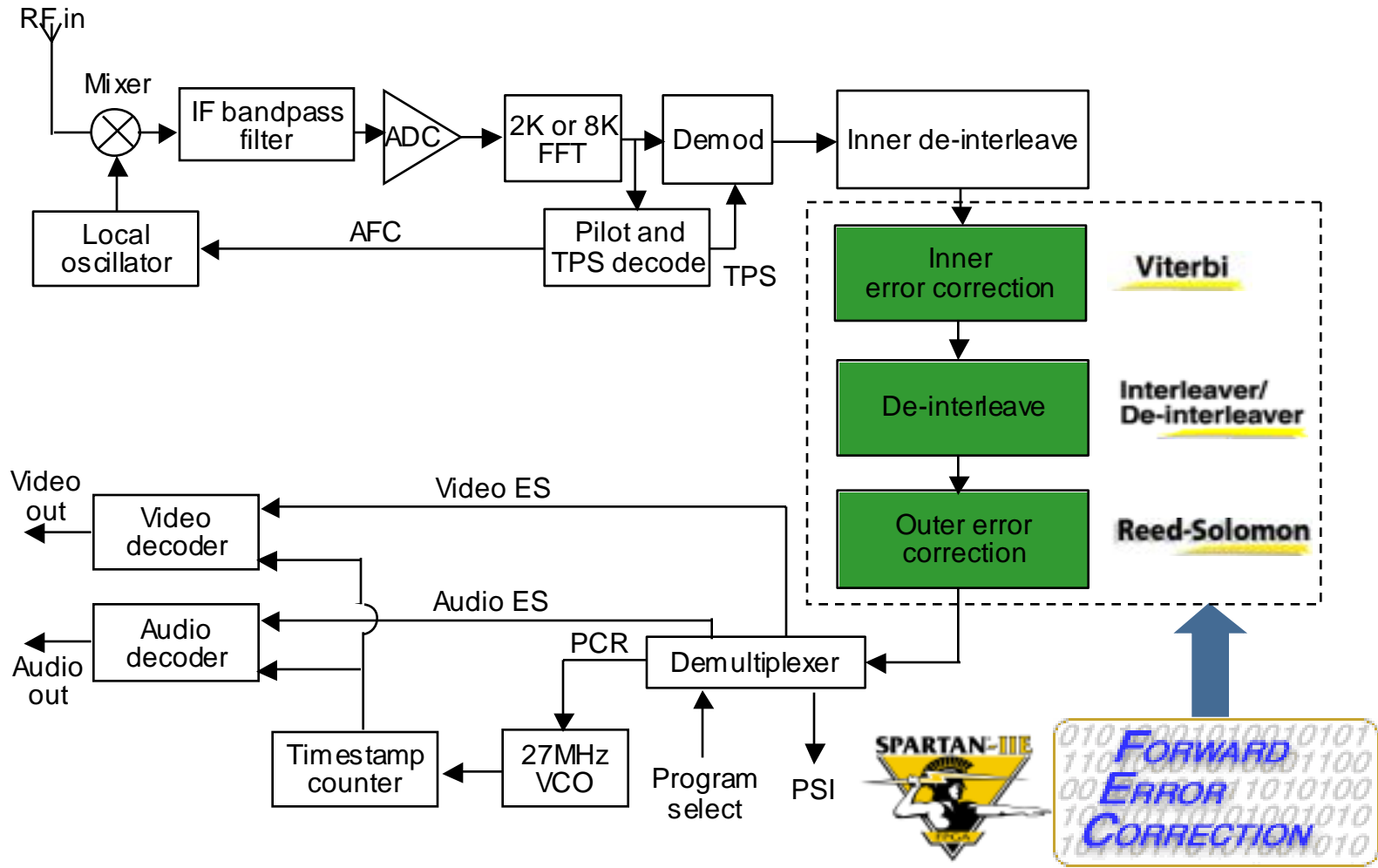


DVB Worldwide Adoption

Digital Standards - Worldwide 2000



DVB-T (Terrestrial) FEC



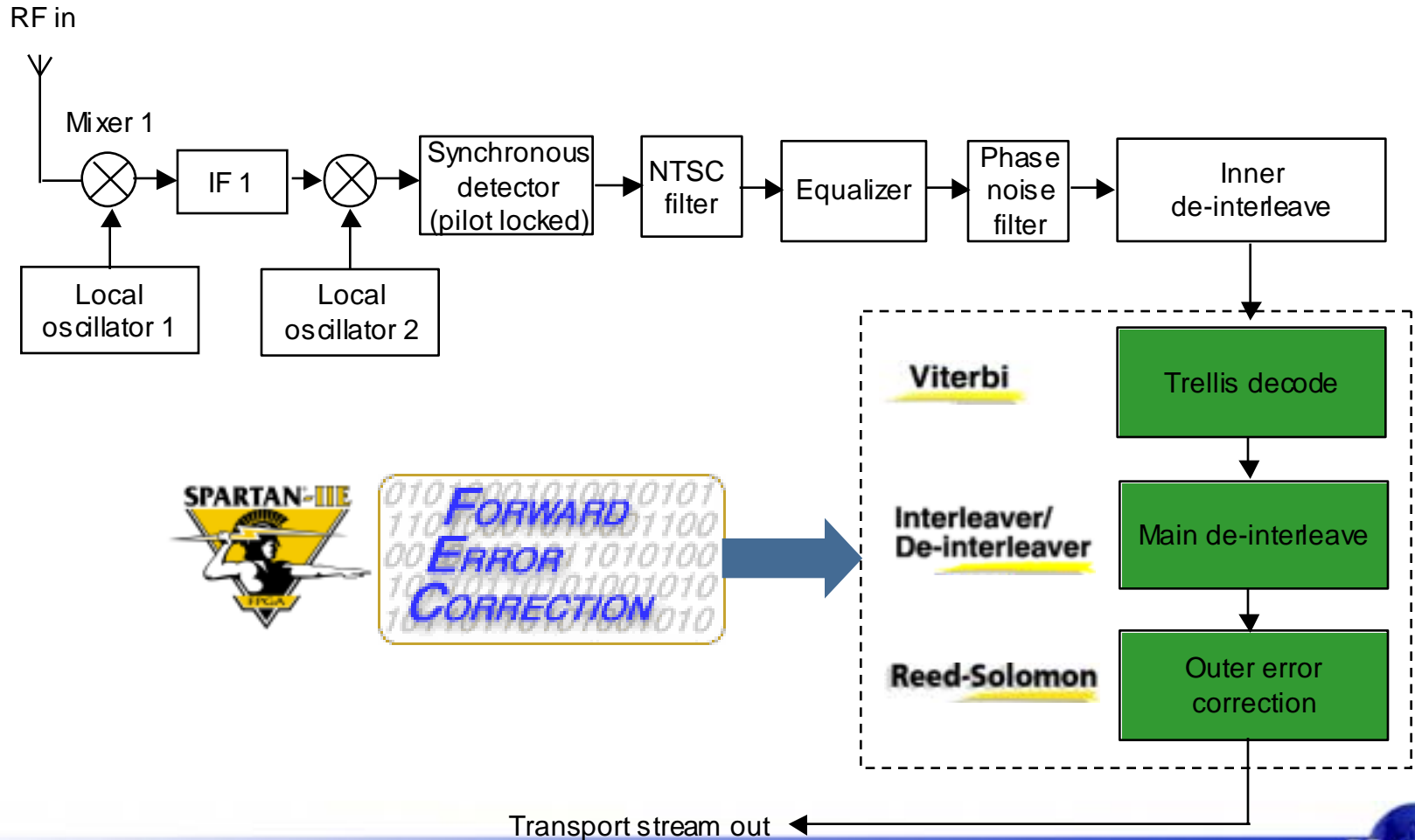
ATSC

- Advanced Television Systems Committee
- Formed in September 1982
- ATSC now has more than 200 members
- Broadcasters
- Manufacturers
- Network operators
- Regulatory bodies
- Co-ordinates television standards among different communications media focusing on digital television, interactive systems, and broadband multimedia communications. Also developing digital television implementation strategies
- Adopted by U.S., Canada, S. Korea, Taiwan and Argentina

a — t — s c

Advanced Television Systems Committee

ATSC - 8VSB (Terrestrial) FEC



ISDB

- Integrated Service for Digital Broadcast
- Developed and adopted by Japan
- Similar to DVB
 - ISDB-T uses OFDM (Orthogonal Frequency Division Multiplex)
 - Same channel coding (FEC) - Reed Solomon and convolutional/Viterbi
- Terrestrial has some additional features
 - RF channel split into 13 segments
 - 3 different modulation schemes can be used on different segments at the same time
 - Optional time interleaver for improved mobile reception
 - 4K FFT mode available

DMB

- Digital Multimedia Broadcasting
- Jointly developed by Qinghua University in Beijing and US-based Legend Silicon
- Proposed for Chinese and Hong Kong markets
- DMB-T (terrestrial) uses TDS-OFDM
- Time domain synchronous OFDM
- Said to provide better synchronization with mobile devices

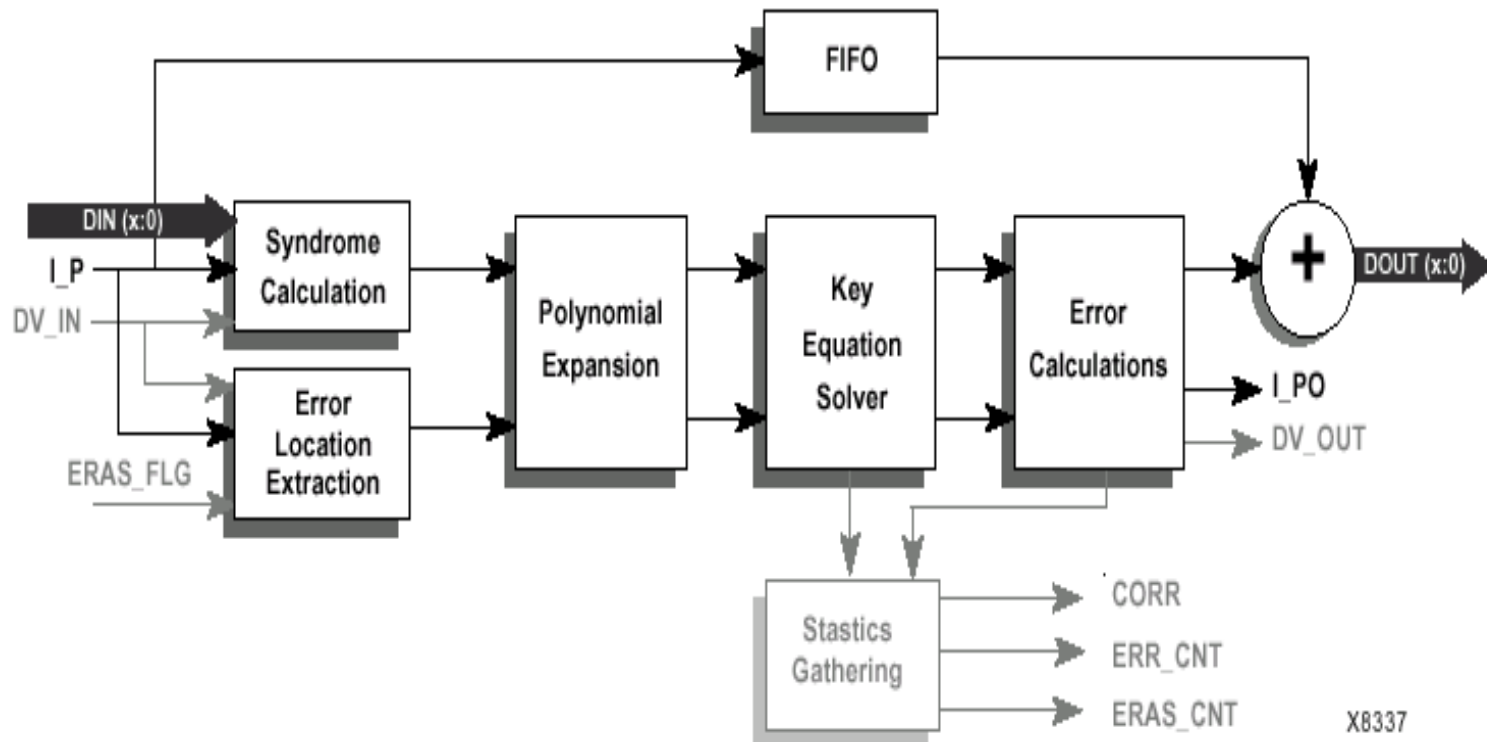
Summary of Terrestrial Systems

Systems	ATSC 8-VSB	DVB-T COFDM	ISDB-T BST-OFDM
Video	Main Profile Syntax of ISO/IEC 13818-2 (MPEG-2 video)		
Audio	ATSC Standard A/52 (Dolby AC-3)	ISO/IEC 13818-2 (MPEG-2 Layer II Audio) and Dolby AC-3	ISO/IEC 13818-7 (MPEG-2 AAC audio)
Transport Stream	ISO/IEC 13818-1 (MPEG-2 TS) transport stream)		
Outer Coding	R-S (207, 187, t=10)	RS (204, 188, t=8)	
Inner Coding	Rate 2/3 trellis code	Punctured convolutional code : Rate 1/2, 2/3, 3/4, 5/6, 7/8 Constraint length = 7, Polynomials (octal) 171, 133	
Inner Interleaver	12 to 1 trellis code interleaver	Bitwise interleaving and frequency interleaving	Bitwise interleaving, frequency interleaving and selectable time interleaving
Data Randomization	16-bit PRBS	16-bit PRBS	16-bit PRBS
Modulation	8-VSB	COFDM QSPK, 16QAM, 64QAM Hierarchical modulation : multi resolution constellation (16QAM and 64QAM) Guard interval : 1/32, 1/16, 1/8 and 1/4 of OFDM symbol 2 modes: 2K & 8K FFT	BST-OFDM with 13 frequency segments DQPSK, QPSK, 16QAM, 64QAM Hierarchical modulation: three different modulations on 13 segments Guard Interval: 1/32, 1/16, 1/8 and 1/4 of OFDM symbol 3 modes: 2K, 4K and 8K FFT

Reed-Solomon Encoder / Decoder

- Reed-Solomon
 - An error-correcting coding system that corrects multiple errors, especially burst-type errors in communication systems
 - Transmitter (encoder)
 - Data is encoded to be corrected in an event it acquires errors
 - Receiver (decoder)
 - Uses the appended encoded bits to determine errors
 - Corrects the errors upon reception of the transmitted signal

Reed-Solomon Decoder Block Diagram for iDTV



X8337

Reed-Solomon GUIs

- Parameterizable encoder and decoder cores available from Xilinx
- Simply select DVB/ATSC from the *Code Specification* menu
- Reed-Solomon tutorials online at Xilinx IP Center

Reed-Solomon Encoder LogiCORE Setup XRSENC V1.0.0

Component Name:

Code-Block Parameters

Code Specification:

Symbol Width:

Field Polynomial:

Generator Start:

Scaling Factor (h):

Data Symbols (k):

Symbols Per Block (n):

Optimization

Area (Latency = 2)

Speed (Latency = 3)

Create RPM

Programming

Log



Reed-Solomon Decoder

DVT Examples

Features	ATSC 1	ATSC 2	ATSC 3	ATSC 4	DVB 1	DBV 2	DBV 3	DBV 4
Generator Start	0	0	0	0	0	0	0	0
k	1	1	1	1	1	1	1	1
k	187	187	187	187	188	188	188	188
n	207	207	207	207	204	204	204	204
Polynomial	285	285	285	285	285	285	285	285
Symbol Width	8	8	8	8	8	8	8	8
Sync Mode	Start Pulse	Start Pulse	Start Pulse	Start Pulse	Start Pulse	Start Pulse	Start Pulse	Start Pulse
Clock Enable	No	Yes	Yes	Yes	No	Yes	Yes	Yes
Synchronous Reset	No	Yes	Yes	Yes	No	Yes	Yes	Yes
Delayed Original Data	No	No	Yes	Yes	No	No	Yes	Yes
Erasure Decoding	No	No	No	Yes	No	No	No	Yes
Clock Periods Per Symbol	1	1	1	1	1	1	1	1
Memory Style	Automatic	Automatic	Automatic	Automatic	Automatic	Automatic	Automatic	Automatic
Processing Delay	294	294	294	525	204	204	204	357
Latency	507	507	507	738	414	414	414	567
Xilinx Device	XC2V250 -FG256-5	XC2V250 -FG256-5	XC2V250 -FG256-5	XC2V500 -FG256-5	XC2V250 -FG256-5	XC2V250 -FG256-5	XC2V250 -FG256-5	XC2V500 -FG256-5
Area (Slices)	754	785	785	1793	619	646	646	1476
Slices Remaining	782	751	751	1279	917	890	890	1596
Maximum Clock Frequency	100 MHz	98 MHz	100 MHz	87 MHz	98 MHz	98 MHz	92 MHz	89 MHz

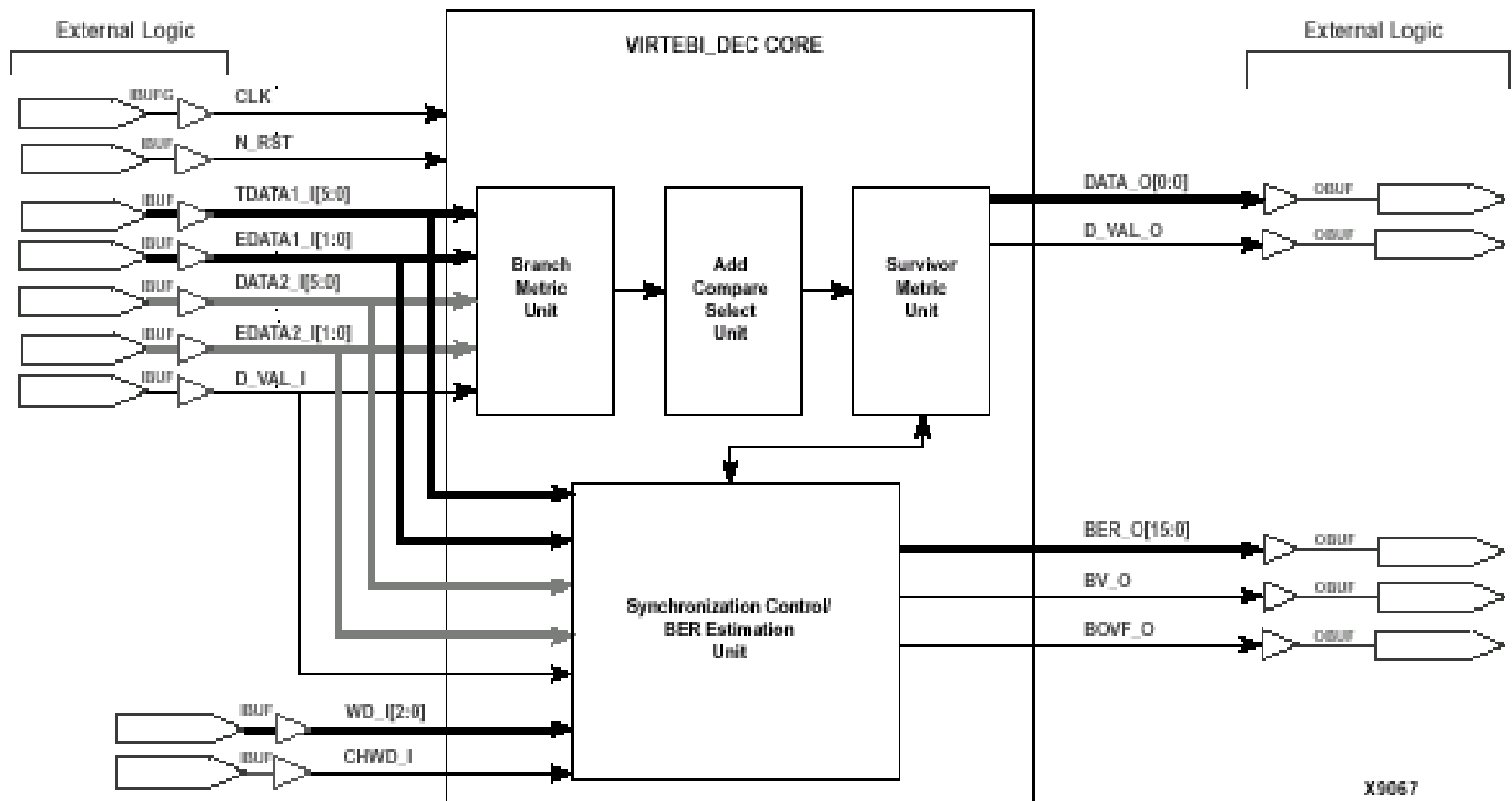
Reed-Solomon IP Solutions - Advantages

- The Xilinx decoder core is half the size of any competitor's offering
- Automatically configured from user parameters
 - Supports all major coding standards and custom implementations
- Can be optimized for area or speed
- Incorporates Xilinx Smart-IP technology for design predictability

Viterbi

- Viterbi algorithm
 - It is a convolutional code to correct random errors
 - It minimizes the number of sequences in the trellis search as new data is received by the demodulator
 - Developed by Dr. Andrew J. Viterbi
 - Co-founder, Retired Vice chairman, Board of Directors of QUALCOMM

Viterbi Decoder Block Diagram

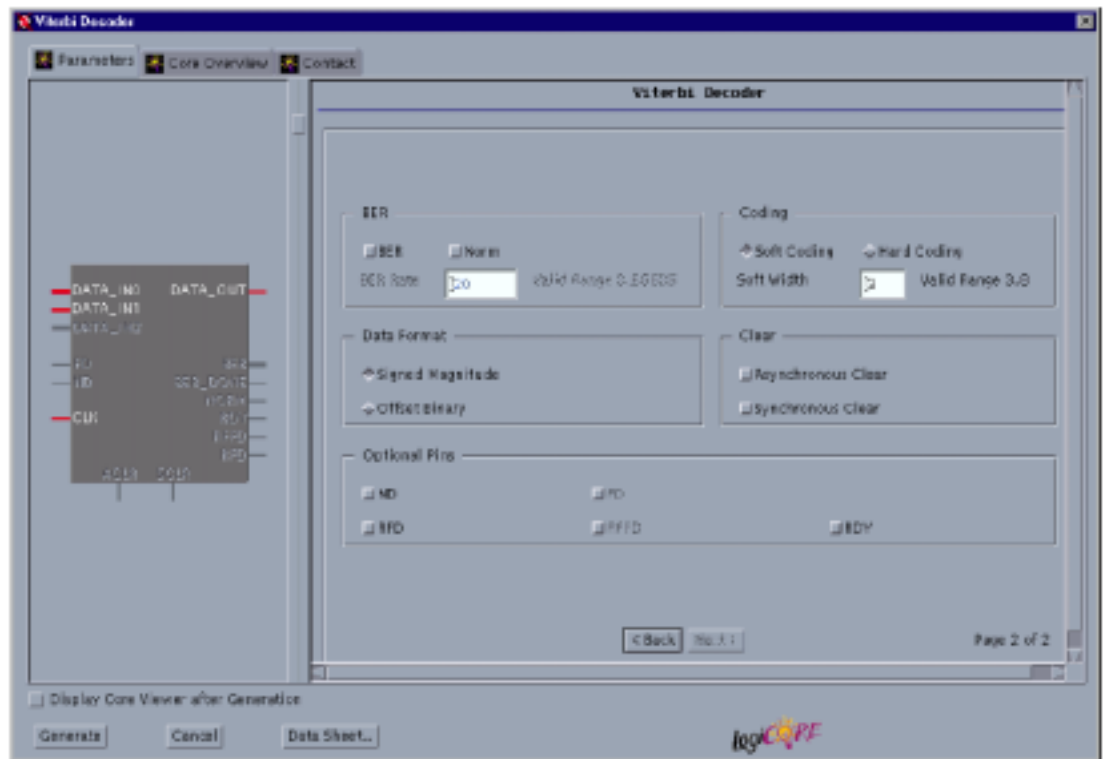


Viterbi Decoder IP

- Decoder of convolutional codes
- Customized VHDL source code available, allowing generation of different netlist versions
- Customized testbench for pre- and post-synthesis verification supplied with the module

Viterbi LogiCore GUI

- Fully parameterizable - includes parallel, serial & puncturing options
- Order DO-DI-VITERBI
- More info at
- <http://www.xilinx.com/ipcenter>



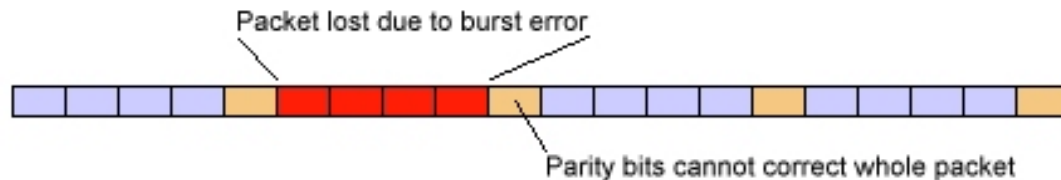
Spartan FPGA Based Viterbi Decoder

Spartan-II FPGAs Based Viterbi Decoder Specifics

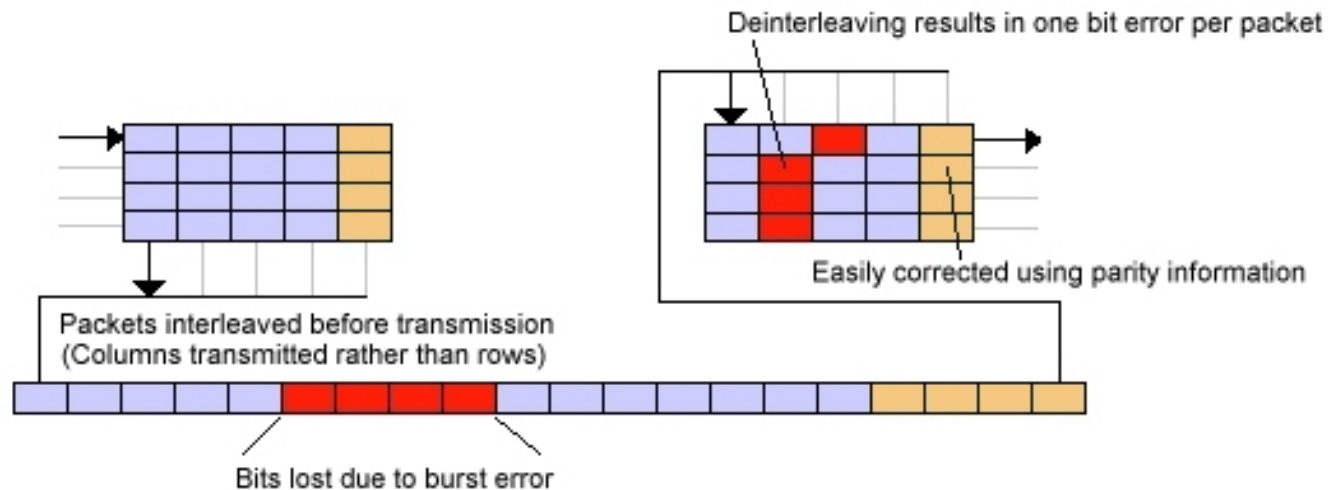
Product Families Supported	Spartan, Spartan-II, Virtex, Virtex-E
Device Tested	XC2S50-6
CLBs	495
Clock IOBs	1
IOBs	34
Performance (MHz)	56
Special Features	4 BlockRAMs

Outer Interleaver

RS decoder can only correct a limited amount of errors per packet:

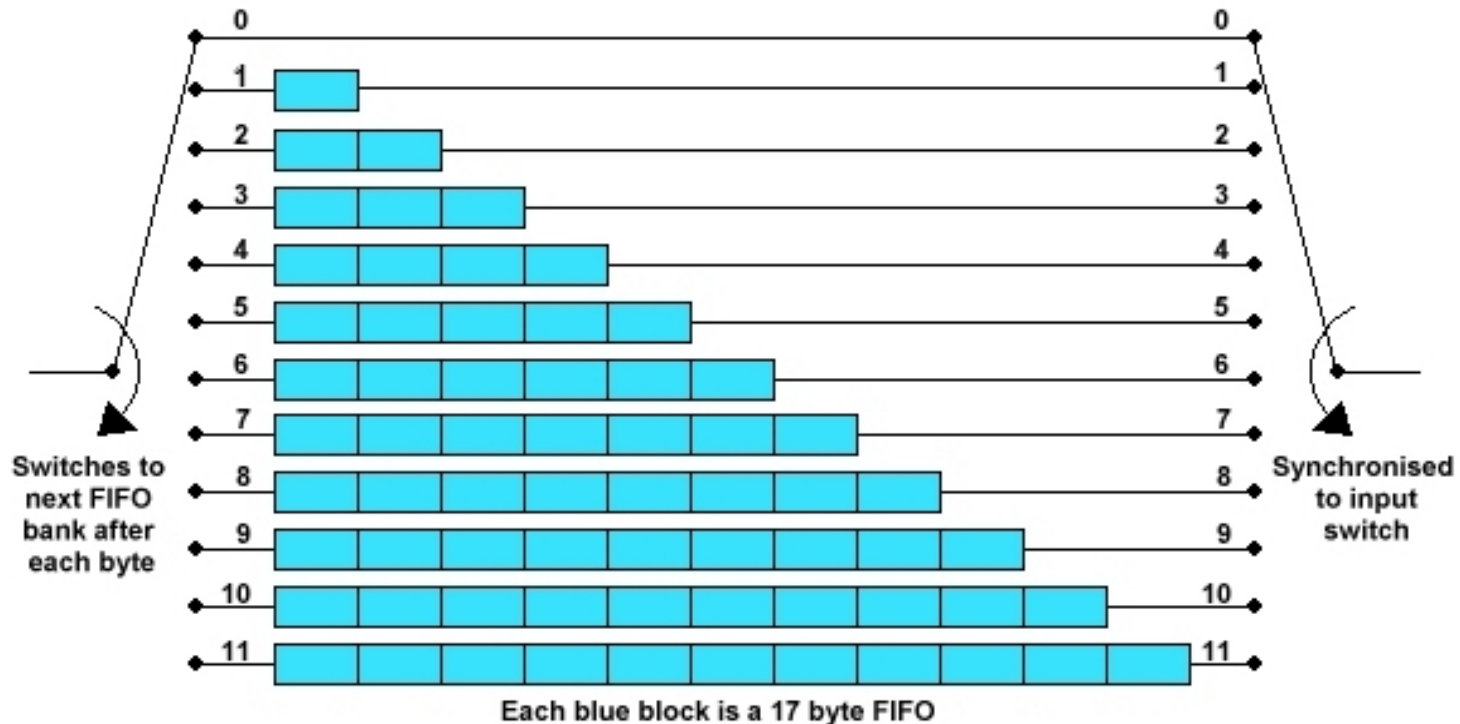


Interleaving spreads burst errors across several packets:



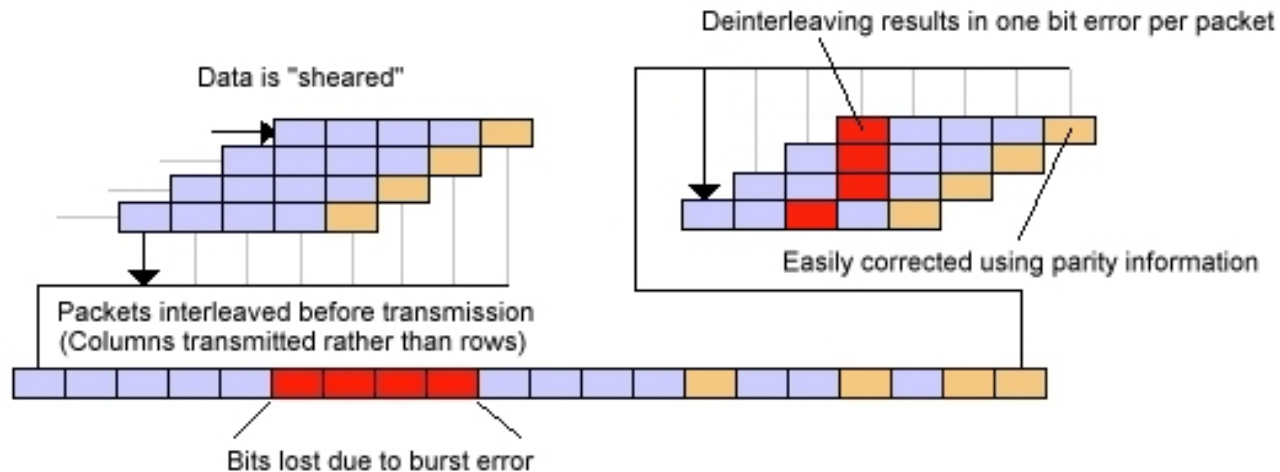
DVB Outer Interleaver

- Previous interleaver example was actually block based whereas DVB version is convolutional (Forney algorithm)
- Error dispersion idea is basically the same



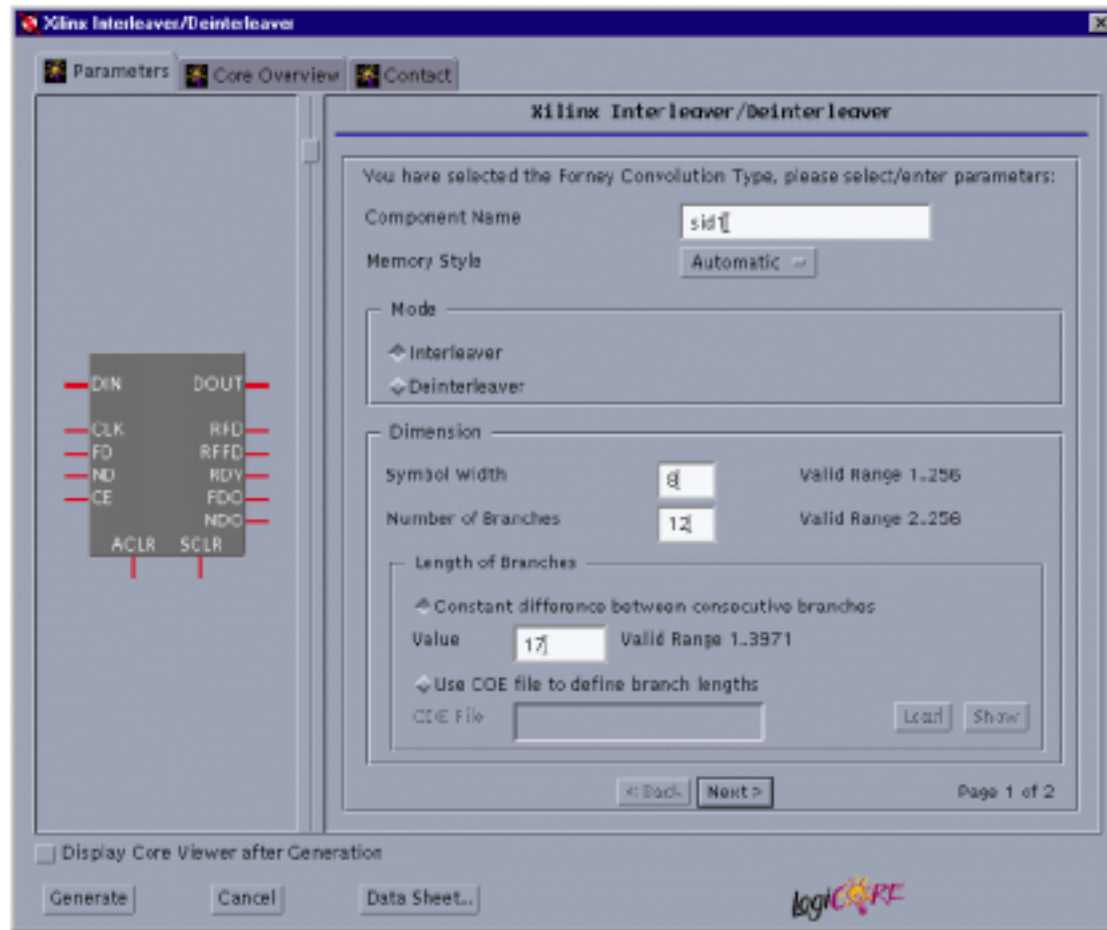
Convolutional Interleaver

- Data is effectively sheared in a DVB interleaver:



This has the advantage of needing less memory for implementation

Xilinx Interleaver/Deinterleaver GUI



Interleaver/Deinterleaver iDTV Example

Options	DVB 1	DVB 2
Mode	Interleaver	De-interleaver
Number of Branches	12	12
Branch Length Constant	17	17
Symbol Width	8	8
Pipelining	Maximum	Maximum
Optional Pins	FDO, RDY, RFFD	FDO, RDY, RFFD
Memory Style	Automatic	Automatic
Create RPM	No	No
Xilinx Device	XC2V40-5	XC2V40-5
Use IOB Flip-Flops	No	No
Area (slices)	79	110
Number of Block RAMs	1	2
Maximum Clock Frequency	187 MHz	183 MHz

FEC Summary

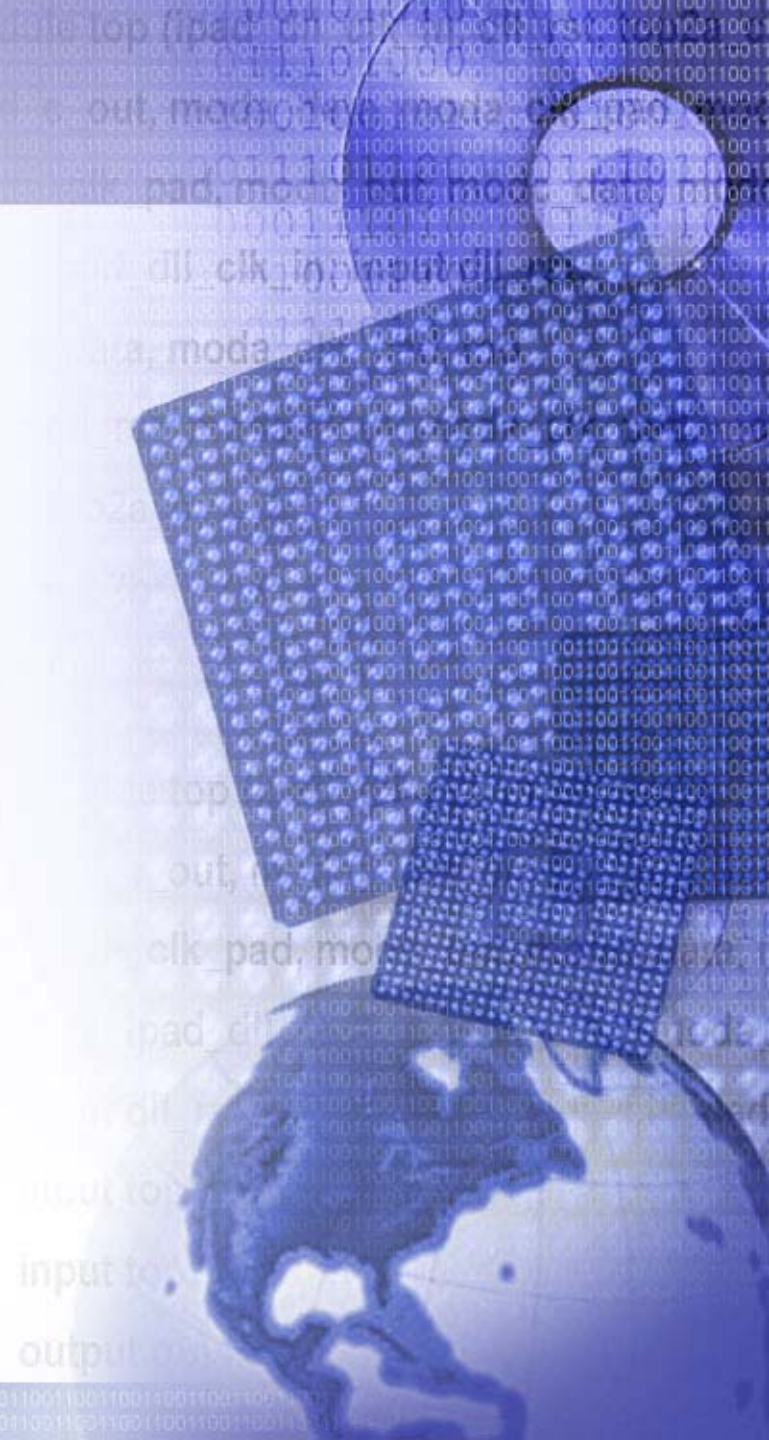
- Range of parameterizable cores available
 - Reed Solomon encoder/decoder
 - Convolutional encoder
 - Viterbi decoder
 - Interleaver/deinterleaver
 - Turbo codecs
- Intuitive generator GUI enables fast core production
- Tutorials and core details available at...

http://www.xilinx.com/ipcenter/fec_index.html





MPEG



The MPEG Algorithm

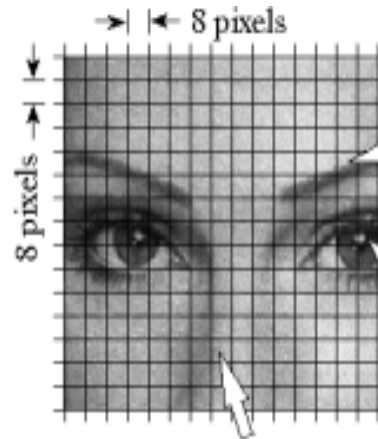
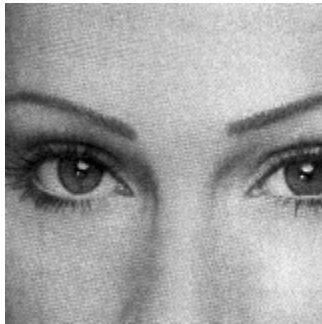
- The MPEG Encoder is composed of a number of discrete algorithmic sections:
- Temporal Processing
 - Seeking out and removing temporal redundancy
 - Involves storing several successive images and performing motion estimation, compensation and simple algorithmic processing to derive a pixel-by-pixel difference signal
- Spatial Processing
 - Uses DCT to remove the high frequencies not discernable by the human eye.
- Statistical or Variable Length Encoding (VLC) to remove redundancy in the output from the DCT

DCT/IDCT Concept

- What is DCT?
 - Returns the discrete cosine transform of 'video/audio input'
 - Can be referred to as the even part of the Fourier series
 - Converts an image or audio block into its equivalent frequency coefficients
- What is IDCT?
 - The IDCT function is the inverse of the DCT function
 - The IDCT reconstructs a sequence from its discrete cosine transform (DCT) coefficients

DCT/IDCT Concept

Original Image



234	224	224	217	217	203	189	196
210	217	209	189	208	224	217	224
196	217	210	224	203	203	196	189
210	203	196	203	182	203	182	189
205	224	203	217	196	175	154	140
182	189	168	161	154	128	119	112
178	154	128	109	140	109	119	94
154	98	105	91	105	61	112	94



DCT

Frequency Coefficients Compared to Magnitude Thresholds, Resulting in Compressed Data Stream

Restored Image
(Notice Lesser Image Quality)



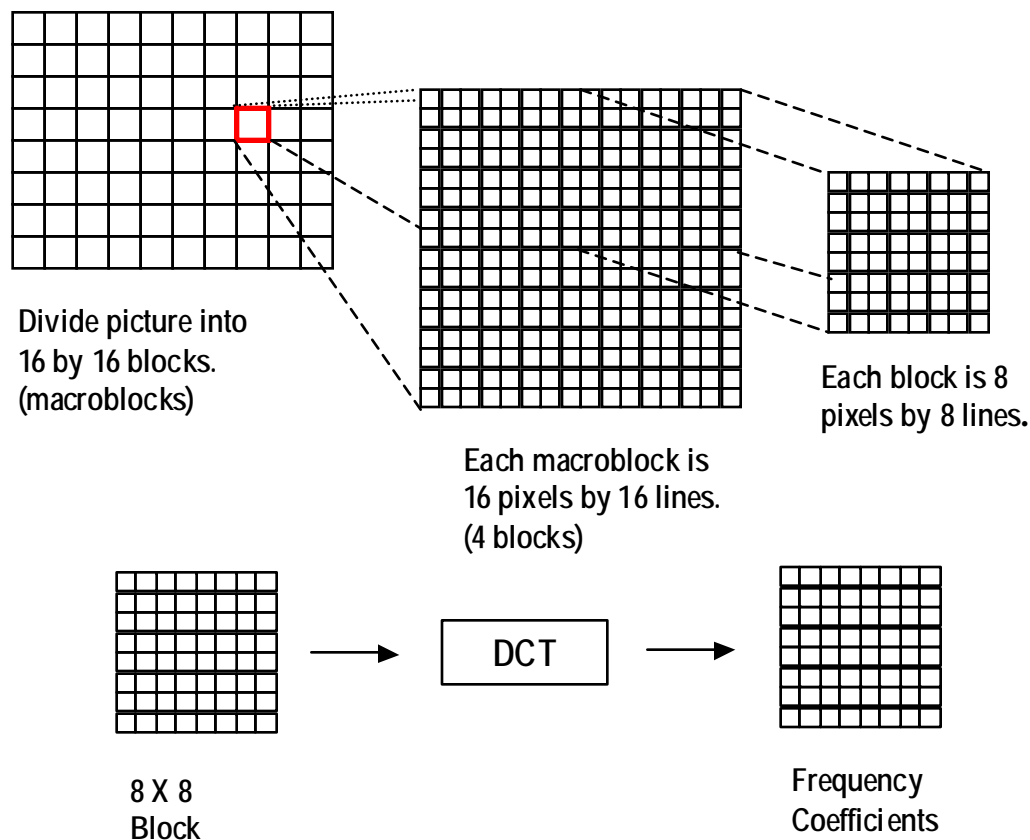
154	134	175	182	189	168	217	175
134	147	168	154	168	168	196	175
175	154	200	175	189	182	196	182
175	168	168	168	140	175	188	203
133	168	154	196	175	189	203	154
168	161	141	168	154	154	189	189
147	161	175	182	189	175	217	175
175	175	200	175	189	175	175	182

42	38	35	28	42	49	35	42
49	49	35	28	35	35	35	42
42	21	21	28	42	35	42	28
21	35	35	42	42	28	28	14
56	70	77	84	91	28	28	21
70	126	133	147	161	91	35	14
126	200	189	182	175	175	35	21
49	189	145	210	182	84	21	15

IDCT

The image is broken into 8x8 groups, each containing 64 pixels. Three of these 8x8 groups are enlarged in this figure, showing the values of the individual pixels, a single byte value between 0 and 255.

DCT/IDCT Concept



Detailed steps in dissecting a typical digital still image prior to being DCT transformed

DCT/IDCT Compression

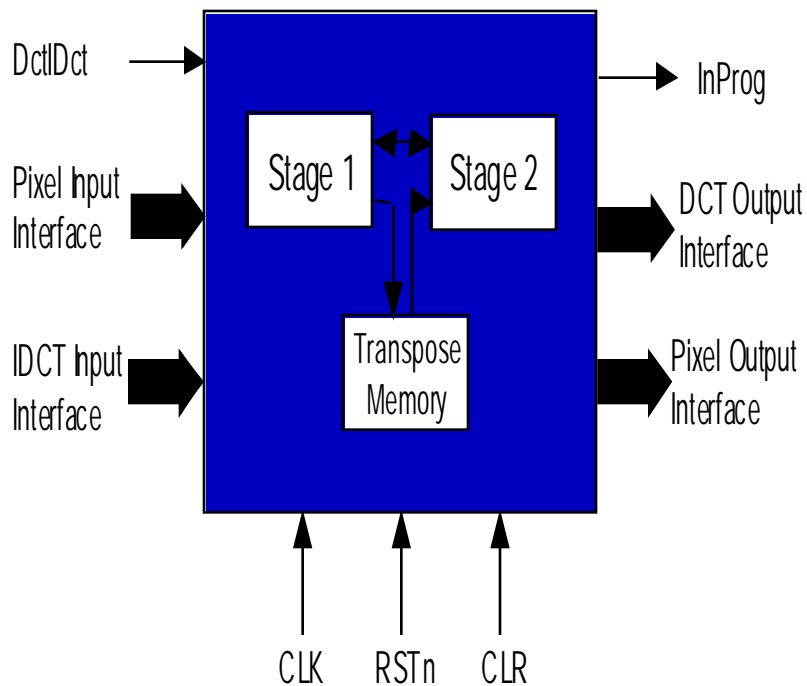
- Compression allows increased throughput through transmission medium
 - Video & audio compression makes multimedia systems very efficient
 - Increases CPU bandwidth
 - Higher video frame rates
 - Better audio quality
 - Enables multimedia interactivity
- DCT/IDCT are widely used in video & audio compression

Spartan-II E DCT/IDCT LogiCore Features

- Combined DCT/IDCT core
- Continuous one symbol per cycle processing capability
- Internal precision
 - 14 bit cosine coefficients
 - 15 bit transpose memory
- Optimized for specific Xilinx architecture
- Fully compliant with the JPEG standard (ISO/IEC10918-1)
- Supplied with Verilog and VHDL test benches



DCT/IDCT Core Overview

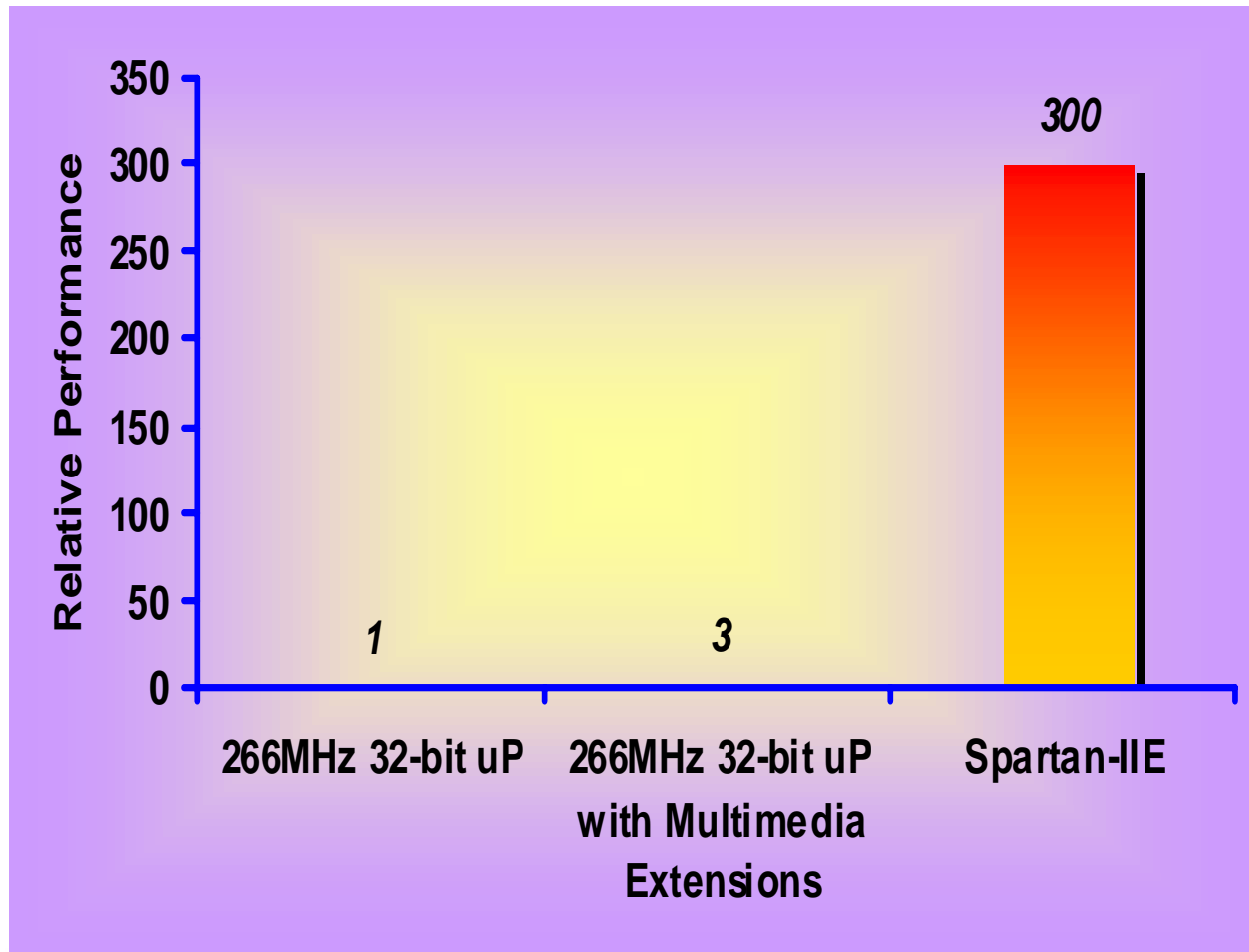


Half-Duplex Operation

Forward or Reverse, Not both simultaneously

- 2D transform decomposed into 2 1D - operations (Stage 1 and Stage 2)
- Intermediate results stored in Transpose Memory
- Forward DCT - 8-bit unsigned input, 11-bit signed output
- Inverse DCT - 11-bit signed input, 8-bit unsigned output
- Continuous streaming - one sample per cycle processing capability

Spartan-II E DCT/IDCT Solution - Performance



LogiCore Implementation

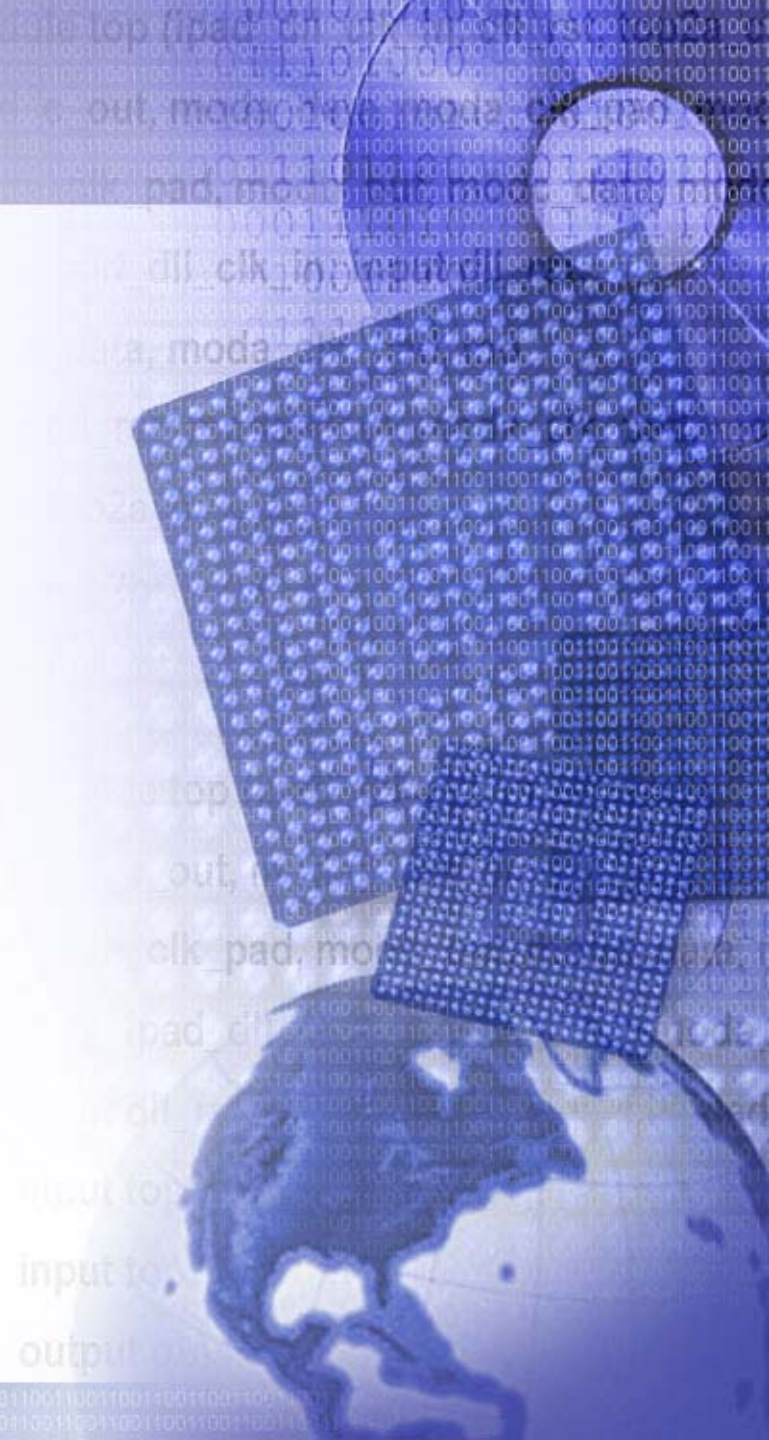
Target Device	Spartan-II E xc2s200E-7	Virtex-E xcv200e-8	Spartan II xc2s150-6
<i>Speed</i>	75 MHz (est.)	80 MHz	71.4 MHz
<i>SDTV (27 MHz) Time Multiplexed Channels</i>	3	3	2
<i>HDTV (75 MHz) Time Multiplexed Channels</i>	1	1	N/A
<i>Size (Slices)</i>	1759	1759	1728

Innovation by

AMPHION™



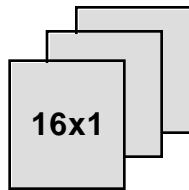
Memory Controllers and Interface



Spartan-II E Memory Solutions

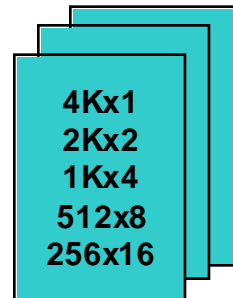


Distributed RAM



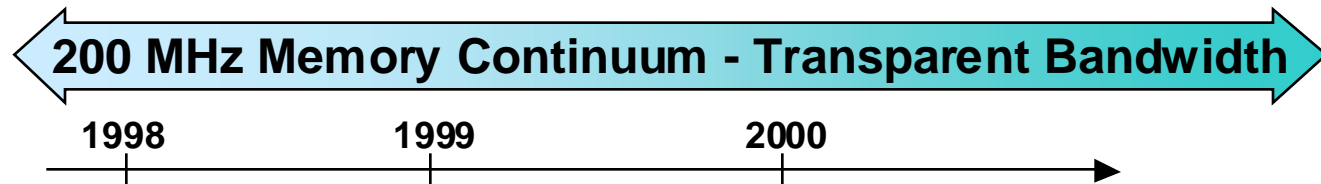
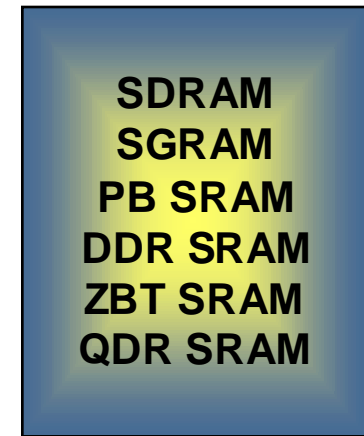
DSP Coefficients
Small FIFOs

Block RAM



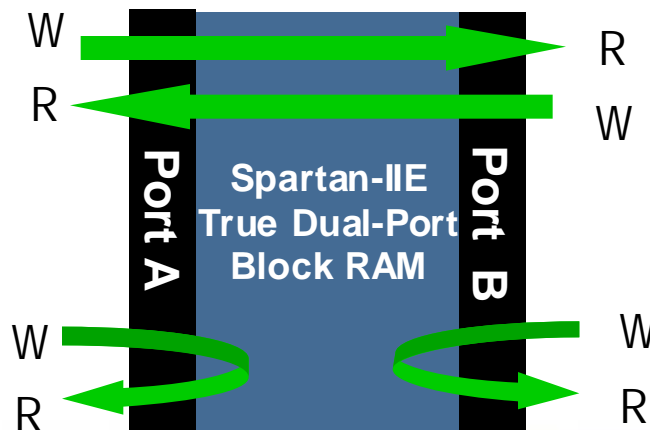
Large FIFOs
Video Line Buffers
Cache Tag Memory

External Memory Interface



Spartan-II E Block RAM

- True Dual-port Static RAM - 4K bits
 - Independently configurable port data width
 - 4K x 1; 2K x 2; 1K x 4; 512 x 8; 256 x 16
 - Fast synchronous read and write
 - 2.5-ns clock-to-output with 1-ns input address/data setup



Data Flow	Spartan-II E
A to B	Yes
B to A	Yes
A to A	Yes
B to B	Yes

Spartan-IIE Memory Controllers

- Spartan-IIE FPGAs
 - Unique and extensive features, flexible architecture, low cost
- Memory controller for interface to different types of SRAM, DRAM & Flash memory
 - Xilinx provides FREE VHDL source code for implementing the memory controllers in Spartan-IIE

Memory Controller Reference Designs

- DRAM reference designs
 - 64-bit DDR DRAM controller
 - 16-bit DDR DRAM controller
 - SDRAM controller
- SRAM reference designs
 - ZBT SRAM controller
 - QDR SRAM controller
- Flash controller
 - NOR / NAND flash controller
- Embedded memory reference designs
 - CAM for ATM applications
 - CAM using shift registers
 - CAM using Block SelectRAM
 - Data-width conversion FIFO
 - 170MHz FIFO for Virtex
 - High speed FIFO for Spartan-II

These Reference Designs are Available for Immediate Download at the Memory Corner

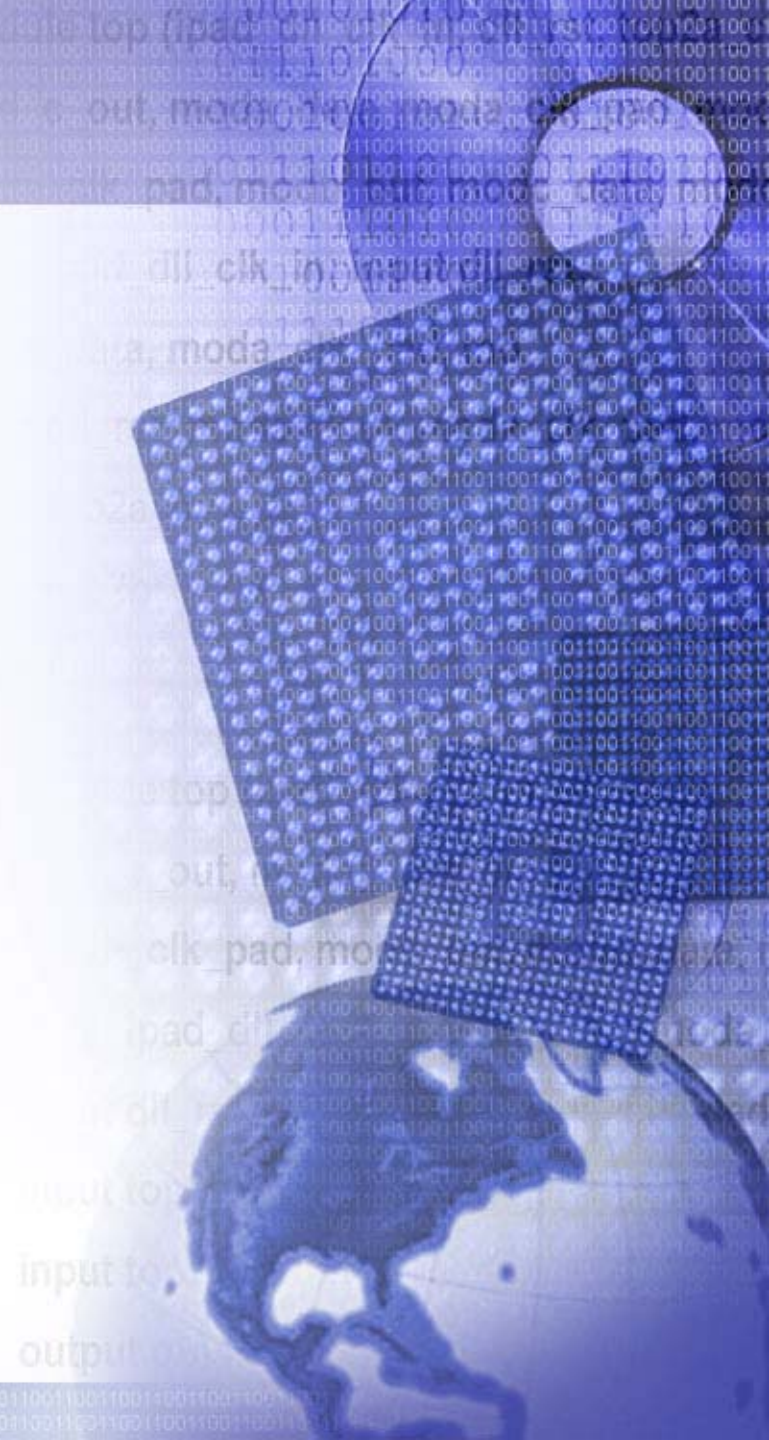
Memory Corner

- Collaboration between Xilinx and major memory vendors to provide comprehensive web-based memory solutions
 - Free reference designs (VHDL/Verilog)
 - SRAM, DRAM & embedded FPGA memory solutions
 - Data sheets, app notes, tutorials, FAQs, design guidelines





IEEE-1394



Bandwidth Requirements for Various Multimedia Applications

Application	Technique	Speed
Video Conference Quality	H.261	0.1 Mbps
Streaming Video	MPEG-4	5Kbps - 10Mbps
VCR Quality	MPEG-1	1.2 Mbps
Broadcast Quality	MPEG-2	2 -4 Mbps
Studio Quality Digital TV	ITU-R 601	165 Mbps
DVD/Studio Quality TV	MPEG-2	3-6 Mbps
HDTV	CD-DA	2 Gbps
HDTV	MPEG-2	25 -34 Mbps
Streaming Audio	MPEG Layer 3 (MP3)	32 -320 Kbps
Consumer CD-Audio	CD-DA	1441 Kbps
Consumer CD-Audio	MPEG with FFT	192 -256 Kbps
Sound Studio Quality	MPEG with FFT	384 Kbps
Dolby AC-3	5.1 Channels	640 Kbps
Telephone (Standard)	G.711 PCM	64 Kbps
Telephone (Standard)	G.721 ADPCM	32 Kbps
Telephone (Lower)	GSM	13 Kbps
Telephone (Lower)	CELP	5 -7 Kbps
Broadband Access (DSL)	ADSL	1.5 - 9 Mbps
Broadband Access (Cable)	DOCSIS	2 Mbps

Require High Bandwidth Interconnectivity Solution

IEEE-1394 & Multimedia Industry

- 1394 is the lowest cost, digital interface available for audio/video applications
- New audio/video applications are the primary market for IEEE-1394
 - Digital Television (DTV)
 - Multimedia CDROM (MMCD)
 - Home Networks
- IEEE-1394 has been accepted as the standard digital interface by the Digital VCR Conference

IEEE-1394 & Multimedia Industry

- The European Digital Video Broadcasters (DVB) have endorsed IEEE-1394 as their digital television interface
 - Several of these companies have proposed IEEE-1394 to the VESA (Video Experts Standards Association) as the digital home network media of choice
- The EIA 4.1 subcommittee has voted for IEEE-1394 as the point-to-point interface for digital TV, as well as the multi-point interface for entertainment systems
- The American National Standards Institute (ANSI) has defined Serial Bus Protocol (SBP) to encapsulate SCSI-3 for IEEE-1394

Why IEEE-1394?

- A hardware and software standard for transporting data at 100, 200, 400, or 800 megabits per second (Mbps)
- A digital interface
 - There is no need to convert digital data into analog and tolerate a loss of data integrity
- Physically small
 - The thin serial cable can replace larger and more expensive interfaces
- Inexpensive and Easy-to-use
 - There is no need for terminators, device IDs, or elaborate setup

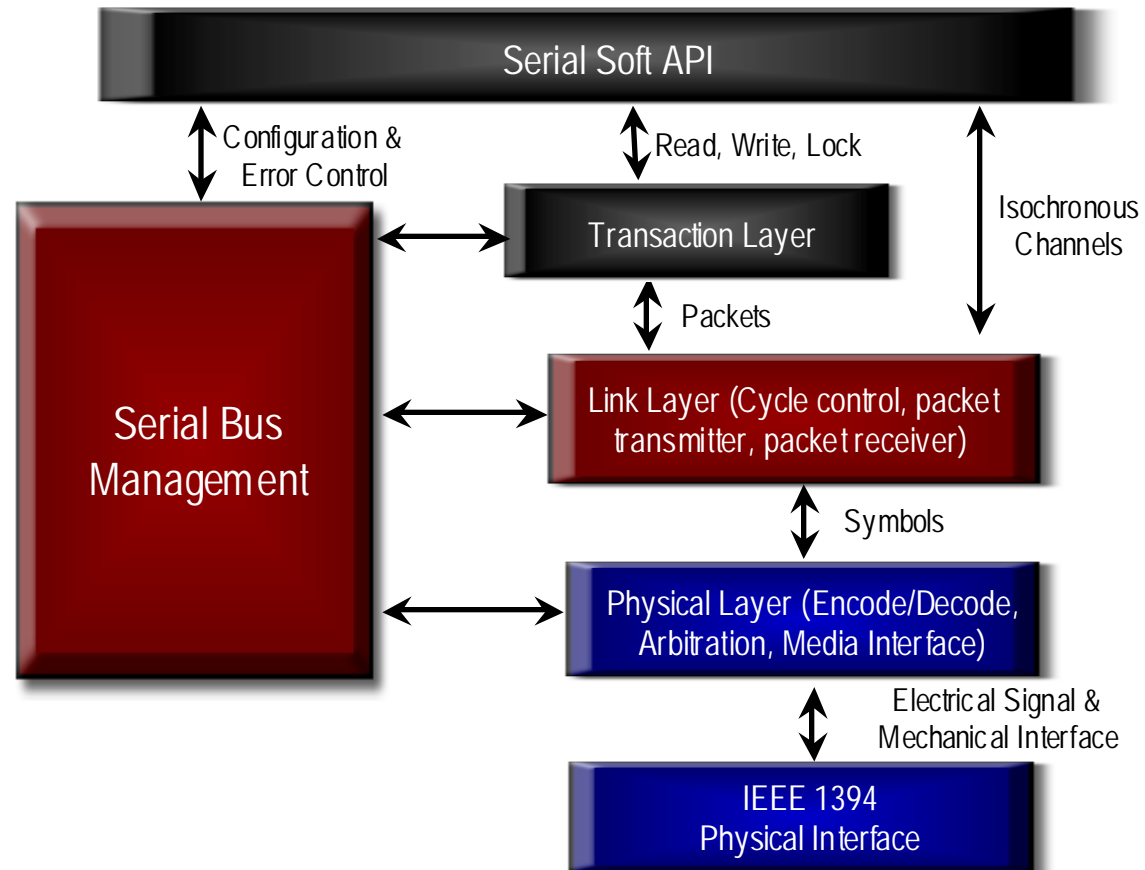
Why IEEE-1394?

- Hot pluggable
 - Users can add or remove 1394 devices with the bus active
- Scalable architecture
 - May mix 100, 200, and 400 Mbps devices on a bus
- Flexible topology
 - Support of daisy chaining and branching for true peer-to-peer communication
- Non-proprietary
 - There is no licensing problem to use for products

Audio/Video Digital Interface of Choice!



IEEE 1394 Protocol Stack



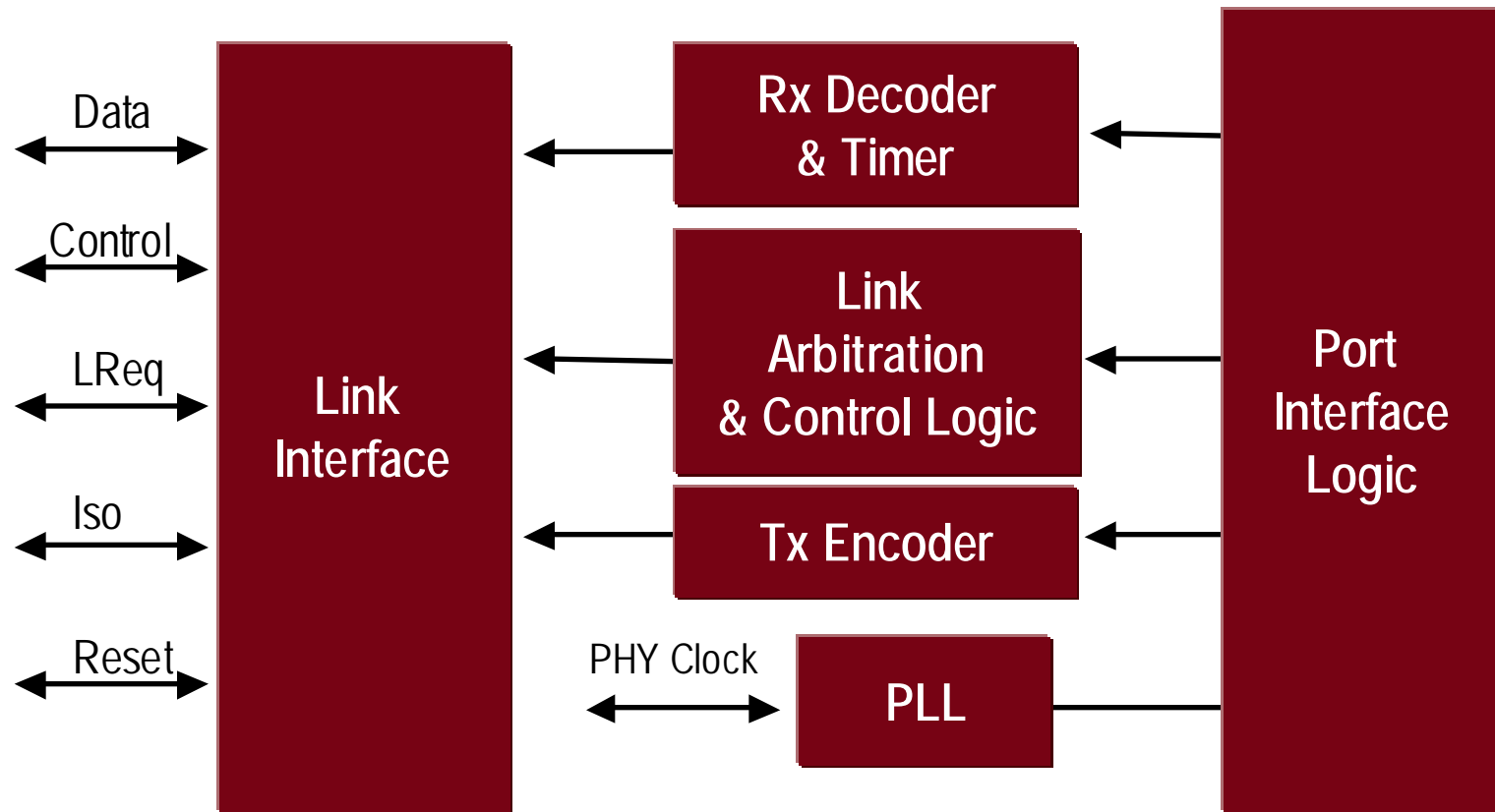
Legend for components:

- Digital
- Memory
- Mixed Signal
- μP or μC
- Programmable
- IP Block

1394 PHY Layer

- The physical layer provides the initialization and arbitration services
 - It assures that only one node is sending data at a time
- The physical layer of the 1394 protocol includes:
 - The electrical signaling
 - The mechanical connectors and cabling
 - The arbitration mechanisms
 - The serial coding and decoding of the data being transferred or received
 - Transfer Speed detection

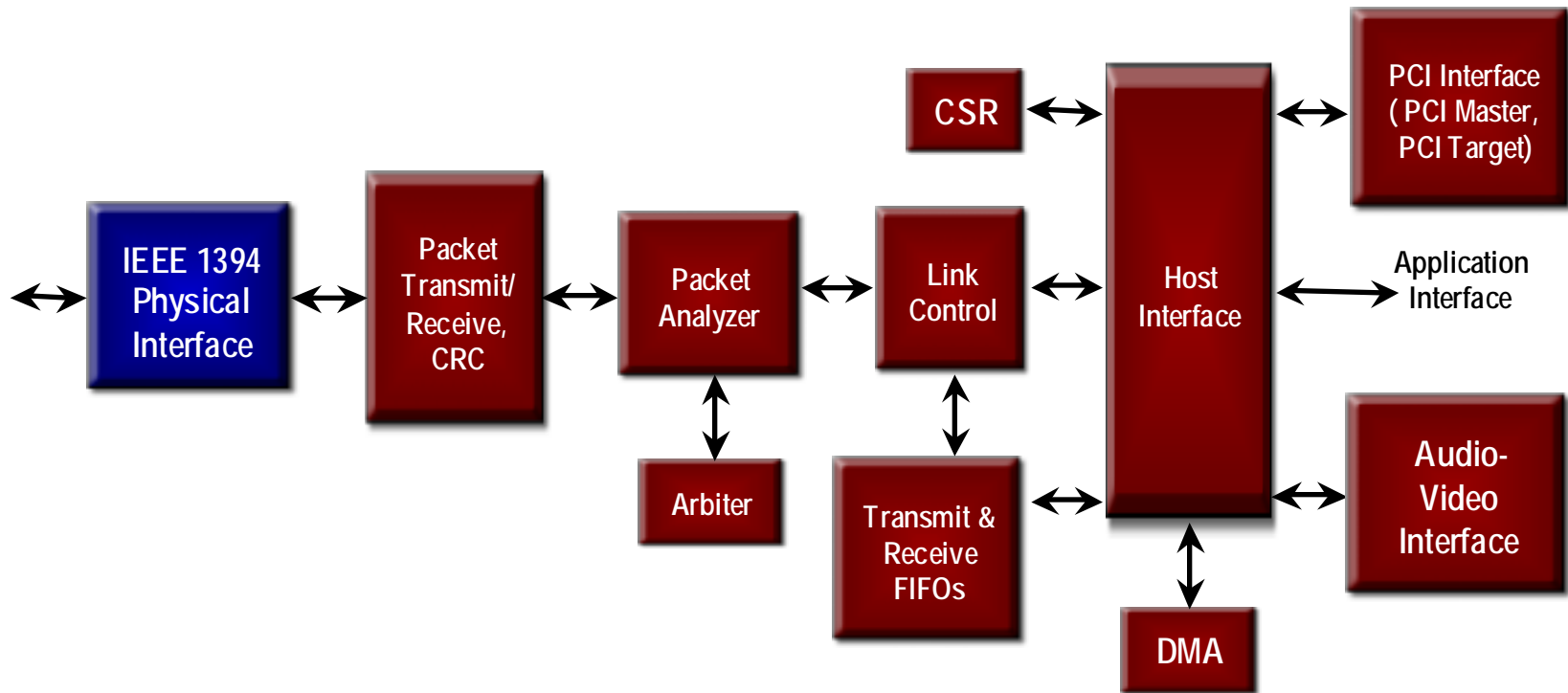
1394 PHY Layer



Link Layer

- Gets data packets on and off the wire
- Does error detection and correction
- Does retransmission
- Handles provision of cycle control for isochronous channels
- The link layer supplies an acknowledged datagram to the transaction layer
 - A datagram is a one-way data transfer with request confirmation

Link Layer

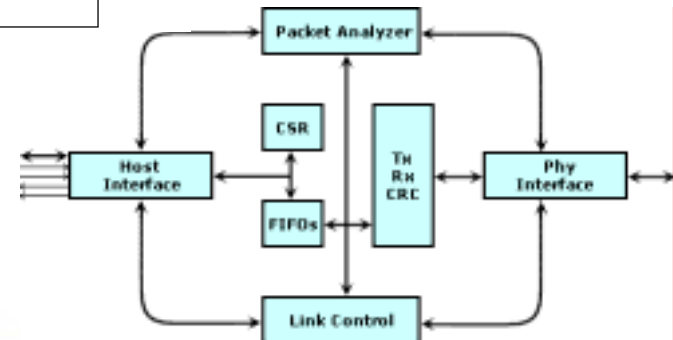
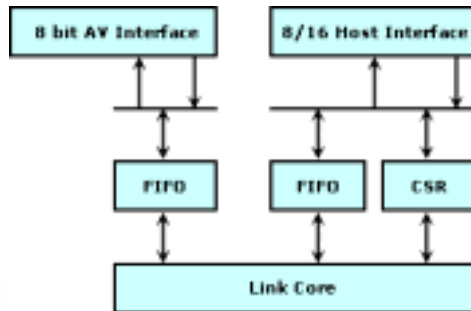
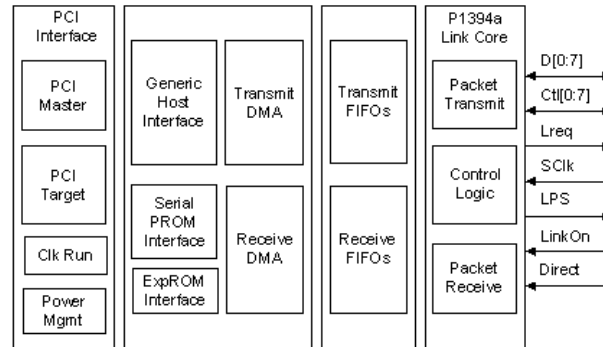
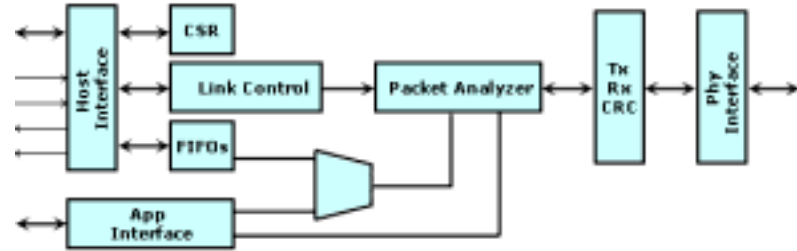
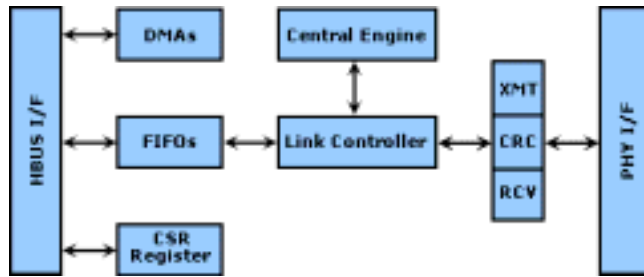


Xilinx FPGAs are ideal for implementing Link Layer Functionality



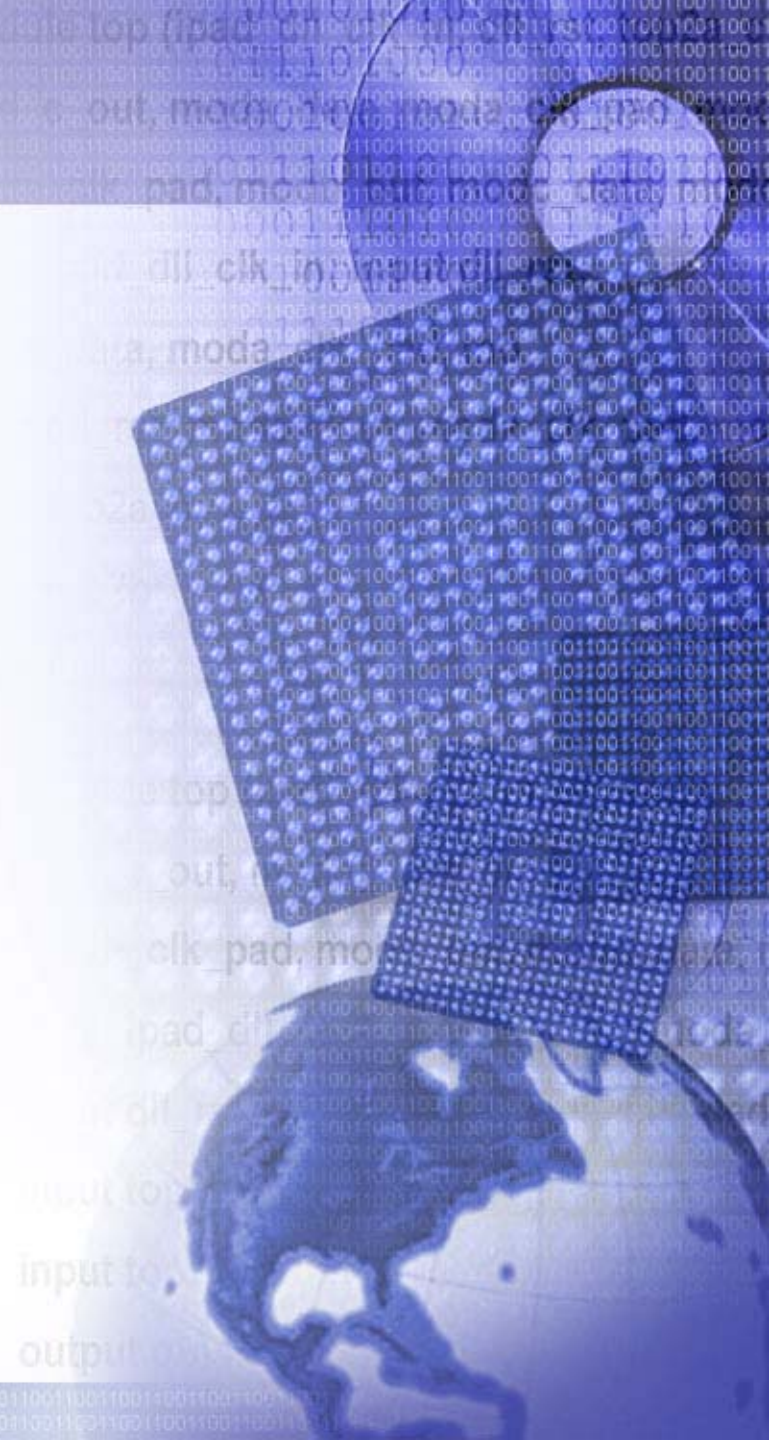
Link Controller IP - Xilinx

Enabled Differentiation





DVI



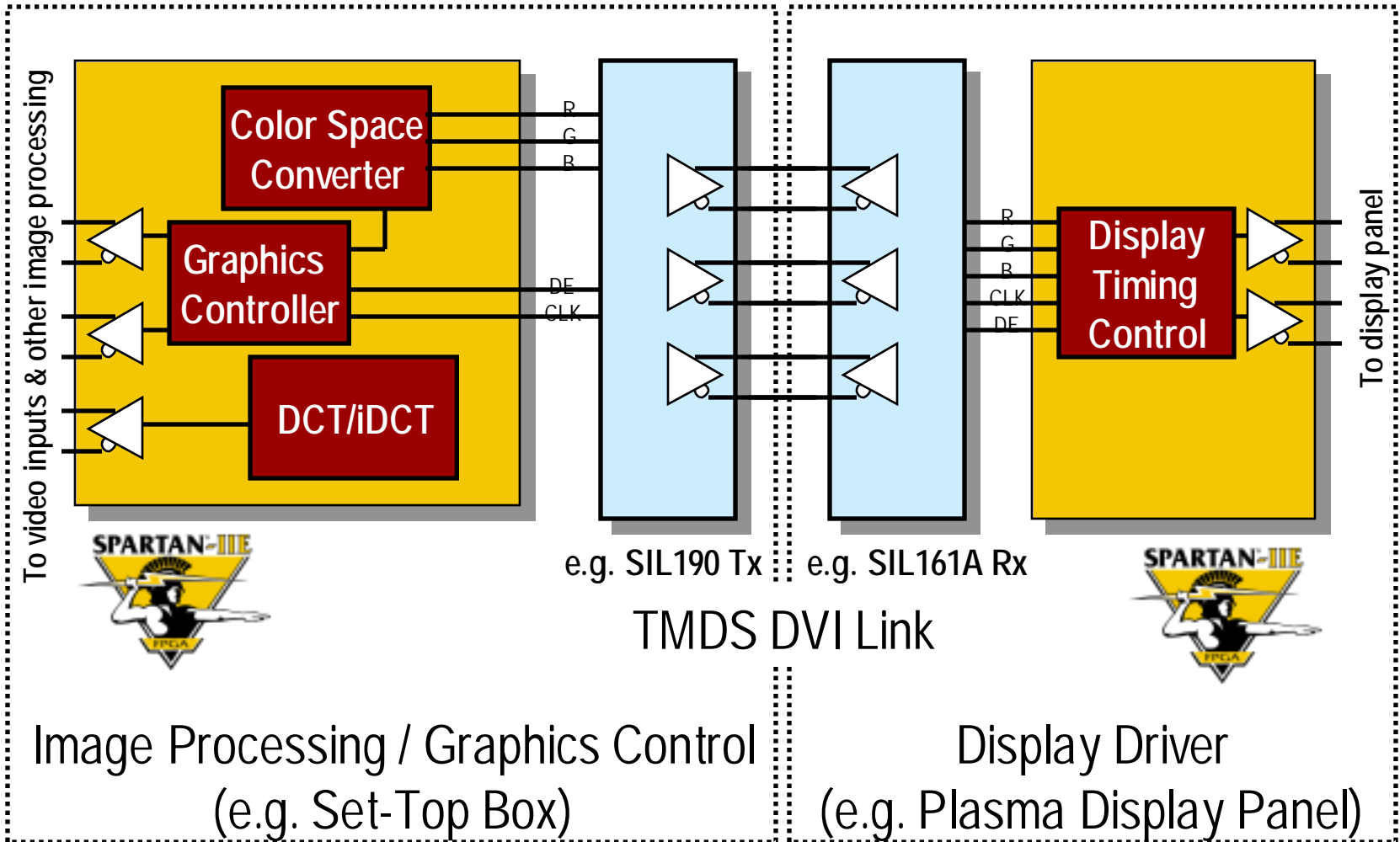
DVI Overview

- Interface to link digital graphics sources to digital displays
- One-way link supporting uncompressed HDTV signals
- Removes an unnecessary analog-digital-analog conversion step (current methods) - enables pure digital signal to display
- Based on Transition Minimized Differential Signaling (TMDS)
- Developed and promoted by the Digital Display Working Group (DDWG)

DVI & IEEE-1394

	Stream	Bit Rate	Architecture	Command & Control	Applications
IEEE-1394	Compressed MPEG-2 Transport	1394: 100, 200, or 400 Mbps, Scalable 1394b: 800 Mbps to 3.2 Gbps, Scalable	Peer-to-peer	Support for AV command & control	Storage, networking
DVI	Uncompressed baseband	Single link DVI: 4.9 Gbps Double link DVI: 9.9 Gbps	Point-to-point	No support for AV command & control	Digital interface between a graphics chip and a monitor

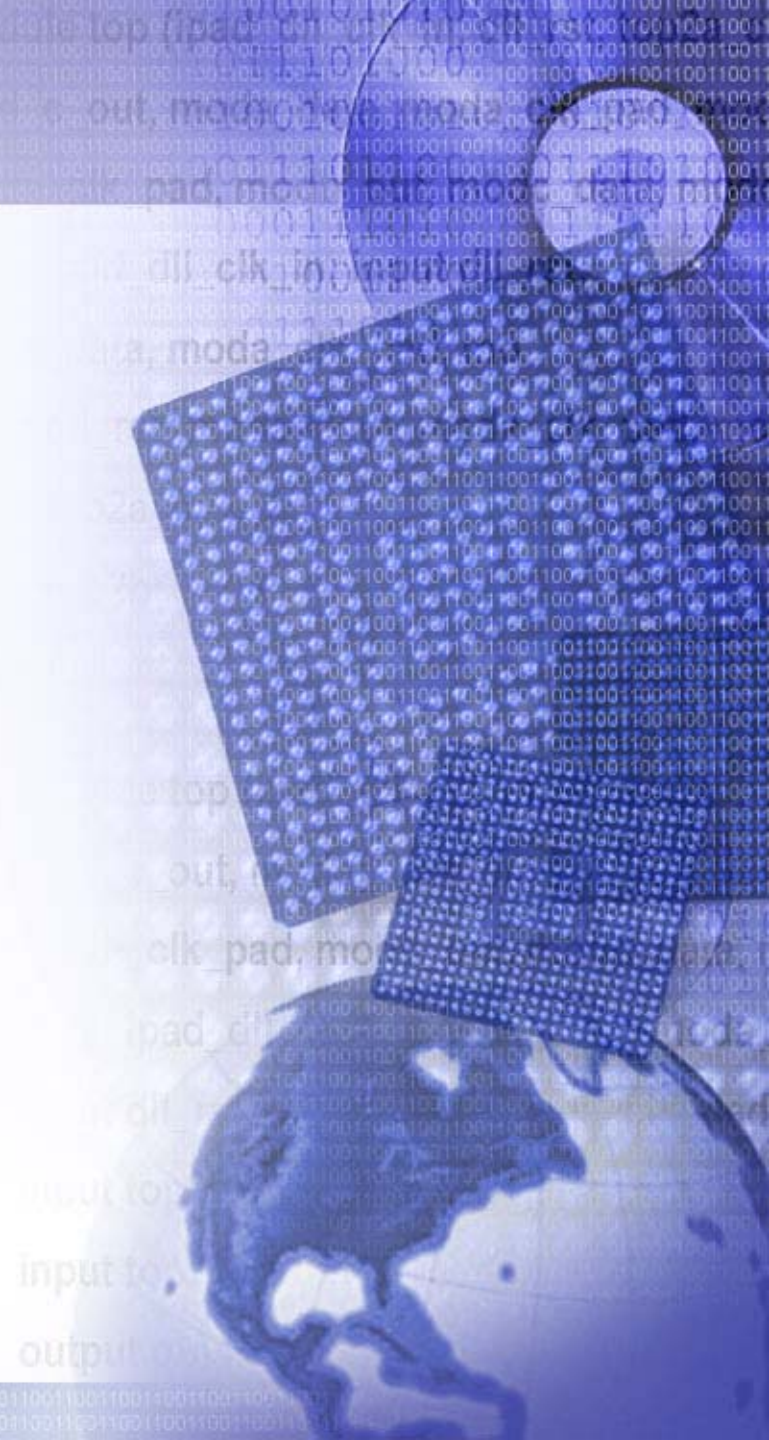
Spartan-II E in Example DVI System





USB 2.0

Universal Serial Bus



USB - Universal Serial Bus



Mice
Keyboards
Joysticks
Gamepads



Modems
Digital Cameras
Printers
Scanners
Microphones
Legacy Conversion



Mass Storage
Broadband
Home Networking
Residential Gateways
Digital Video/Audio
Legacy Conversion



Low-Speed
1.5 Mbps



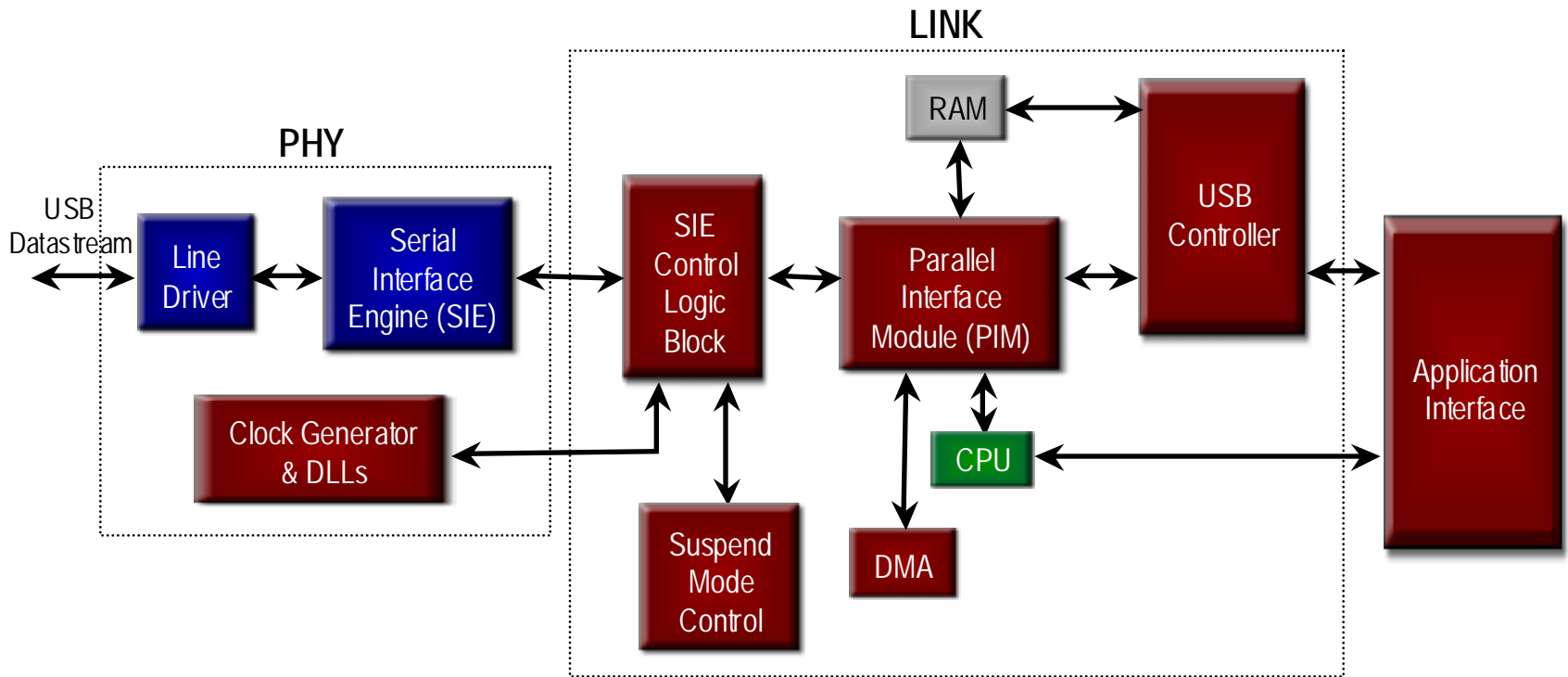
Full-Speed
12 Mbps



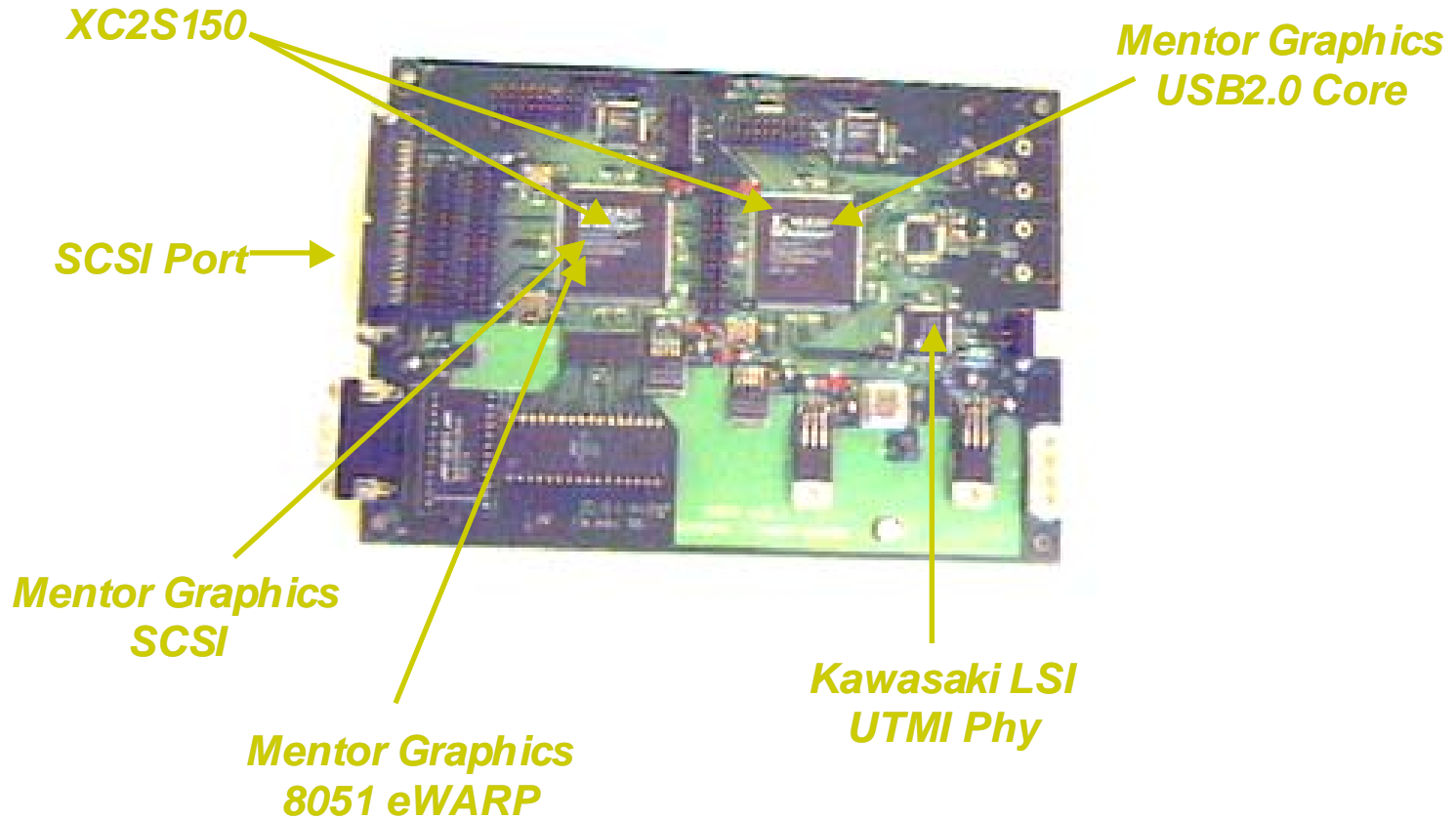
High-Speed
480 Mbps



USB 2.0 IP Core



The Xilinx USB 2.0 Solution

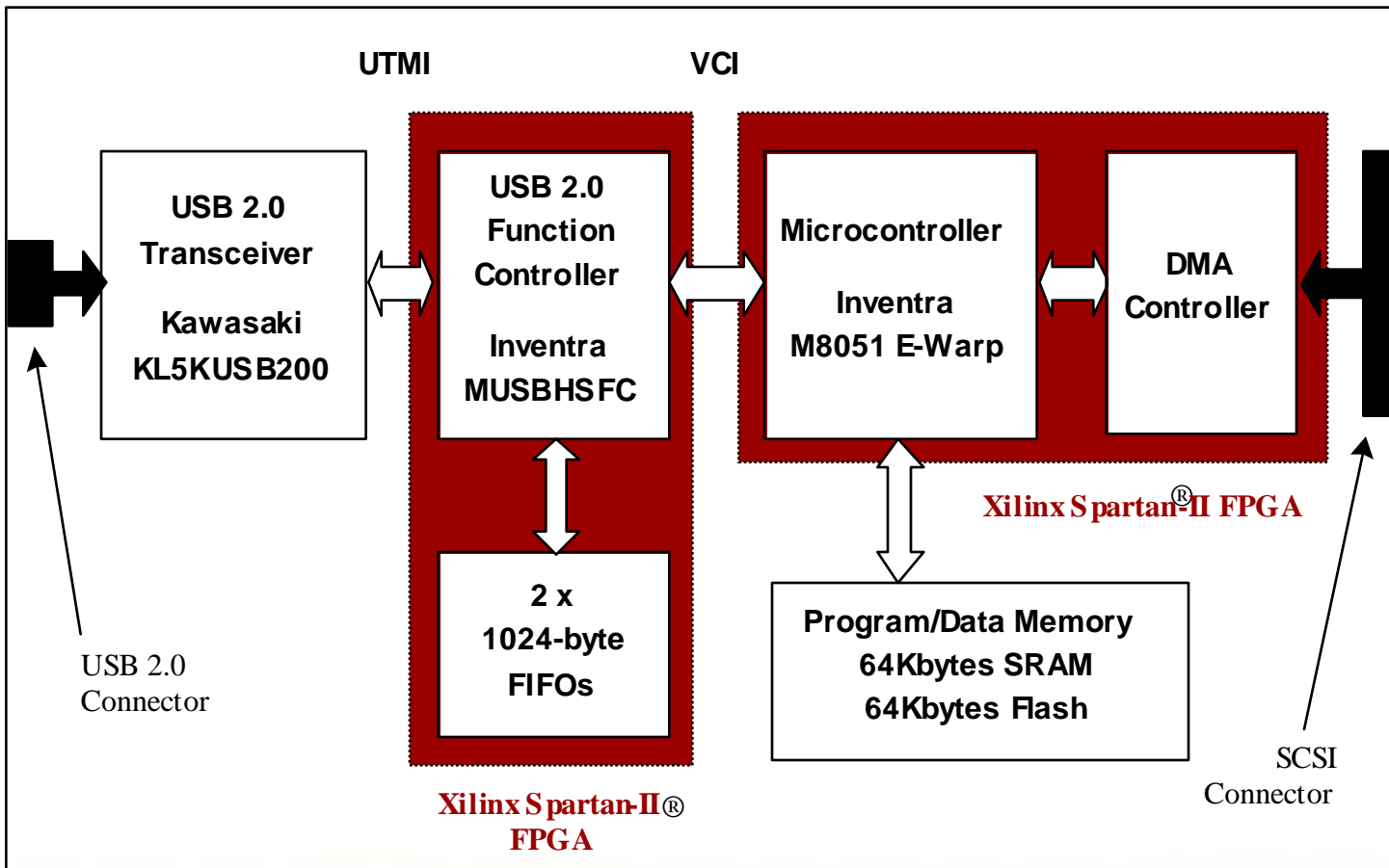


First USB2.0 Mass Storage Reference Design

The Xilinx USB 2.0 Solution

- Kawasaki LSI, Mentor Graphics and Xilinx have partnered and developed the industry's first UTMI-compliant USB 2.0 upgradable reference design
 - Provides a USB 2.0 to SCSI technology bridge, and can be used to provide end-to-end high-bandwidth data storage
 - For hard disk drives, CD writers, DVD ROMs, etc.
 - Flexible and upgradable USB 2.0 technology bridge to multiple home networking standards
 - Such as HomePNA, HomePlug, HomeRF, IEEE-1394, IEEE802.11b

USB 2.0 Mass Storage Reference Design Details

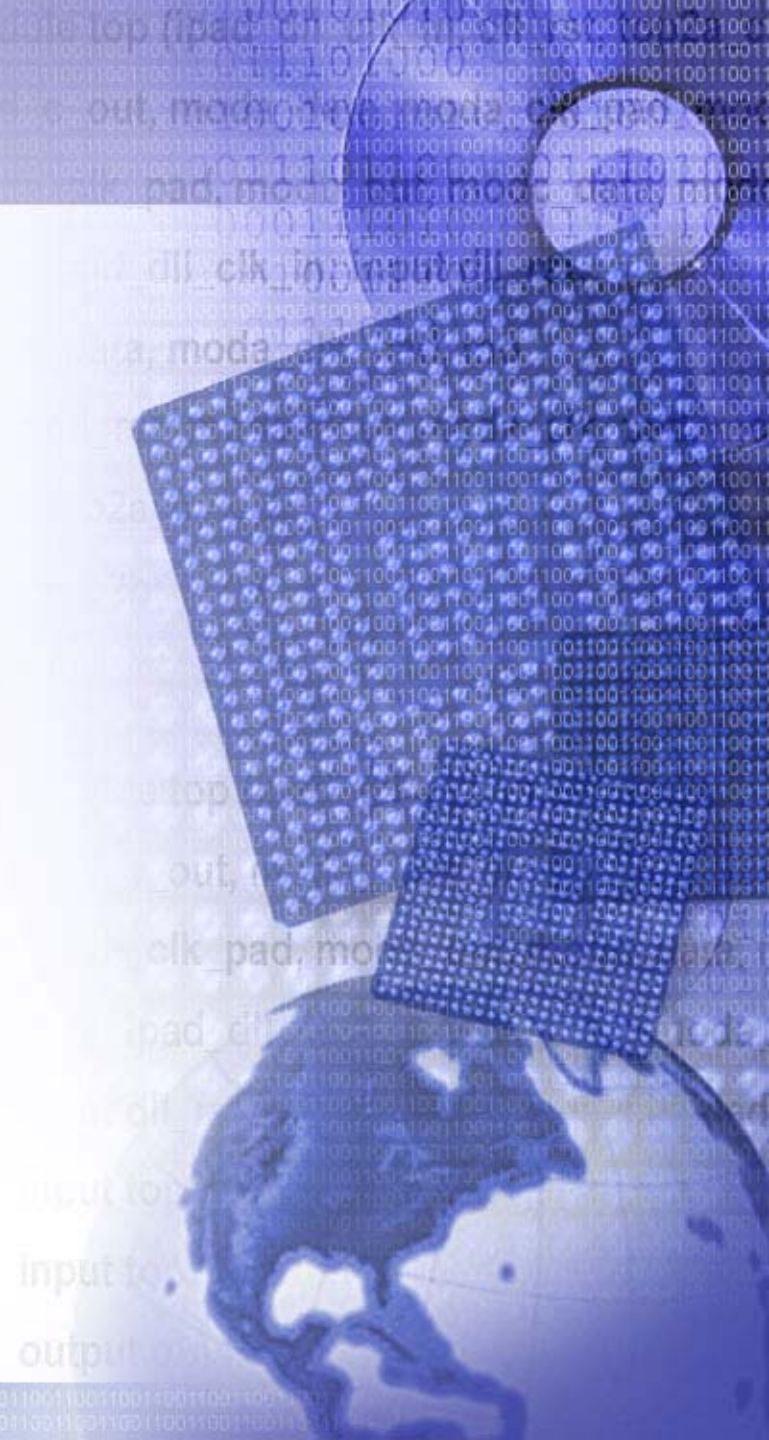


Solution - Features

- USB 2.0 Transceiver Macrocell Interface (UTMI) compliant physical layer from Kawasaki LSI
- High-speed (480Mbps) USB 2.0 functionality
- Mentor Graphics MUSBHSFC Fully Synthesizable Core Optimized for low-cost Spartan-II FPGAs
- Backward compatible with full-speed USB 1.1
- Future-proof, reprogrammable SIE
- Low-cost home networking solution



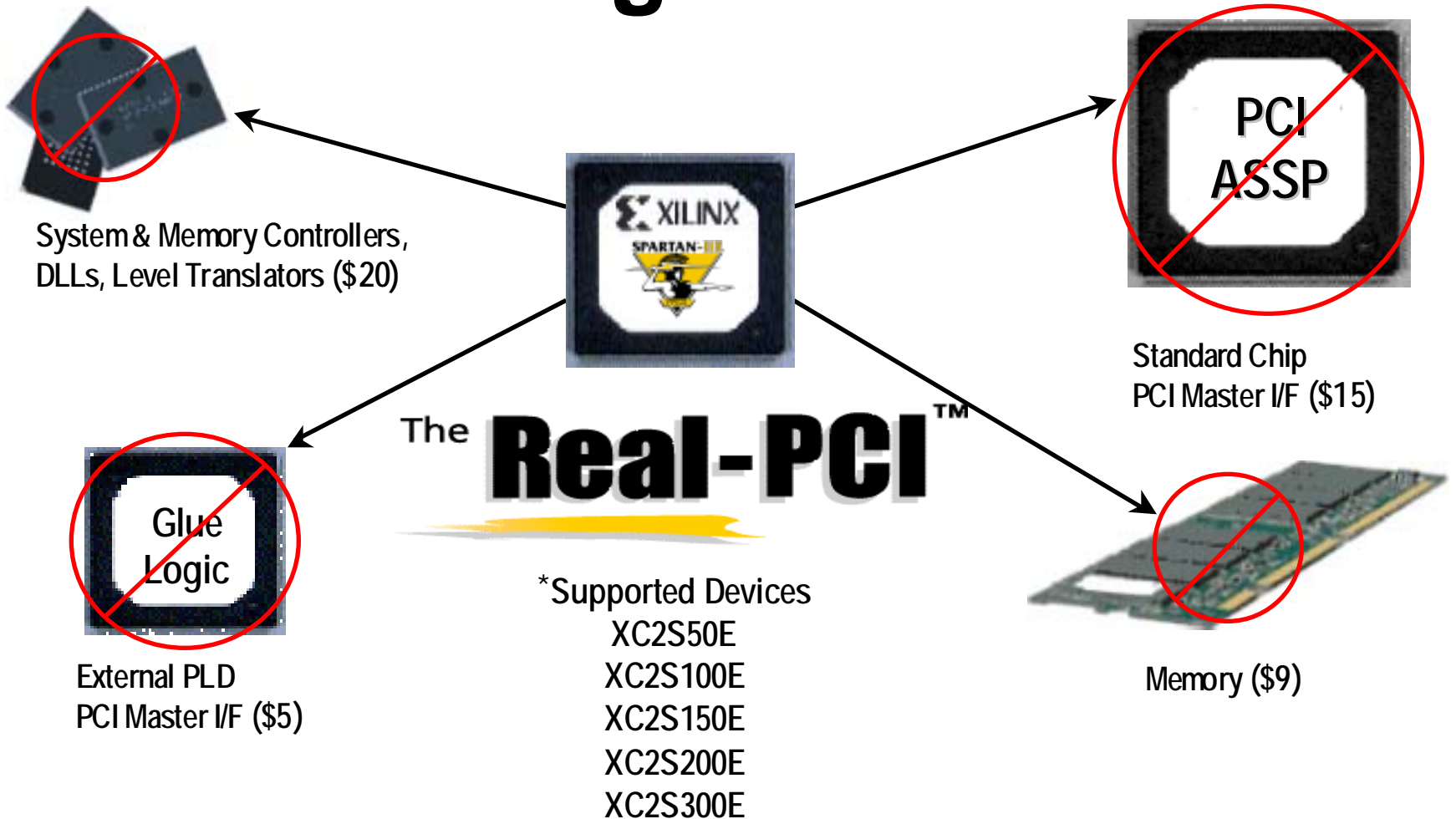
PCI



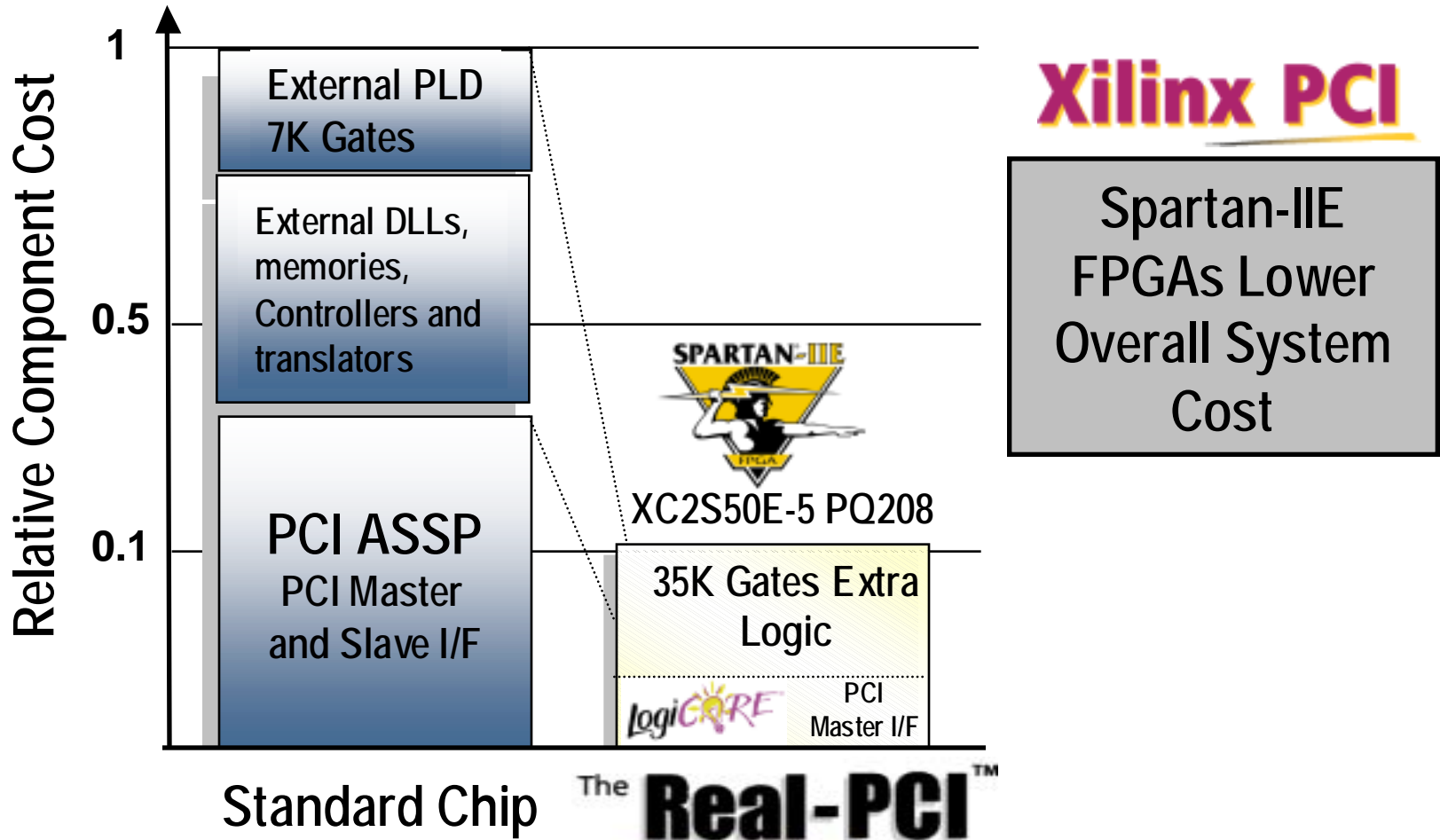
PCI - Concept

- PCI
 - Peripheral Component Interconnect
 - Originated in the PC industry
 - High performance bus that provides a processor independent data path between the CPU and high-speed peripherals
 - Robust interconnect mechanism developed to relieve the I/O bottlenecks

ASSP Replacement & Integration



PCI - A Successful Programmable Solution



Spartan-II E PCI Solutions

Spartan-II E Device	PCI Core	Speed	Available User Logic (system gates)	Available BlockRAM bits
2S50E	PCI32	33 MHz 66 MHz*	30-35K	32,768
2S100E	PCI32	33 MHz 66 MHz*	70-75K	40,960
2S150E	PCI32 PCI64	33 MHz 66 MHz	130-135K	49,152
2S200E	PCI32 PCI64	33 MHz 66 MHz	180-185K	57,344
2S300E	PCI32 PCI64	33 MHz 66 MHz	280-285K	65,536

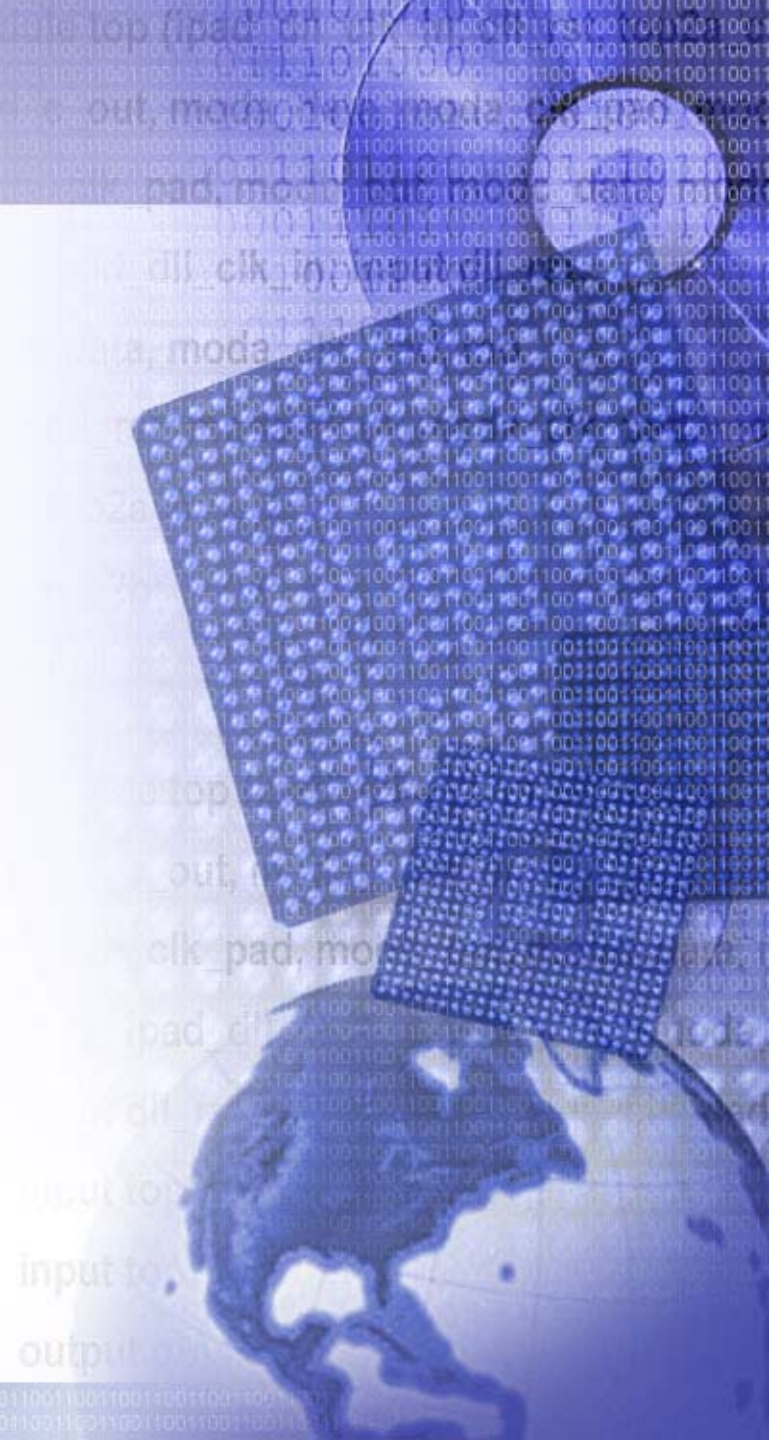
* PCI32: 66 MHz design available using Xilinx XPERTs or Design Services

Customer Benefits

- Reduces Cost Over PCI ASSPs
 - Cost savings of more than 50%
- Integrate and Replace System Functions
 - PLL/DLL clock management devices
 - SSTL-3/HSTL translators
 - Back plane logic and drivers
 - External Memory devices
 - System & caches controllers
- Significant Time-to-Market Advantage



Data Encryption



Copy Protection and Data Encryption

- Motivation for data encryption & cryptography
 - Data privacy (integrity & secrecy)
 - Authenticating the source of the information
- Several methods of data encryption exist
 - RSA (Rivest-Shamir-Adleman), Diffie-Hellman, RC4/RC5
 - Secure Hashing Algorithm (SHA), Blowfish
 - Elliptic Curves, ElGamal, LUC (Lucas Sequence)
 - DES (Data Encryption Standard) & Triple-DES (TDES)
- Xilinx Spartan-II E + IP Cores today provide
 - AES, DES, Triple DES, proprietary

Copy Protection Efforts

Copy-protection efforts at a glance

- CPTWG (a cross-industry forum among the movie, PC and consumer electronics industries): Five-year-old group meets regularly to propose and discuss technology issues related to DVD, including copy protection, encryption and watermarking.
- 5C (formed by Intel Corp., Hitachi Ltd., Sony Corp, Toshiba Corp. and Matsushita Electric Industrial Co.): Worked to develop Digital Transmission Content Protection (DTCP) to define a cryptographic protocol copy protection.
- 4C (initiated by Intel, IBM, Matsushita and Toshiba): Working on a Content Protection for Recordable Media and Pre-Recorded Media (CPRM/CPPM) specification that defines a renewable cryptographic method to protect entertainment content recorded on physical media.
- TCPA (formed by Compaq, HP, IBM, Intel and Microsoft): Focuses on developing a specification to deliver a set of hardware and operating-system security capabilities that customers can use to “enhance the trust and security in their computing environments,” the group said.

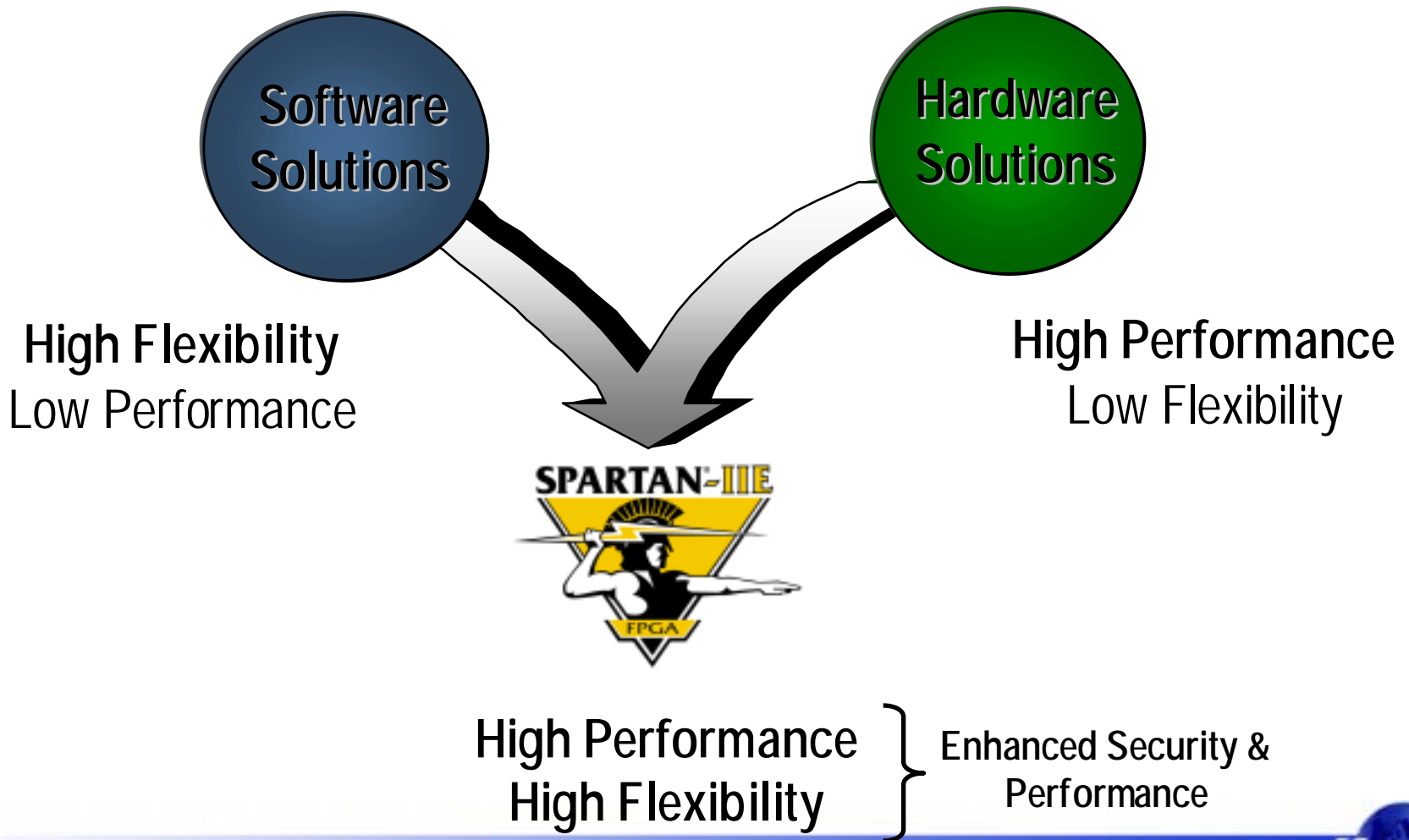
Courtesy: EETimes

Copy Protection

FPGAs Add Significant Value

- Security Systems Standards and Certification Act (Draft)
 - Calls for interactive digital devices to include security technologies certified by the U.S. Secretary of Commerce
- The bill becoming a law will prevent companies from shipping products without appropriate security
 - There is however no guidance on security schemes
 - A hardware based security implementation is preferred
- Lack of consensus between companies on the encryption schemes and their implementation is leading to chaos
- Copy protection for digital video products is in it's infancy and will be a significant area of focus

Spartan-III Advantages Over Hardware & Software Solutions



DES Concept

- The Data Encryption Standard (DES) algorithm
 - Developed by IBM Corporation
 - Most prevalent encryption algorithm
 - Adopted by the U.S. government in 1977, as the federal standard for encryption of commercial and sensitive, yet unclassified data
 - Is a block cipher
 - Encryption algorithm that encrypts block of data all at once, and then goes on to the next block
 - Divides 64-bit plaintext into blocks of fixed length (ciphertext)
 - Enciphers using a 56-bit secret internal key

Triple-DES Concept

- Triple-DES concept
 - More powerful and more secure
 - Equivalent to performing DES 3 times on plaintext with 3 different keys
 - TDES uses 2 or 3 56-bit keys
 - With one key, TDES performs the same as DES
 - TDES implementation: serial and parallel
 - Parallel improves performance and reduces gate count

Value Proposition in DES and TDES

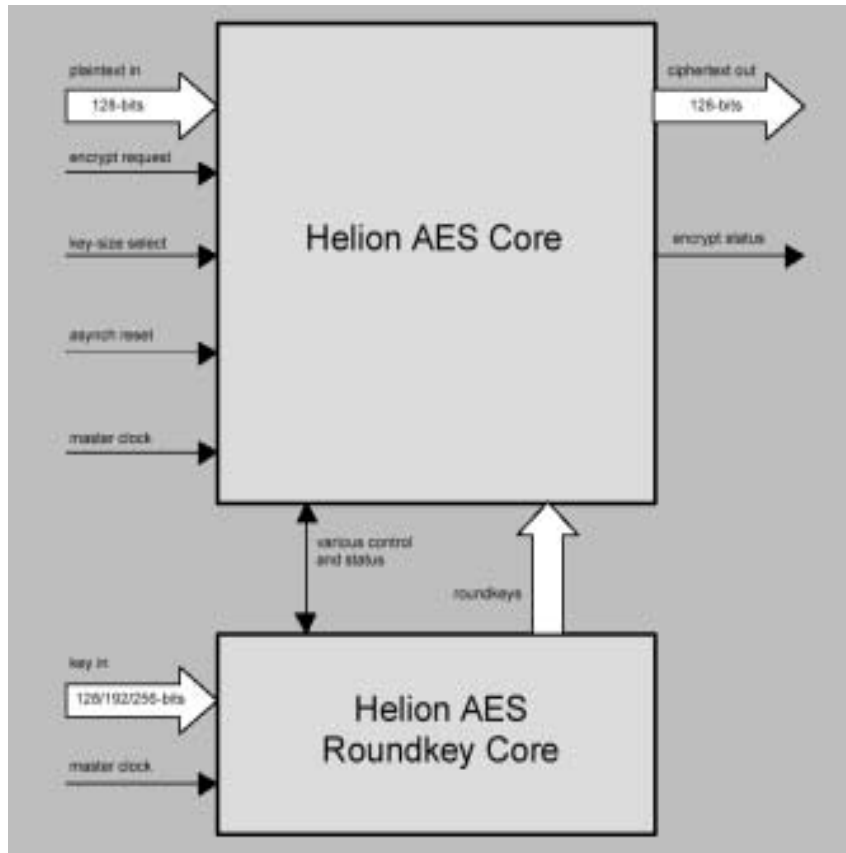
- High performance, many features and cost effective
- High scalability and flexibility
 - Reconfigurable fabric and Internet Reconfigurable Logic
- Embedded solutions
 - FPGA logic not used from DES/Triple-DES soft IP can be used for other IP solutions
 - DCT/IDCT and DES/TDES soft IP in a Spartan-II E FPGA can be used in multimedia and imaging applications
 - Increase the value proposition and reduces solution cost
- Spartan-II E can be programmed with broadcaster proprietary conditional access algorithms

AES (Rijndael)

- AES (Rijndael) chosen by the National Institute of Standards and Technology (NIST) as the cryptographic algorithm for use by U.S. government organizations to protect sensitive (unclassified) information
 - Rijndael block cipher named after its Dutch developers Vincent Rijmen and Joan Daemen
- Aimed to replace DES in the long run
 - DES has been successfully attacked using dedicated hardware and parallel computer networks
 - DES to be phased out
- Triple-DES expected to remain for foreseeable future

AES (Rijndael)

IP Solutions - Helion Technology



Features

- Implements AES (Rijndael) to latest NIST FIPS proposal
- 128-bit block-size, option of 128, 192 or 256-bit key-size (can be changed dynamically)
- Very fast operation – completes one AES round per master clock
- Supports data rates in excess of 10Gbps
- Separate encrypt and decrypt cores available
- Supports optional real-time roundkey generation
- All AES operating modes easily implemented (eg. ECB, CBC, OFB, CFB, MAC)
- Simple external interface
- Highly optimised for use in Xilinx FPGA technologies

Deliverables

- Target specific netlist or fully synthesisable RTL VHDL
- VHDL simulation model and testbench with FIPS test vectors
- User documentation

HELION



Spartan-IIE Encryption Solutions

- Spartan-IIE encryption solutions are NIST approved
- The programmable nature of these solutions allows easy customization based on end application requirement

	Spartan-IIE Solution			
	DES	Triple-DES	AES	AES
Device	2S100E-6	2S150E-6	2S100E-6	2S100E-6
CLB Slices	235	1611	358*	231**
Performance	94 MHz	48 MHz	82 MHz	82 MHz
Area Utilization	19.58%	93.22%	29.83%	19.25%
Key Size	56-bit	128-bit or two 64-bit	128/192/256-bit	128/192/256-bit

Note: Solution includes encryption, decryption and key generation

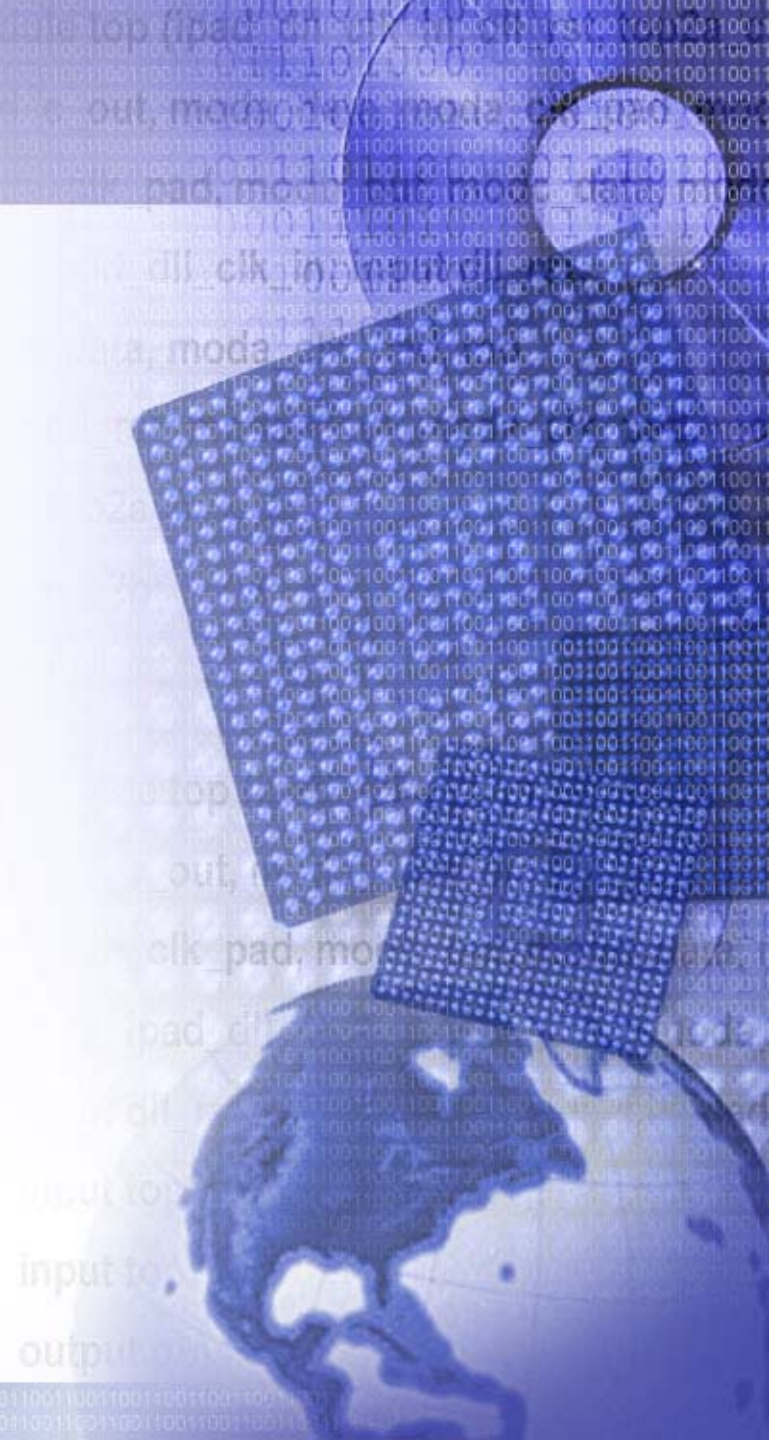
* 128-bit key implementation

** Key Generation offloaded to embedded μ C/ μ P



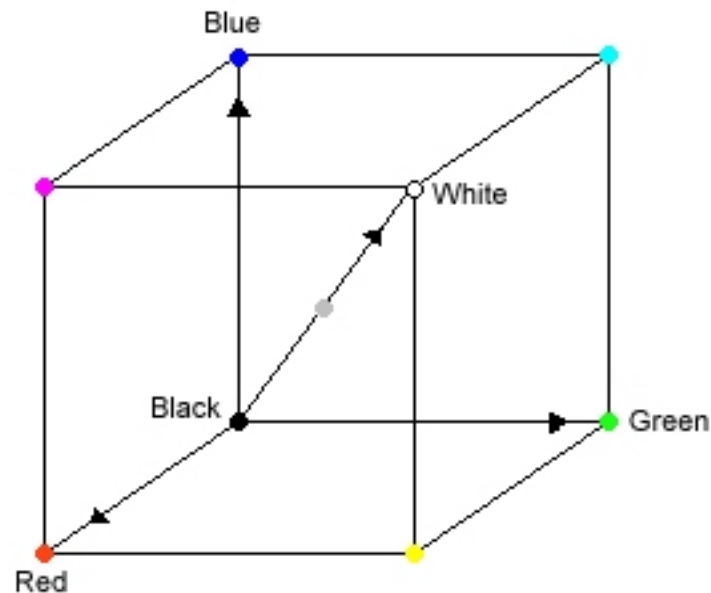


Color Space Conversion



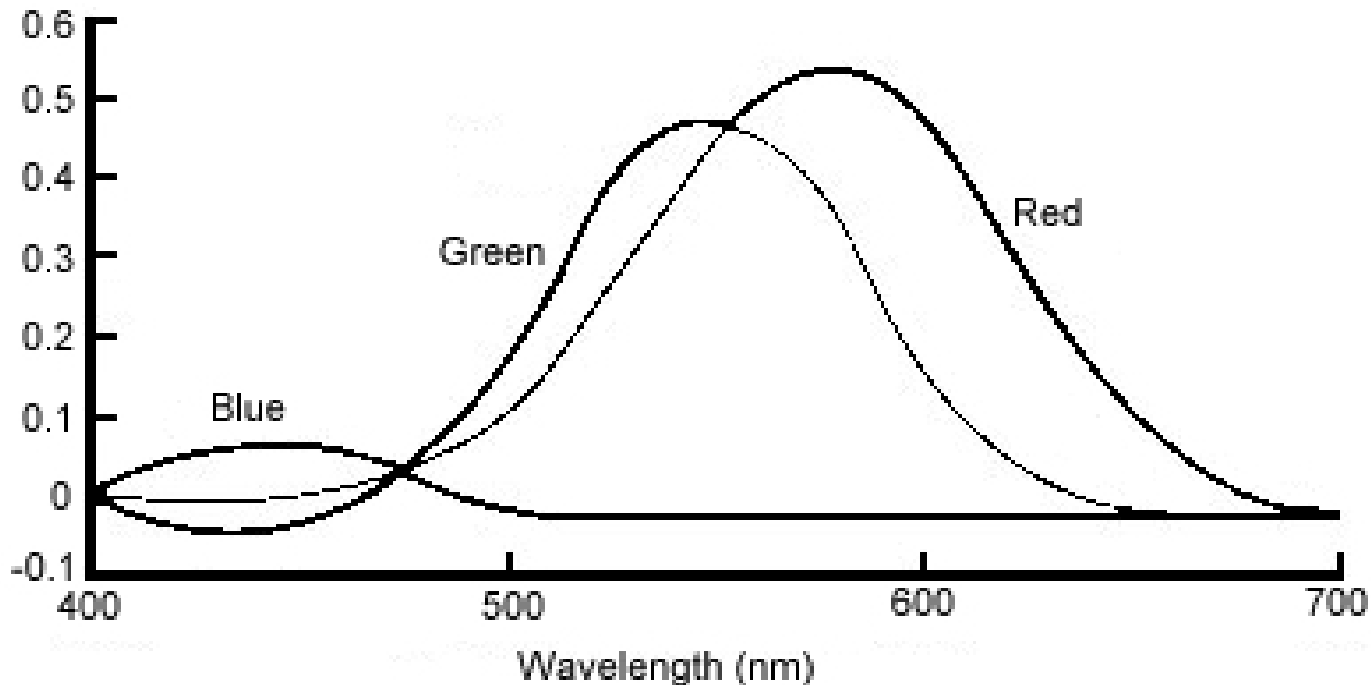
RGB Unity Color Space

- Mixtures of color components can be mapped into an RGB color space covering all variations from black ($0xR + 0xG + 0xB$) to white ($1xR + 1xG + 1xB$)



Spectral Response of Human Eye

- Green sensing cones in the human eye respond to most wavelengths in the light spectrum



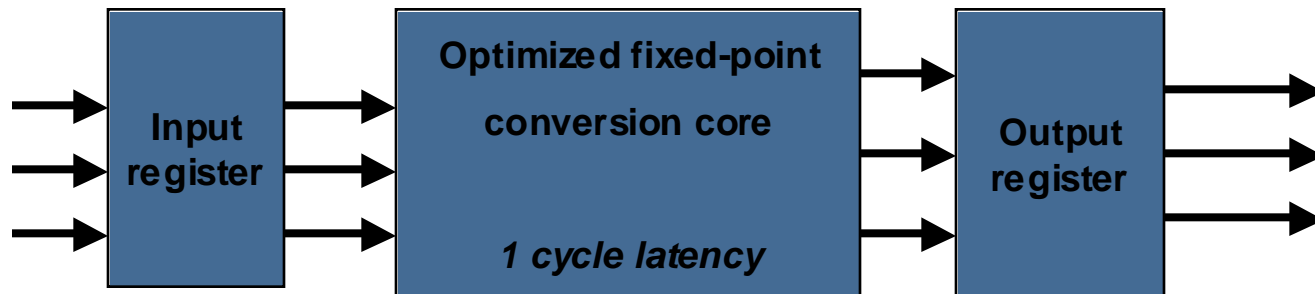
Luminance and Color Difference

- Pictures are almost always represented as pixels on final medium
 - Whether on printed paper or TFT, PDP & CRT displays
- Pixels can be represented with 3 full bandwidth analog RGB components
 - Huge storage and transmission bandwidth requirements for high resolution, large format displays (up to 200 terabytes during post-production)
- Human eye is more receptive to brightness than it is to color
 - Full resolution of human vision is restricted to brightness variations
 - Color detail resolution is about a quarter that of brightness variations
 - Green objects will produce more stimulus than red objects of the same brightness, with blue objects producing the least
- A brightness/luma signal (Y) can be obtained by adding RGB values together which are weighted by relative eye response

Luminance and Color Difference

- ITU CCR 601 says $Y = 0.299R + 0.587G + 0.114B$
- To save bandwidth, color difference signals are sent with luma rather than RGB
- Color difference possibilities
 - R-Y
 - B-Y
 - G-Y ← As G contributes most to Y, this signal would be small and most susceptible to noise
- Simple maths can be used to reconstruct signals at the display

Color Space Converter Structure



- Fully synchronous
- Registered input and output, 1 internal pipeline stage
- Low latency (3 cycles)
- Continuous processing
- One 3-color conversion every clock cycle
- Internal 10-bit precision for accuracy
- Rounded to 8-bit outputs

Cores Available

CCIR 601 Standard

- RGB2YCrCb
- $Y = 0.257 \times R' + 0.504 \times G' + 0.098 \times B' + 16$
- $Cr = 0.439 \times R' - 0.368 \times G' - 0.071 \times B' + 128$
- $Cb = -0.148 \times R' - 0.291 \times G' + 0.439 \times B' + 128$
- YCrCb2RGB
- $R' = 1.164 \times (Y - 16) + 1.596 \times (Cr - 128)$
- $G' = 1.164 \times (Y - 16) - 0.813 \times (Cr - 128) - 0.392 \times (Cb - 128)$
- $B' = 1.164 \times (Y - 16) + 2.017 \times (Cb - 128)$
- RGB2YUV
- $Y = 0.299 \times R' + 0.587 \times G' + 0.114 \times B'$
- $U = -0.147 \times R' - 0.289 \times G' + 0.436 \times B'$
- $V = 0.615 \times R' - 0.515 \times G' - 0.100 \times B'$
- YUV2RGB
- $R' = Y + 1.140 \times V$
- $G' = Y - 0.394 \times U - 0.581 \times V$
- $B' = Y - 2.032 \times U$



Color Space
Converter Lounge
www.xilinx.com/ipcenter

Xilinx Color Space LogiCore Solutions



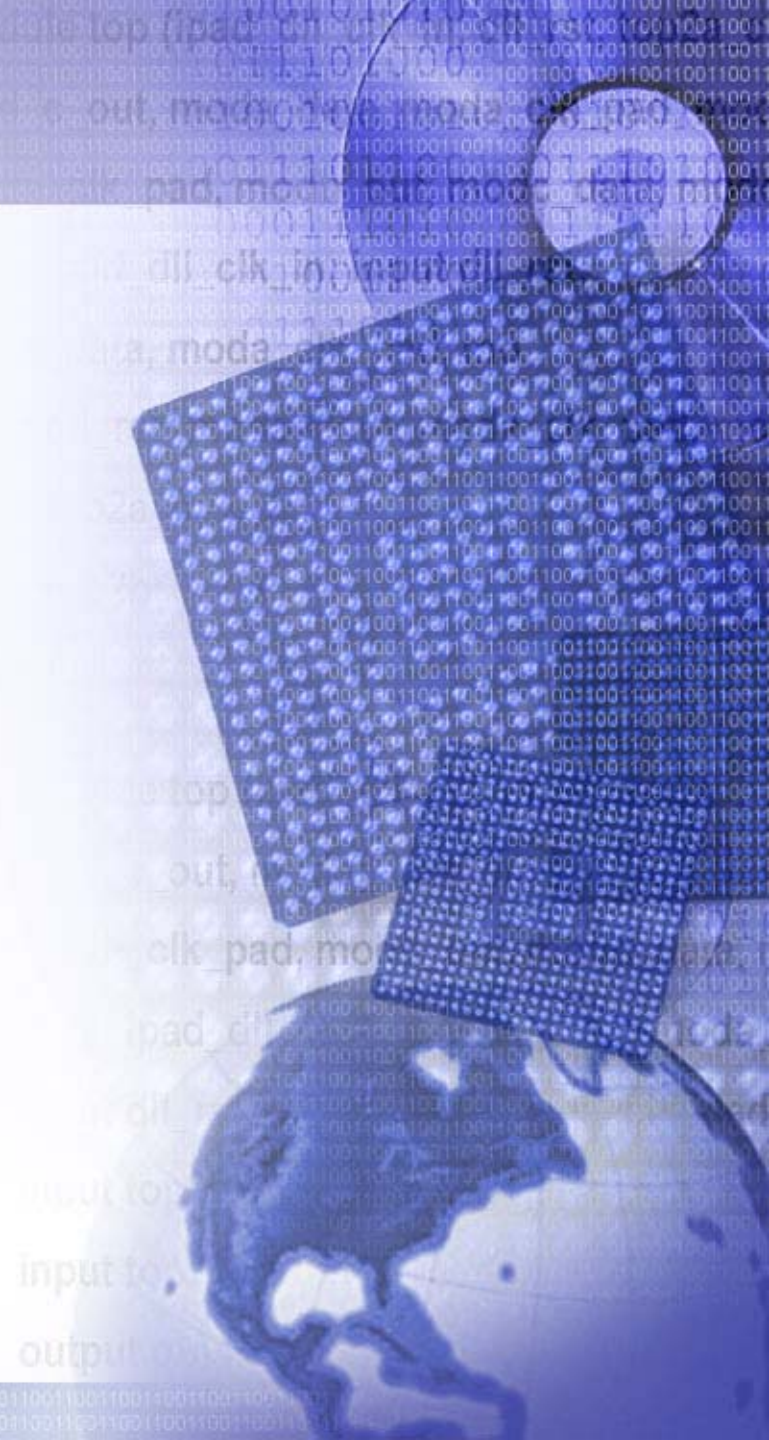
Product/Cores	YCrCb2RGB	RGB2YCrCb	YUV2RGB	RGB2YUV
Size: Virtex / Virtex-E	194 Slices	217 Slices	158 Slices	245 Slices
Synchronous	Full	Full	Full	Full
Supported Family	Spartan Spartan-II Spartan-II-E Virtex Virtex-E	Spartan-II Spartan-II-E Virtex Virtex-E	Spartan Spartan-II Spartan-II-E Virtex Virtex-E	Spartan-II Spartan-II-E Virtex Virtex-E
Latency	3 Clock Cycles	3 Clock Cycles	3 Clock Cycles	3 Clock Cycles
Performance: Spartan-II-E	>95 MHz	>90 MHz	>90MHz	>110MHz
SDTV (27 MHz) Time Multiplexed Channels	7 (Spartan-II-E)	3 (Spartan-II-E)	8 (Spartan-II-E)	3 (Spartan-II-E)
HDTV (75 MHz) Time Multiplexed	2 (Spartan-II-E)	1 (Spartan-II-E)	3 (Spartan-II-E)	1 (Spartan-II-E)
Cost	\$995	\$995	\$995	\$995

Xilinx Color Space Solutions

- LogiCORE Color Space Converters provide straight forward, accurate, high-performance conversion useable in a wide range of video/image applications
- More area efficient than existing cores
- Speeds ensure operation in all TV and HDTV applications
- Available through Xilinx Coregen



Clock Generation & Distribution



Clock Generation and Distribution

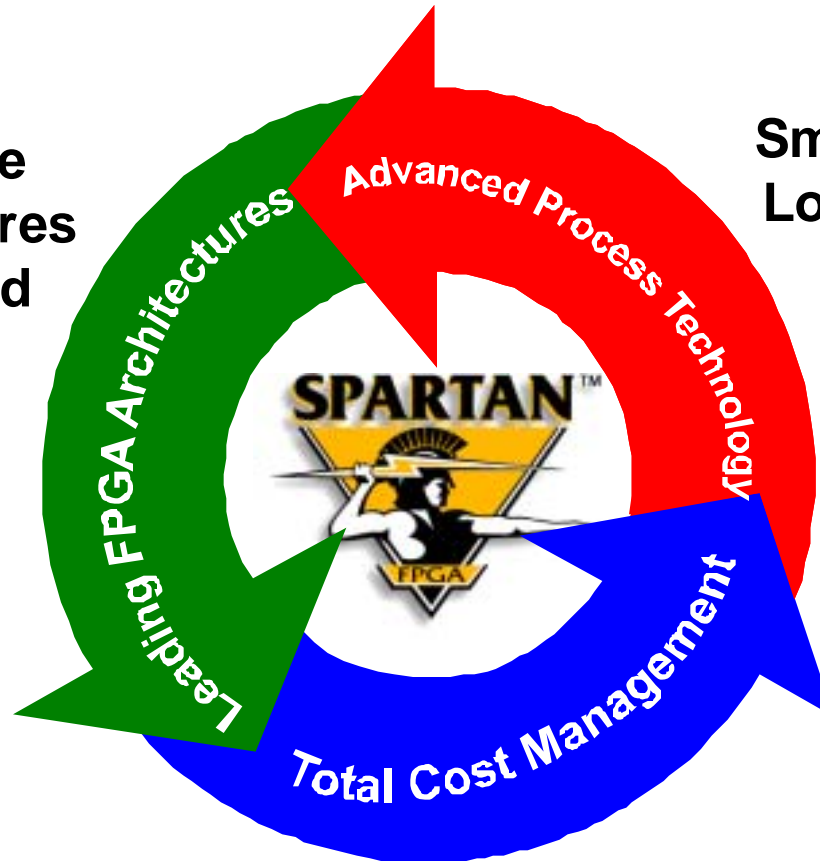
- Spartan-II/E DLL circuits provide full clock management solution
- Clock generation
 - Synthesizing many clocks from a single reference crystal or clock
- Clock buffering and distribution
 - Providing multiple copies of a single clock
 - SDRAM clocks
- Spread spectrum clocks for EMI reduction
 - DLL circuits allow tolerance for $\pm 2.5\%$ variance

Introducing the Spartan-II E FPGA Family



Xilinx Spartan Series FPGAs

High
Performance
System Features
Software and
Cores



Smallest Die Size
Lowest Possible
Cost

Low Cost Plastic Packages
Streamlined Testing

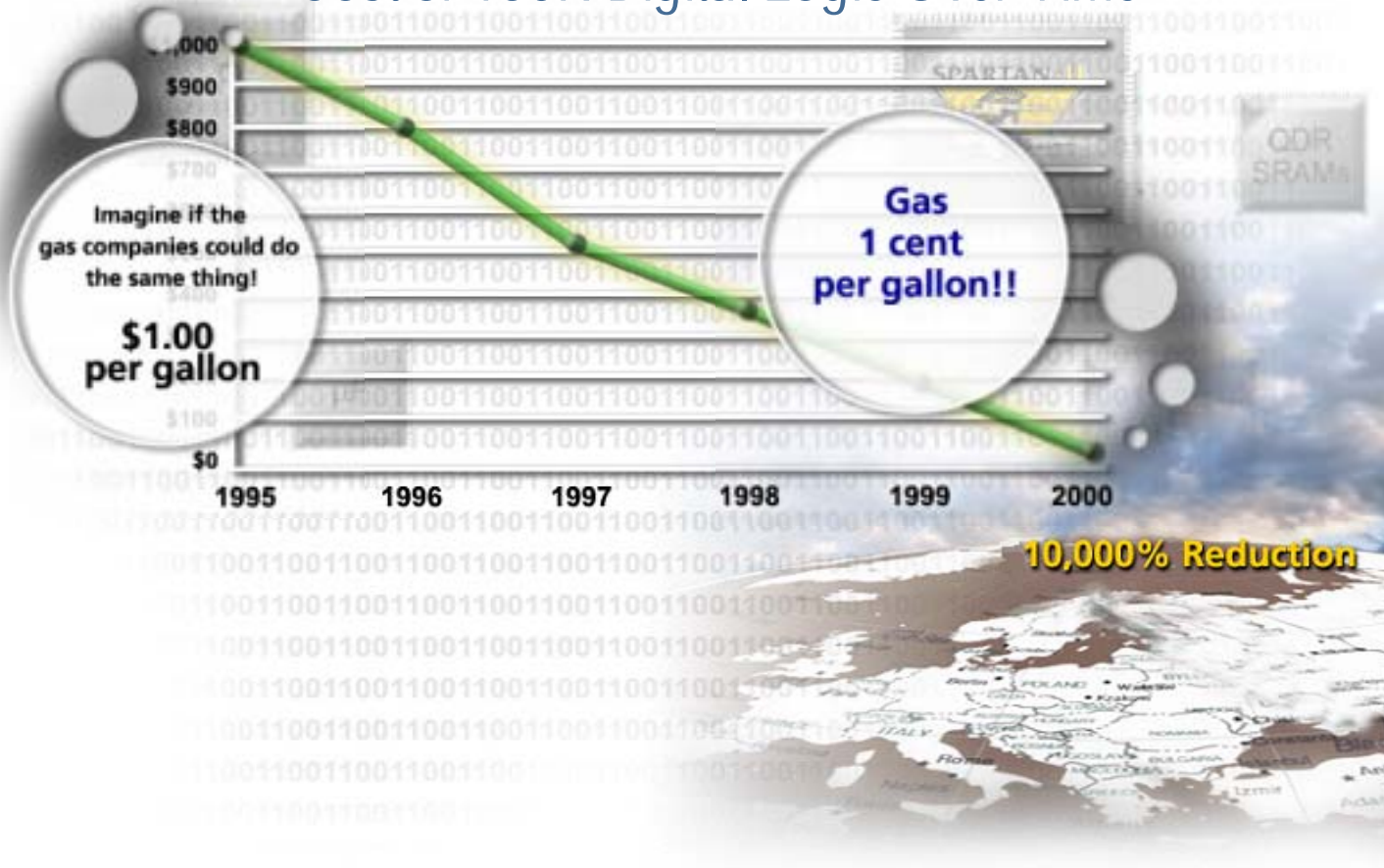
Spartan-II E FPGAs

A Natural Fit for Digital Convergence

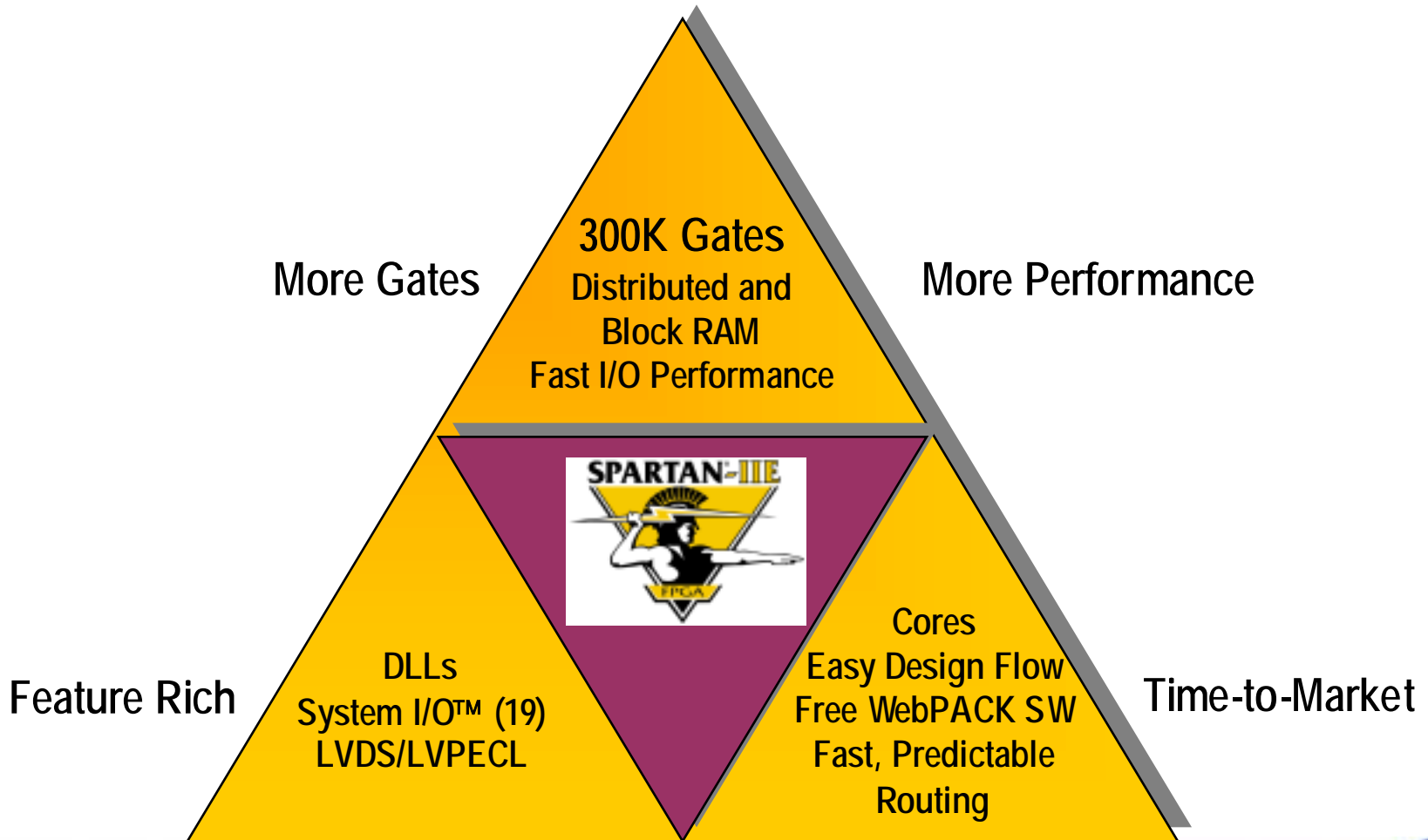
- Xilinx Solutions Allow Customers To Thrive in Chaos
 - FPGAs traditionally offer fast time-to-market
 - First to market, increases market share and revenue advantage
 - Xilinx Online offers reconfigurability in the field
 - Allows shipped product to support revisions to the spec
 - Enables unique opportunities to add value
 - Increases lifecycle revenue yield and hence, time-in-market
 - Enables rapid product proliferation
 - New designs can be quickly turned into derivatives
 - Superior lifecycle component logistics
 - Proven FPGA technology, software, test benches
- Spartan-II E FPGAs Are Cost Effective!!!

Taking the Cost Down...

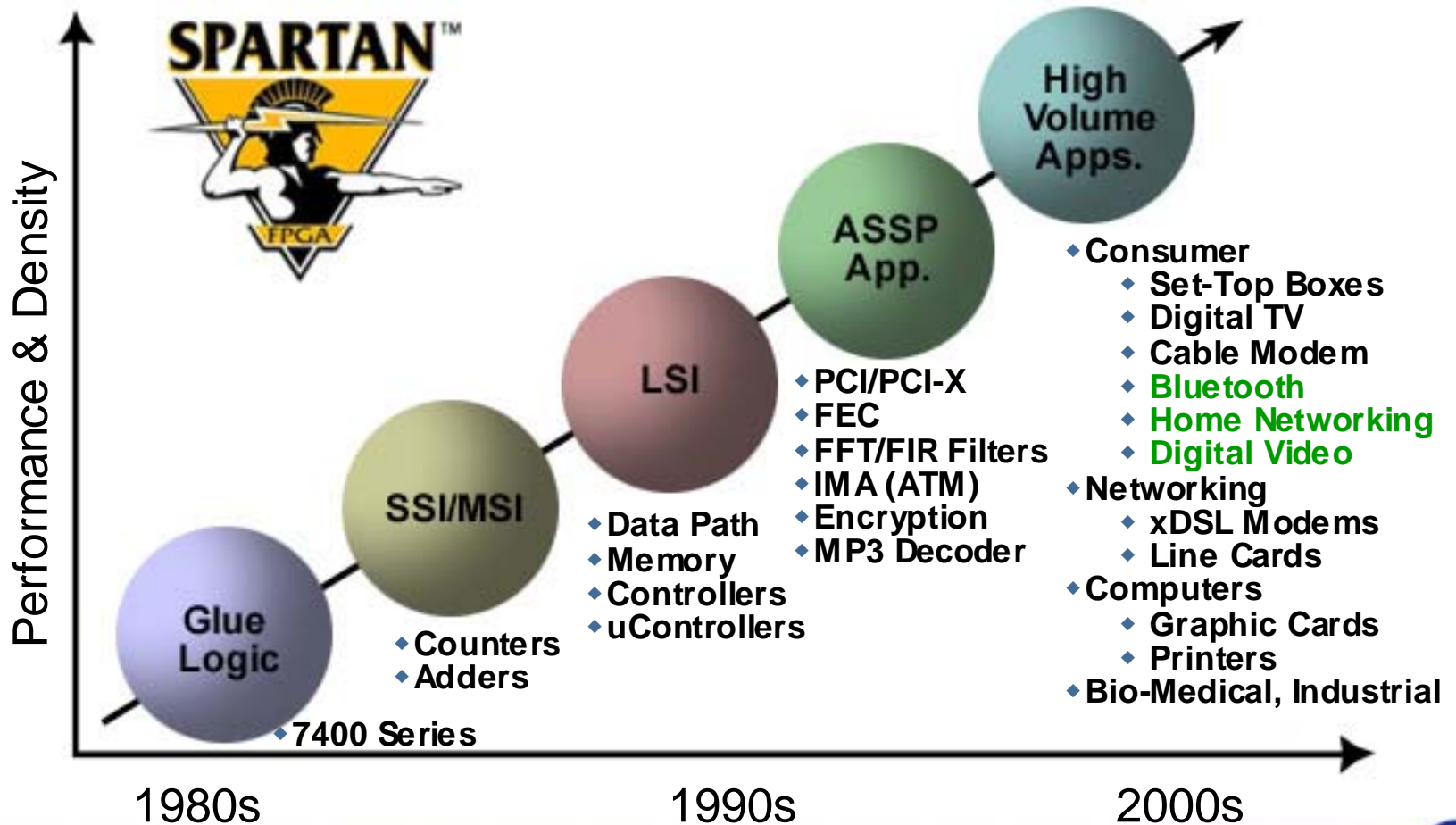
Cost of 150K Digital Logic Over Time



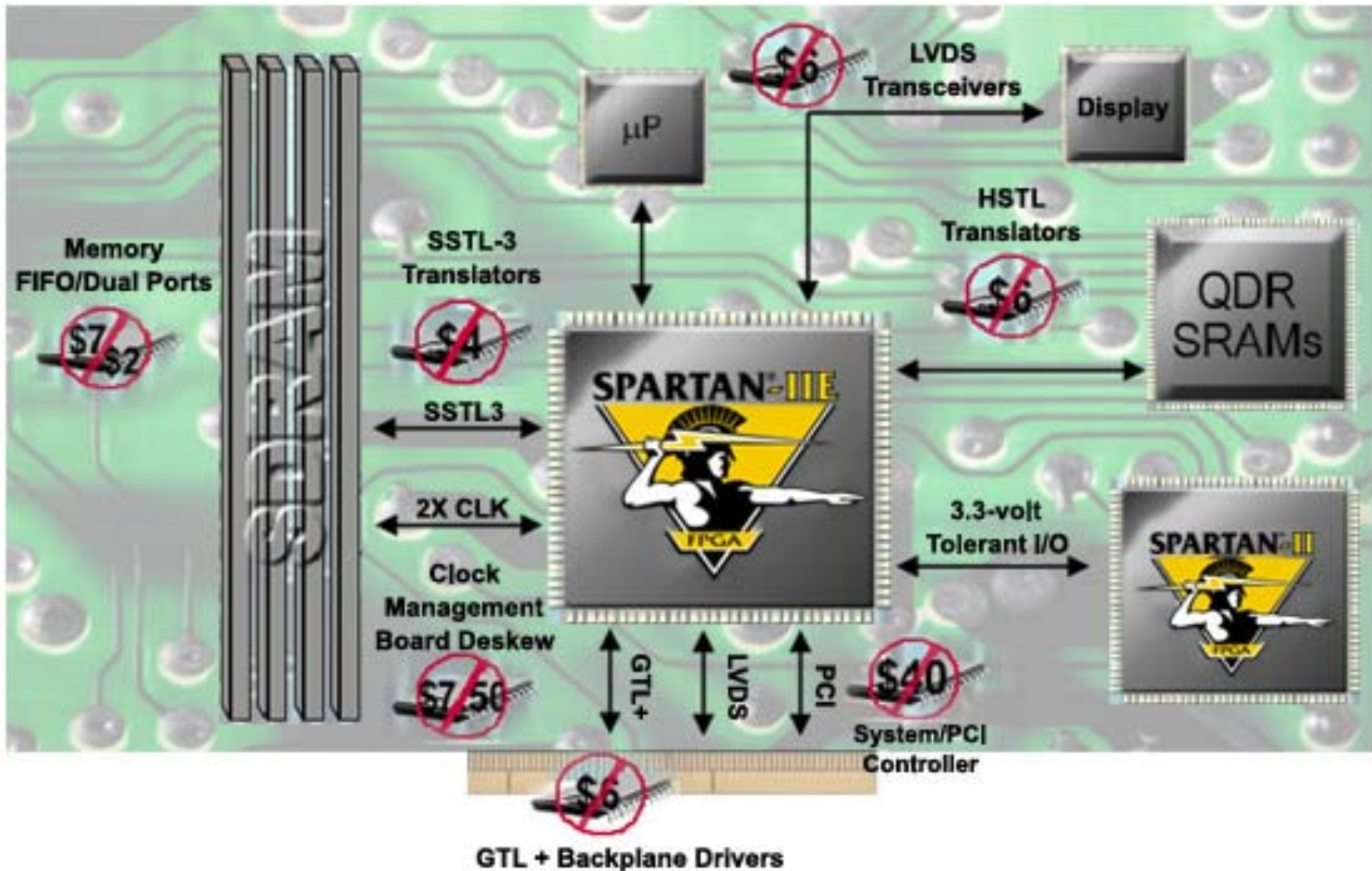
Spartan-II E: The Total Solution



FPGA Application Trends



Spartan-IIE - System Integration



Spartan-II E Features

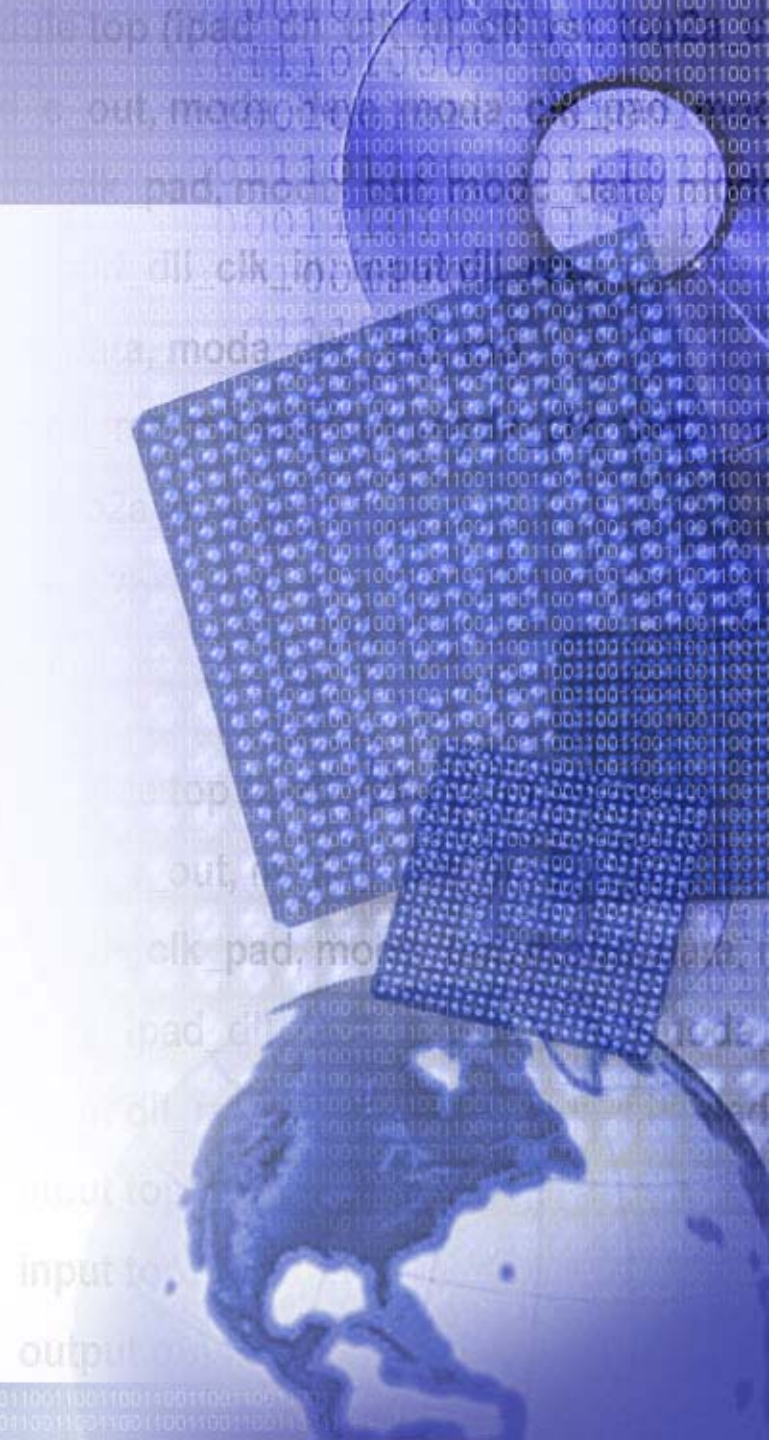
Value in Digital Video

Spartan-II E Silicon Features	Value for Digital Video Applications
FPGA Fabric and Routing, Up to 300,000 System Gates	Performance in excess of 20 billion MACs/second
Delay Locked Loops (DLLs)	Clock multiplication and division, clock mirror, Improve I/O Perf.
Select/I/O - HSTL-I, -III, -IV	High-speed SRAM interface
Select/I/O - SSTL3-I, -II; SSTL2-I, -II	High-speed DRAM interface
Select/I/O - GTL, PCI, AGP	Chip-to-Backplane, Chip-to-Chip interfaces
Differential Signaling - LVDS, Bus LVDS, LVPECL	Bandwidth management (saving the number of pins), reduced power consumption, reduced EMI, high noise immunity
SRL-16	16-bit Shift Register ideal for capturing high-speed or burst-mode data and to store data in DSP applications
Distributed RAM	DSP Coefficients, Small FIFOs
Block RAM	Video Line Buffers, Cache Tag Memory, Scratch-pad Memory, Packet Buffers, Large FIFOs



Spartan-II E LVDS Solution

System Applications, Clock Distribution, Cost Management, Pin Savings, EMI Reduction



What is LVDS?

- LVDS - Low Voltage Differential Signaling
- LVDS is a differential signaling interconnect technology
 - Requires two pins per channel
- LVDS was first used as a interconnectivity technology in laptops and displays to alleviate EMI issues
- Technology is now widely used in:
 - A broad spectrum of telecom and networking applications
 - Mainstream consumer applications like digital video and displays

Differential Signaling Benefits

- Higher performance per pin pair
- Reduced EMI
 - Low output voltage swing
 - Relatively slow edge rates (dV/dt)
- High noise immunity
 - Switching noise cancels between the two lines
 - Data is not affected by the noise
 - External noise affects both lines, but the voltage difference stays about the same
- Reduced power consumption

Spartan-II E Differential I/O Counts

Device	TQ144		PQ208		FT256		FG456	
	User	Diff	User	Diff	User	Diff	User	Diff
XC2S50E	102	28	146	50	182	84		
XC2S100E	102	28	146	50	182	84	202	86
XC2S150E			146	50	182	84	263	114
XC2S200E			146	50	182	84	289	120
XC2S300E			146	50	182	84	329	120

User = Maximum number of User I/Os available

Diff = Maximum number of Differential Paired I/Os available

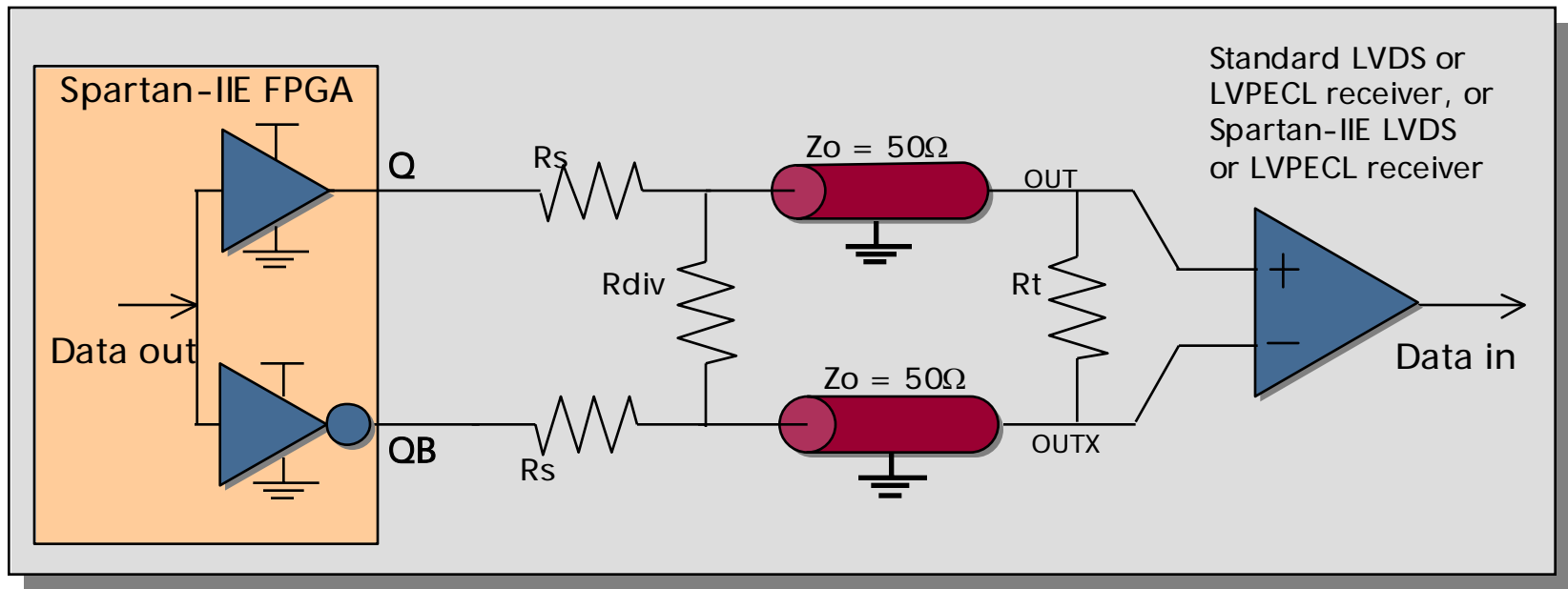
Spartan-IIe LVDS Support

- All IOBs have LVDS/BLVDS/LVPECL capability
- IOBs configured as LVDS can be :
 - Synchronous or asynchronous
 - Input or output
- Two IOBs (pair) form one LVDS signal.
 - One IOB will function as + or P
 - The other IOB will function as - or N.
- LVDS pin pairs are indicated in the datasheet
- Maximum number of LVDS pin-pairs: 120

Bus LVDS and LVPECL

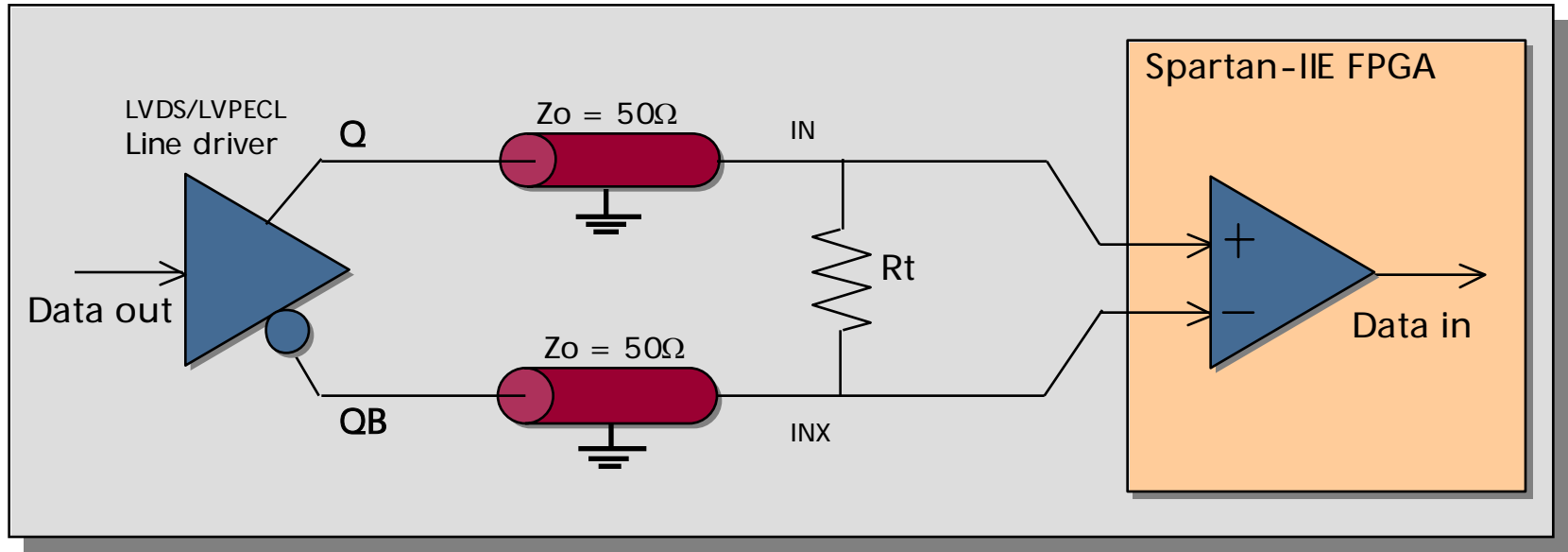
- Bus LVDS - Bi-directional LVDS
 - The device can transmit and receive LVDS signals through the same pins
 - Requires different termination than LVDS
- LVPECL - Low Voltage Positive Emitter Coupled Logic
 - Well known industry standard for fast clocking and interconnectivity
 - Voltage swing (~750 mV) over two differential connections

Spartan-II E as a Differential Driver



Capable of driving any standard LVDS or LVPECL receiver

Spartan-II E as a Differential Receiver



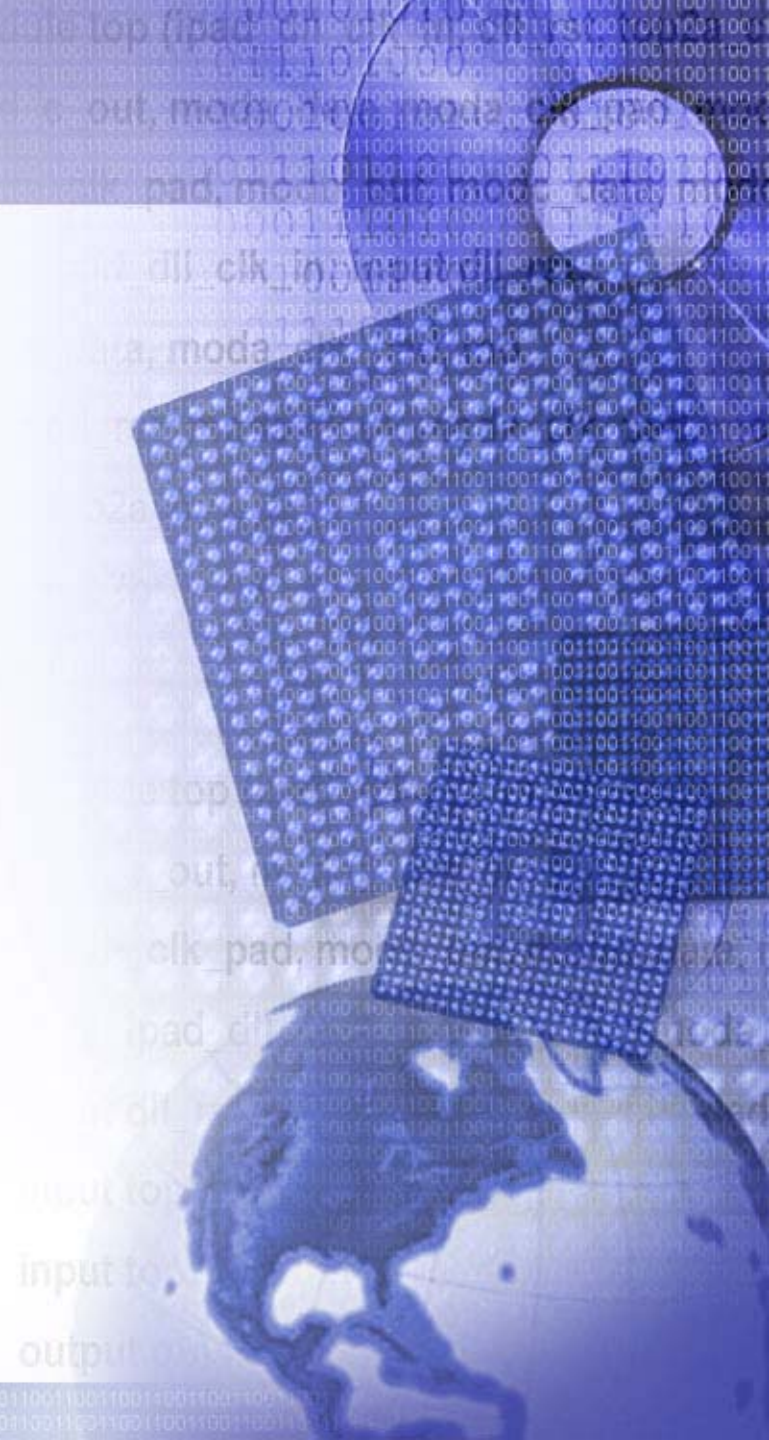
Spartan-II E can be driven by any standard LVDS or LVPECL driver
Spartan-II E receiver complies with the LVDS or LVPECL specs

Spartan-II E Core Support

- On-chip memory & storage
 - Distributed, BlockRAM, FIFOs
- Bus products
 - PCI (64- & 32-bit, 33/66MHz), Arbiter, CAN bus interface
- DSP functions (FIR filter)
- Error correction
 - Reed-Solomon, Viterbi
- Encryption (DES & TDES)
- Microprocessor
 - ARC 32-bit configurable RISC, 8-bit 8051 microcontroller
- Memory controllers (10+)
 - SDRAM, QDR SRAM
- Communications
 - ATM (IMA, UTOPIA), Fast Ethernet (MAC)
- Telecom
 - CDMA matched filter, HDLC, DVB satellite, ADPCM speech codec
- Video & image processing
 - JPEG codec, DCT/IDCT, color space converter
- UARTs



Programmable Solutions Advantages



Spartan-II Enhances Advantages of Programmable Logic

- Time-to-Market
- Flexibility
- Field Upgradable
- Cost Competitive

Xilinx Programmable Solutions Provide Several Benefits

- Accelerating time-to-market
 - Consumer devices require fast time-to-market
 - ASICs & ASSPs take 12-18 months to spin out
 - Immediate production upon design release
 - Fast design iterations
 - Rich, IP portfolio and efficient tools for design and synthesis
- System integration
- Testing and verification
 - Re-programmable means avoiding/reducing risk
 - Solutions are built on a proven FPGA technology with pre-verified silicon and IP that guarantees performance

Xilinx Programmable Solutions Provide Several Benefits

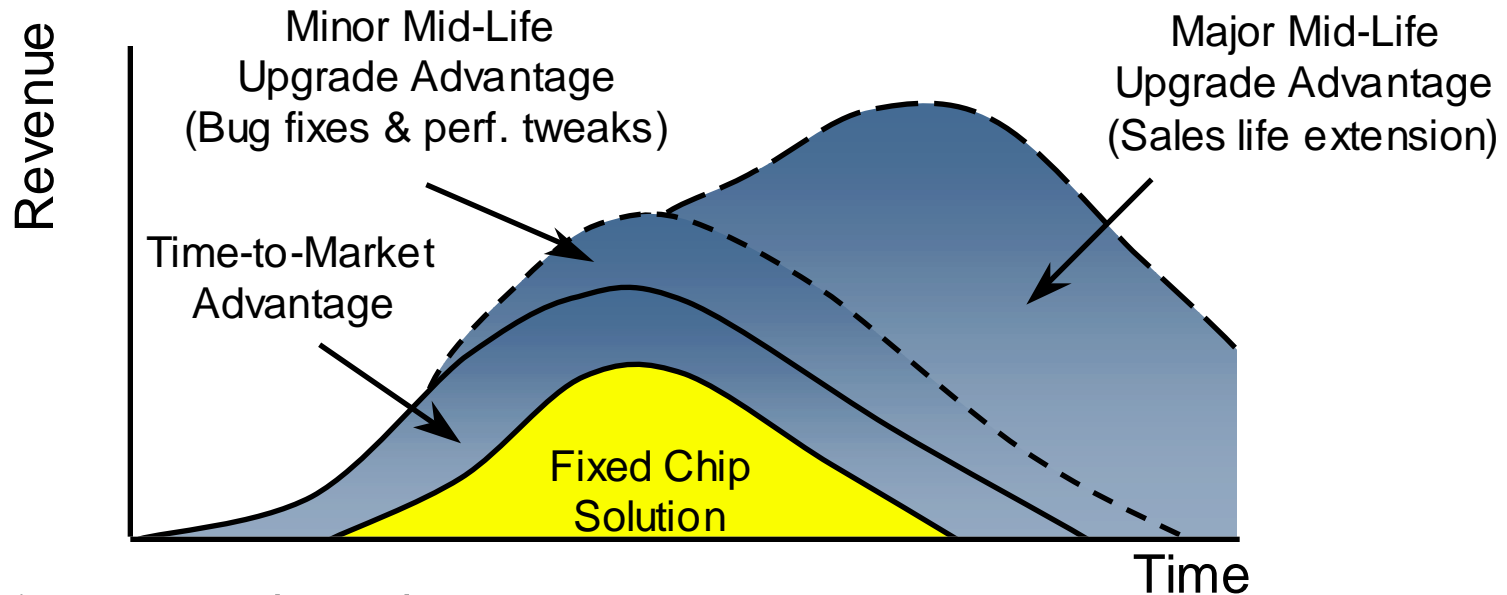
- Increased flexibility
 - Product customization to meet customer needs
 - Accommodate multiple standards & spec updates/changes
 - Feature upgrades through field upgradability (IRL)
 - Remote update of software and hardware
 - Increased lifetime for a product (time-in-market) and allows new, interesting applications
 - Enable product features per end user needs
 - Broad product line
 - Broad IP and tools solutions

Xilinx Programmable Solutions Provide Several Advantages

- Issues in creating a stand-alone ASIC/ASSP
 - Which standards and formats will win in which geographies?
 - Choosing the right solution: over-design or under-design
 - Product customization
 - Development cost and amortization
- System cost management and assured source of supply
 - Multiple sourcing for key high \$ BOM components
 - Reduced support costs via IRL
 - Commodity component flexibility
 - Programmable logic solutions are standard parts
- Low cost

PLD Development Flow Advantages

Accelerating Time-to-Market, Extending Time-in-Market



- Time-to-Market advantage
 - First to market increase market share and revenue advantage
- Time-in-Market advantage
 - Maintains/extends competitive position
 - Can greatly increase lifecycle revenue yield

Xilinx Solutions for Digital TVs

- High-speed image/signal processing needs, coupled with large bandwidth requirements of HDTV can be met with low-cost Spartan-II E FPGAs with LVDS I/O
- Image processing can be done real-time in FPGAs
 - Cuts down on memory requirements
- Numerous standards (and versions) cause uncertainty so designs need flexibility
 - Transmission schemes, MPEG profiles, display formats, color correction etc.
- Xilinx FPGAs can differentiate your product from the competition while still conforming to the latest revision of standards
- Spartan-II E FPGAs offer flexible, cost-effective solutions to ASSPs
- Faster time-to-market and longer time-in-market