



2018 Xilinx Security Working Group (XSWG) Washington, D.C. Agenda

Crowne Plaza Dulles Airport Hotel, 2200 Centreville Rd., Herndon VA 20170

Tuesday, November 6, 2018	
All Lectures in Salon A/B	
Topic	Time
Check In and Continental Breakfast	7:15 - 8:15
Welcome / Introduction to Xilinx Security	8:15 - 8:45
Next Generation Security / Survey	8:45 - 9:45
Break	9:45 - 10:15
Everest Introduction	10:15 - 10:45
Everest Security I	10:45 - 11:45
Lunch	11:45 - 12:45
Everest Security II	12:45 - 2:00
Break	2:00 - 2:30
Everest Security III	2:30 - 3:45
Break	3:45 - 4:15
Guidance on Essential Security Design Resources/Information	4:15 - 5:00
Day 1 Wrap Up / Summary Statements	5:00 - 5:15
Join us for appetizers and drinks! Evening Social and Partner Demonstrations Crowne Plaza Hotel, Ballroom Foyer	5:30 - 7:30



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Wednesday, November 7, 2018		
Check In and Continental Breakfast		7:45 - 8:15
Lectures :Salon A/B	Time	Demonstrations : Salon C
All Hands Day 2 Re-Greet	8:15 - 8:30	(No Demo This Period)
Zynq UltraScale+ MPSoC Security	8:30 - 9:00	UltraScale and UltraScale+ FPGA Secure Configuration
	9:00 - 9:30	UltraScale and UltraScale+ FPGA Tamper Logging and Penalty Response
Break	9:30 - 10:00	Break
Zynq UltraScale+ MPSoC Secure Boot	10:00 - 11:00	Functional and Physical Isolation Within the Programmable Logic (PL) of the Zynq UltraScale+ MPSoC
Zynq UltraScale+ MPSoC Trusted Execution Environment	11:00 - 12:00	Functional and Physical Isolation Within the Processing Subsystem (PS) of the Zynq UltraScale+ MPSoC
Lunch	12:00 - 1:00	Lunch
Authority Message	1:00 - 2:00	Zynq UltraScale+ MPSoC Secure Boot
Xilinx TRUST/DoD5200.44	2:00 - 3:00	
Break	3:00 - 3:30	Break
Security Monitor (SecMon) IP	3:30 - 4:00	Zynq UltraScale+ MPSoC Enhanced Key Revocation
	4:00 - 4:30	Secure Storage Using the Zynq UltraScale+ MPSoC Physical Unclonable Function (PUF)
Next Generation Survey Results	4:30 - 5:00	(No Demo This Period)
XSWG 2018 Adjournment and Door Prizes	5:00 - 5:15	

Classified Session

Thursday November 8, 7:30am check in, 1:00pm conclusion

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