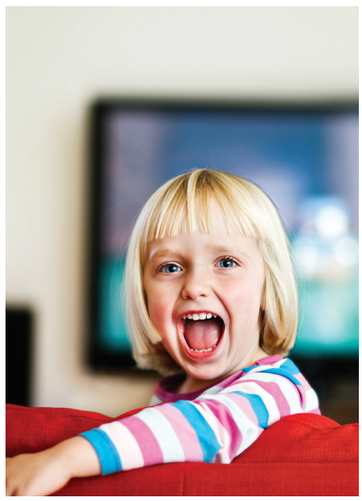
CASE STUDIES

ACCELERATING TOWARD ZERO DEFECTS

Customer Success = Xilinx Success



Xilinx has a long history of delivering products and services that accelerate the process of designing quality. This commitment to quality benefits many markets including communications, automotive, aerospace, defense, medical, and industrial. To meet the stringent requirements of these and other quality-sensitive markets and applications, Xilinx offers customers access to a dynamic infrastructure with the goal of producing defect-free product experiences. The Xilinx zero-defect mindset and goals drive ongoing iterative improvements. While this takes a tremendous level of focus and partnership, the rewards have been extraordinary.

ENGINEERING PRODUCT QUALITY	QUALITY IMPLEMENTATION
Design for quality and reliability	Design-for-manufacturability (DFM) and design-for-test (DFT) methodologies
	Software Before Silicon drives test development efficiency
	Process and Performance Learning Vehicles (PPLVs), leading to shorter times to stable process, best-known methods (BKM), and pre-qualification cycle of learning
	Enhanced verification and characterization prevents late discovery of critical issues
Manufacturing readiness	Metrics for engineering samples and production units
	Design tools released at the same time
	Defect density, line yield, assembly yield, test coverage, test yield, qualification
New Product Evaluation (NPE) and New Product Introduction (NPI) process controls and release criteria	Design tapeout release criteria
	Design tools released with silicon
	Hard production review and release criteria

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ENGINEERING QUALITY PROCESSES	KEY RESULTS
Address manufacturing variability	Enhanced design tools
	Scalable optimized architecture
	Enhanced manufacturing corner material available for better qualification of customer designs*
Robust qualification certifications	TL9000 re-certification with no major findings
	ADQ "V-Flow" qualified aerospace products
	DO-254 qualification
	Maintain stringent compliance to TS16949 and ensure all Xilinx suppliers certified to TS16949 ▪ Xilinx Automotive (XA) products qualified to AECQ100 / Beyond AECQ100 ▪ Continuation of special automotive processes (PPAP, change control, etc.)

** To learn if your company qualifies for this program, contact the Xilinx quality team at: wwcqe@xilinx.com*

High-volume customer applications can achieve the zero-defect level of quality. Xilinx has proven this repeatedly in structured customer collaborations, and many of our customers report this level of quality for Xilinx-based products. Taking a disciplined approach to defect reduction with customers creates synergy through joint design reviews, manufacturing corner material, and focused teamwork. In successful engagements, collaborative efforts often extend beyond customer engineering teams to support contract manufacturers in an ever-increasing supply chain. By working with Xilinx, engineers can enjoy a process that delivers superior results and creates a valuable advantage in the market in terms of the end quality of the systems produced.

ENGINEERING DEVELOPMENT	KEY STEPS & HIGHLIGHTS
Collaborate during early development process	Validate interoperability
	Build final bill of materials
	Create and validate customer design
Quality training to aid the design process	Initiate and verify prototype build
	Online training focused on improving design margin
	FPGA Design Quality Checklists to avoid common pitfalls
	Field application engineering (FAE) support to drive best practices
Reduce/eliminate in-line manufacturing issues	Work closely with contract manufacturers to: ▪ Increase troubleshooting capabilities and signature analysis ▪ Address common manufacturing issues such as electrical overstress damage ▪ Facilitate hands-on customer involvement

** For more information, visit: http://www.xilinx.com/products/quality/fpga_best_practices.htm*

XILINX®

PRODUCT QUALITY ENGINEERING

Engineering Customer Quality Improvements

CASE STUDIES

In today's highly dynamic and fiercely competitive markets, customers need quick identification and resolution of any problem that potentially impacts system quality. Xilinx recognizes this need and works with customers to rapidly assess product issues, mitigate risks, and ensure uninterrupted production processes.

To better support customers, Xilinx engages at the first indication of any potential problem. Field applications engineers (FAEs) work with the customer's engineering teams to quickly diagnose issues, and, when necessary, bring in second-level technical support experts from around the globe. Once diagnosed, the issue is turned over to factory-based customer quality engineers who efficiently track and manage each case, coordinate the engineering data, and prioritize issues to ensure the fast, efficient handling of any urgent situations.

To keep customers informed at every step of the process, an online Return Materials Authorization (RMA) portal provides at-a-glance real-time status. In today's complex multinational manufacturing and design environments, this system gives stakeholders visibility and speeds issue resolution.

Since 2009, Xilinx has diagnosed more than half of all customer issues in the field, and has achieved aggressive cycle time targets for RMA cases based on customer needs. RMA on-time delivery metrics have driven steady improvements to Xilinx support capabilities and helped ensure predictable processes and results. Xilinx product quality engineers work with factory engineering teams to diagnose escapes, improve outlier prevention, and drive FPGA failure rates lower year after year.

ACCELERATING PROCESSES	AREAS COVERED
Collaborative engineering and learning	Early Product Quality Engineering engagement and learning with new product teams
	Early engagement in 7 series (28 nm) products, including Xilinx® Artix™, Kintex™, Virtex®, and Zynq™
	Acquire knowledge on silicon issues and fixes from tapeout to production
	Rapid learning curve in resolving new product quality issues
Provide quality solutions	Smooth and seamless handoff process for silicon through application issues
	Proactive relevant data/case information collection
	Hardware and design tool readiness
Improve RMA processes	Integrated communication process with technical support for seamless transitions that streamline component, software, and application issue resolution
	RMA quality escalation system (QES) and best practices deployed globally to expedite the capture and resolution of quality issues
	Customer-centric RMA portal enhancements enable customers to: ▪ Log and track issues ▪ Open cases automatically using systematic triggers and email notifications

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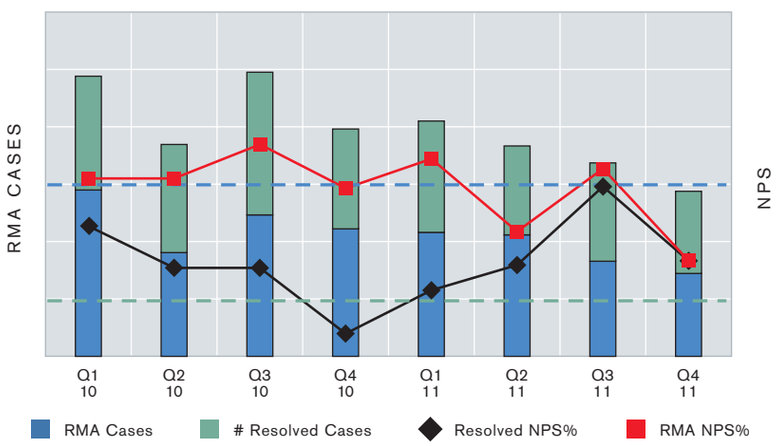
Xilinx customers have responded positively, giving Xilinx consistently high net promoter scores (NPSs) throughout 2011. In 2012, Xilinx will continue to place emphasis on speedy issue resolution and work with customers to further evolve processes that drive up product quality.

GOALS FOR ACCELERATING ISSUE RESOLUTION	KEY RESULTS IN 2011
Reduce customer returns through proactive engagements that address critical needs with superb response times	45% reduction in RMAs since 2009
	Consistently resolved customer issues within committed time expectancy
	15 days average TAT in 2011
Reduce no evidence of failure (NEOF) cases through FAE learning and 100% post-case customer engagement	47% reduction of NEOF identified cases in 2011
	Educated contract manufacturers on EOS causes
	Drove closed-loop process with customers to identify root cause issues
	85% of NEOF verification were customer issues
	Top customer issues related to customer manufacturing or applications
Monitor and optimize customer satisfaction levels	Evaluated RMA portal based on customer feedback
	Expanded request options: analysis request categories now include *visual mechanical*, *administrative*, and *development kit* issues
	Added a "Contributor" section: users can now distribute the RMA portal request form to colleagues via an easy-to-use link and automatic email notifications
	Improved file management: customer files and Xilinx analysis reports can now be uploaded and retrieved directly via RMA portal case links, without downloading from email notifications
	RMA portal unified for simpler RMA processing by including *visual mechanical* RMAs

RMA Customer Satisfaction



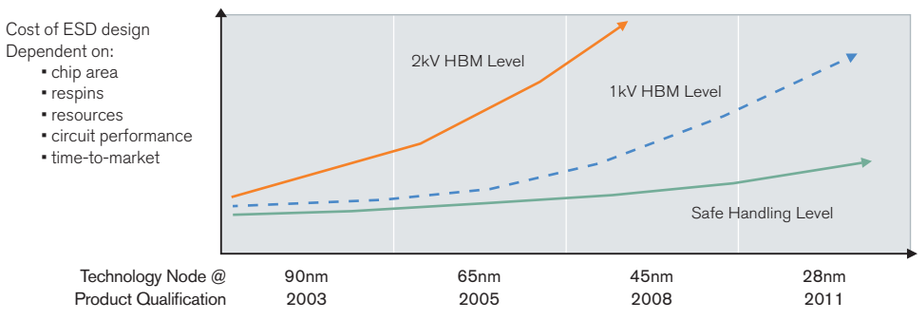
Xilinx achieved excellent customer satisfaction ratings for RMA cases that did not require failure analysis.

CASE STUDIES

INDUSTRY ESD TRENDS

Over the last 40 years or more, electrostatic discharge (ESD) requirements have become an increasingly important consideration in electronics design and operation. As device geometries shrink, ESD assessment becomes even more critical. As a result, Xilinx invests resources and expertise each year to help customers better understand the risks and adopt optimal approaches for managing ESD. Xilinx also aims to maintain the ESD levels for Human Body Model (HBM) and Charge Device Model (CDM) as high as possible while reducing the feature size. Xilinx designs products with ESD protection circuitry that is extensively tested and qualified before product release. Reliability monitoring data is published quarterly on *www.xilinx.com*.

Cost of ESD Protection



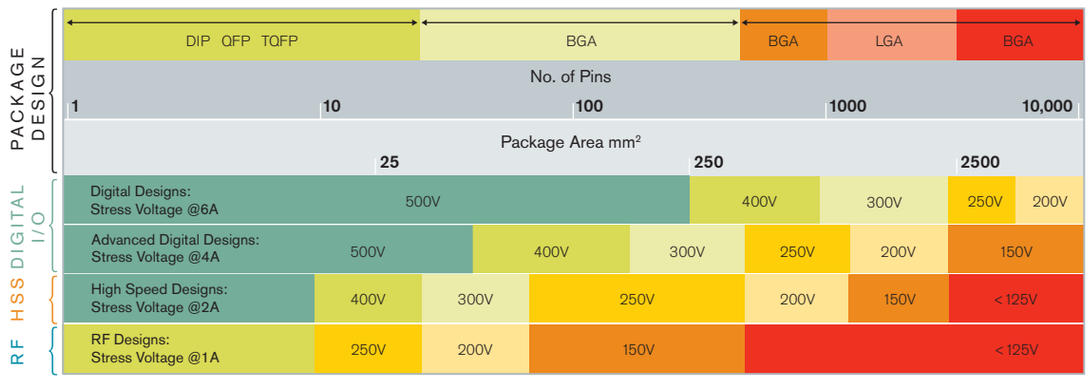
Source: JEDEC (JEP155)

Challenges Surrounding Smaller Devices

New technology nodes bring improved speed and power. The design changes required to improve performance make protecting the devices more difficult given the continuous drive toward smaller features, thinner oxides, lower breakdown voltages, and high-performance I/O. As a result, breakdown voltages are reduced, leaving devices more susceptible to ESD damage. All of these elements combine to make maintaining existing ESD levels a significant challenge.

Putting Focus on the Right Parameters

In 1995, 2kV HBM and 500V CDM were the standard. Today, the ESDA, JEDEC, and AEC organizations are all evaluating lowering ESD limits to keep pace with current semiconductor trends.



CDM package map projected for 22nm designs. Products with >1000 pins or 1200mm² area would be limited to <150V CDM passing voltage for all HSS and RF designs.

Source: JEDEC (JEP155)

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The costs associated with protecting devices have been rising. But, the benefits of minimizing field risk come through pursuit of controls around CDM as opposed to HBM. Many ESD experts have concluded that HBM has been overspecified, since the failure rate due to electrical stress is independent of the achieved HBM level of > 500V.

CDM is now evolving to become the key parameter for device-related ESD investments, particularly in view of CDM-related drivers, such as large packages and pin counts, thinner metal and higher current density, and higher-speed pins.

A Key Consideration

Many real-world failures attributed to electrical overstress (EOS) are actually caused by more severe ESD failures beyond the device level, such as charged-board events (CBEs) and cable discharge events (CDEs). The failure analysis data of more than 11 billion devices collected by the members of the JEDEC council showed that EOS/ESD failures can appear in the field independent of the CDM robustness level from less than 100V to greater than 2,000V. Case studies showed that most of the field failures in the data are due to EOS or CBEs. These EOS-like failures normally did not occur on the weak pins but on more robust pins that are somewhat exposed. Also, these CBE-like failures are not directly comparable to CDM failures. Rather, they have their origin in the charging of the board, which can be assessed in the same way as legitimate CDM failures.

A Proactive Approach

Companies can avoid costly field failures by proactively preventing failures in the factory. Investments in factory controls for comprehensive ESD protection can be based on standards such as ANSI/ESDA S20.20 or IEC 61340-5-1. These broadly accepted standards have been proven to be effective by many OEMs and contract manufacturers. Xilinx also aims to maintain the ESD levels for HBM and CDM as high as possible while reducing the feature size.

System-Level ESD Protection Recommendations

Commonly used system-level ESD protection and mitigation methods include:

1. **Discrete diodes, resistors, and capacitors:** Wherever design performance and real estate allow, put a capacitor between power and ground, a clamp diode, or a resistor in series of the I/O pins of the ICs. This method may not be a viable solution if the extra added loads slow down the performance of the design to an unacceptable level.
2. **Shielded interface connectors:** With a shielded connector, the discharge will be directed to the metal shield and then to the ground, thereby eliminating damage to component pins.
3. **Make ESD-resistant enclosures:** For enclosure design, the overall goal is to keep all ESD outside the enclosure. The best way to achieve this is to use an electrically nonconductive (typically plastic) enclosure. Since plastic materials have a dielectric constant two to three times that of air, their breakdown voltage is a lot higher than air's. Therefore, the thickness of plastic needed is significantly less than in air to achieve 8kV discharge (IEC 61000-4-2 requirement).
4. **PCB layout:**
   a. Use separate power and ground plane in multilayer PCB design
   b. Keep bypass capacitor close to each power pin of all IC's
   c. Have multi-point grounds on the PCB to connect to the chassis

COUNTERFEIT AND UNAUTHORIZED ELECTRONICS

CASE STUDIES

Over the past 10 years there has been a dramatic increase in the numbers of reported incidents of counterfeit semiconductor devices appearing in supply chains around the world. Xilinx has taken aggressive actions to ensure the integrity of its authorized partners and supply chain to combat the proliferation of counterfeit materials. Like many semiconductor companies, Xilinx protects its trademarks in the United States and internationally, which results in the seizure of counterfeit products globally.

Economic slowdowns, or any market conditions that drive down demand, can lead to excess inventories of electronic components. Some of these excesses are diverted from authorized distribution channels or end users into the gray market for subsequent sale by electronic component brokers and after-market resellers. There is also some evidence of disreputable dealers harvesting components from discarded electronics, and subsequently reworking and selling them in the gray market. With the rise in the number of gray market electronic component brokers and Internet marketplaces, some of which may have connections with otherwise reputable distributors, consumers are at increased risk.

While the gray market may offer short-term advantages over parts obtained through authorized distribution channels, there are no standards, controls, or records to verify proper storage and handling. Since the quality and reliability of those parts cannot be assured, Xilinx and other vendors in the same situation do not authorize the pass-through of warranty for any such devices.

Xilinx invests significant resources and energy to ensure that reliable, high-quality components are supplied to customers. These standards of quality and reliability are maintained through exhaustive internal efforts, and formalized procedures and audits with authorized distributors. This contributes to industry-leading quality and product reliability FIT rates.

To manage the quality of its products, Xilinx uses unique traceability mechanisms. This not only allows for better customer quality support, but also aids in identifying and deterring counterfeit products. In addition, the newest generations of Xilinx components include a programmed internal code that is used in conjunction with existing mechanisms.

U.S. Customs and Border Protection has been identifying counterfeit materials entering various points of entry. The table and charts below and on the back page show an increase in the overall numbers of seizures, as well as in the proportion of incidents categories that relate to Xilinx devices: electronic articles, and critical technology components. For a complete Customs and Border Protection report, please visit:

http://www.cbp.gov/linkhandler/cgov/trade/priority_trade/ipr/ipr_communications/seizure/ipr_seizures_fy2011.ctt/ipr_seizure_fy2011.pdf

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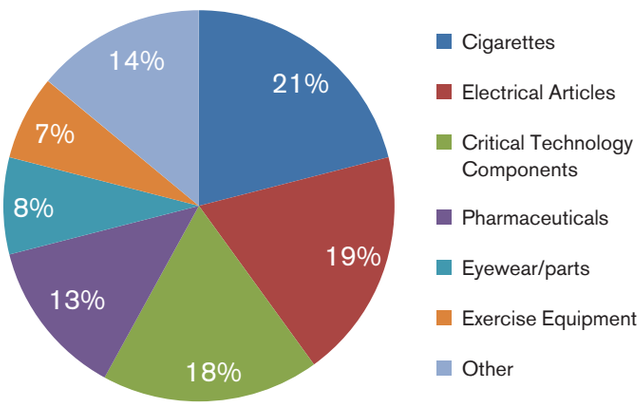
For protection from the risks of unauthorized parts, customers are advised to restrict the purchases of products to Xilinx direct channels or one of the company's authorized distributors. A list of these authorized distributors is posted at:

http://www.xilinx.com/company/sales/ww_disti.htm

U.S. Customs Seizure Totals

	FY2009	FY2010
Domestic Value USD$ (millions)	$260.60	$188.10
MSRP Value USD$ (est. in millions)	$2,065	$1,413

FY2010 Consumer Safety and Critical Technologies



FY2009 Consumer Safety and Critical Technologies