CASE STUDIES

INTEGRATED SOFTWARE QUALITY

Streamlining Downloads: Counteracting Code Expansion

Over the last several releases of Xilinx ISE® Design Suite, there has been a significant increase in the software platform code size. To counteract otherwise dramatic increases in download times for customers, a Xilinx initiative aimed at reducing the size of the ISE Design Suite was implemented for the 12.1 release in Q1 2010.

This case study reports on the steps that Xilinx has taken to optimize code size, and describes the results for the end users.

Project Objective

- *60% reduction in the size of ISE Design Suite 12.1, resulting in less than 4GB for downloading*

Steps Taken

A total of 13 separate projects were carried out by teams in California, Colorado, and Scotland. The combined efforts addressed all of the key software components: Embedded Design Kit (EDK), ISE, IP, PlanAhead,™ System Generator for Digital Signal Processing (DSP), the installer, and data files. The major contributions to the success of the overall initiative included:

- *A new compression algorithm, leading to a 30% reduction in the size of all ISE Design Suite files*
- *Optimized device data for the FPGA Editor*
- *Optimized documentation for IP subsystems, to reduce the size of the .pdf files*

Results

Even though the planned enhancements for release 12.1 translated into 1.2GB of additional code, the code-size reduction initiative resulted in impressive results:

- *Previous release (11.3) download size: 9.84GB*
- *Final 12.1 download size: 3.78GB*

Benefits

The code-size reduction initiative exceeded the initial goal, achieving a 66% overall reduction. Additionally:

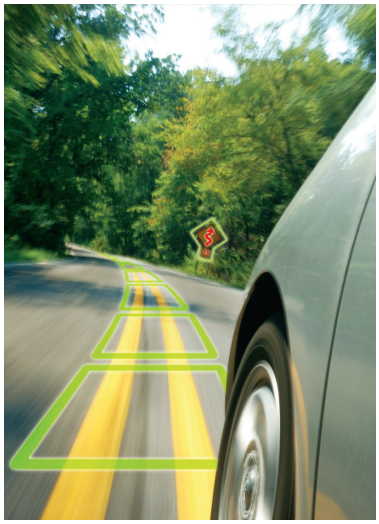
- *ISE Design Suite install image fits on a single one-sided DVD*
- *For Windows systems, the download size of ISE Design Suite 12.1 is 27% smaller than the nearest competitor (2.86GB, compared with 4.5GB)*
- *For Linux systems, ISE Design Suite 12.1 is 16% smaller than the nearest competitors (2.81GB vs. 3.8GB)*
- *According to the ISE Design Suite Quality Survey completed in November 2010, customer satisfaction increased by 20% for version 12.1*

As a result of the intiative, all of the 12.x update releases came in at less than 4GB in size.

CASE STUDIES

ACCELERATING TOWARD ZERO DEFECTS

Customer Success = Xilinx Success



Xilinx has a long legacy of delivering products and services that accelerate the process of designing quality into automotive, aerospace and defense, and medical electronics systems. To meet the stringent requirements of these and other quality-sensitive markets, Xilinx offers customers access to an infrastructure continuously tuned for defect-free product experiences. While this effort takes a tremendous level of focus and partnership, the rewards have been extraordinary. Xilinx remains committed to this mission and the belief that customer success is the ultimate metric for the company's success.

ACCELERATING PRODUCT QUALITY	QUALITY IMPLEMENTATION
Design for quality and reliability	Design-for-manufacturability (DFM) and design-for-test (DFT) methodologies
Manufacturing readiness	Metrics for engineering samples and production units
	Defect density, line yield, assembly yield, test coverage, test yield, qualification
New product evaluation (NPE) and new product introduction (NPI) process controls and release criteria	Stricter design tapeout release criteria based on 6 series learning
	Refined NPE/NPI checklists
	Hard production review and release criteria
Organize to drive new product introduction	Functional organization alignment
	Global integration of QA and NPE/NPI engineering

CONT'D. >>

ACCELERATING QUALITY PROCESSES	KEY RESULTS
Eliminate defects for customer applications	Shipped more than 11.4 million units with zero PPM for high-volume consumer applications
Address manufacturing variability	Manufacturing corner material available for better qualification of customer designs*
Robust qualification certifications	TL9000 re-certification with no major findings
	ADQ "V-Flow" qualified aerospace product
	DO 254 qualification
	Maintain stringent compliance to TS16949 and ensure all Xilinx suppliers certified to TS16949 ▪ Continue to follow standard TS16949 audit schedule ▪ "XA" automotive products qualified to AECQ100 / 2x AECQ100 ▪ Continuation of special automotive processes (PPAP, change control, etc.)

** To learn if your company qualifies for this program, contact the Xilinx quality team at: wwcqe@xilinx.com*

Xilinx has proven repeatedly in structured customer collaborations that high-volume customer applications can achieve zero-defects. This disciplined approach creates synergy between Xilinx and customers through joint design reviews, manufacturing corner material, and focused teamwork. Collaborative efforts often extend to the support of contract manufacturers. By working with Xilinx, designers can enjoy a process that delivers superior results and creates a valuable advantage in system introduction and quality.

ACCELERATING DEVELOPMENT	KEY STEPS & HIGHLIGHTS
Collaborate during early development process	Validate interoperability
	Create and validate customer design
	Initiate and verify prototype build
Quality training to aid the design process	Manufacturing corner materials to improve design margin
	FPGA design quality checklists to avoid common pitfalls*
	FAE support to drive best practices
Reduce/eliminate in-line manufacturing issues	Work closely with contract manufacturers to: ▪ Increase troubleshooting capabilities and signature analysis ▪ Address common manufacturing issues such as electrical overstress damage ▪ Facilitate hands-on customer involvement

** For more information, visit: http://www.xilinx.com/products/quality/fpga_best_practices.htm*

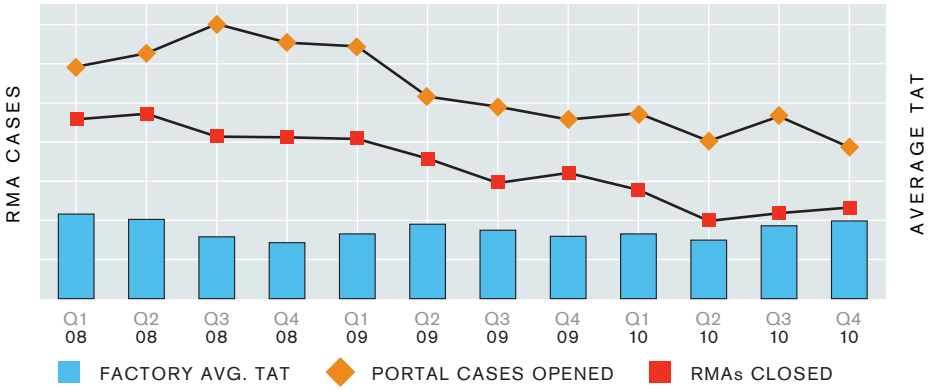
CASE STUDIES

PRODUCT QUALITY ENGINEERING

Accelerating Quality with Superior Customer Experience

In today's highly dynamic and fiercely competitive markets, customers need fast resolution of any problem that will potentially impact system quality. Xilinx recognizes the need to help customers rapidly assess product issues, mitigate risks, and ensure uninterrupted production processes.

RMA Trends



Customers can engage Xilinx at the first indication of any potential problem, knowing that Xilinx customer quality engineers (CQEs) will efficiently track and manage each case, perform rigorous case reviews for problem diagnosis, and prioritize issues to ensure urgent situations are efficiently escalated. To keep customers informed at every step of the process, an online return materials authorization (RMA) portal provides at-a-glance real-time status updates. In today's complex multinational manufacturing and design environments, this system keeps all stakeholders informed and speeds issue resolution.

ACCELERATING PROCESSES	AREAS COVERED
Early Product Quality Engineering (PQE) engagement with NPI team	New product early engagement
	Acquire knowledge on silicon issues and fixes from tapeout to production
	Rapid learning curve in resolving new product quality issues
Provide quality solutions	Smooth and seamless hand-off process for silicon through application issues
	Proactive relevant data/case information collection
	Hardware and design tool readiness
Improve RMA processes	Integrated communication process with Technical Support provides seamless transitions that streamline component, software, and application issue resolution
	RMA quality escalation system and best practices deployed globally to expedite the capture and escalation of quality issues
	Customer-centric RMA portal enhancements enable customers to: ▪ Log and track issues ▪ Open cases automatically using systematic triggers and e-mail notifications

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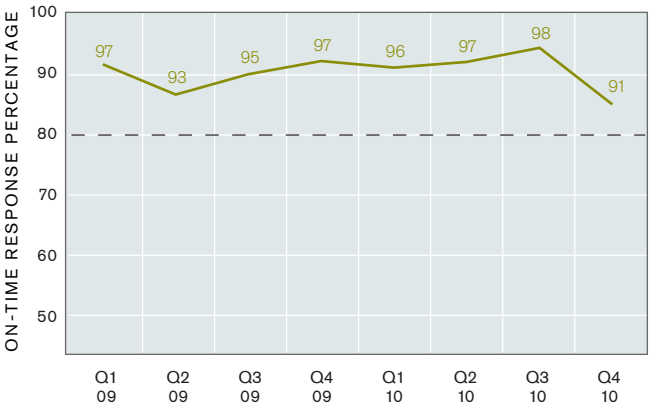
Since 2008, Xilinx has set and achieved cycle time targets for RMA cases based on customer needs. On-time delivery metrics have yielded steady improvements of Xilinx support capabilities and helped ensure predictable processes and results.

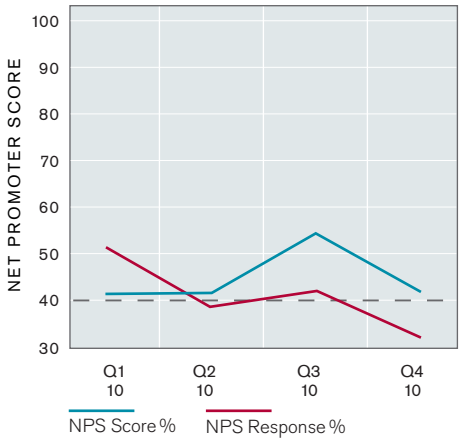
GOALS FOR ACCELERATING ISSUE RESOLUTION	KEY RESULTS IN 2010
Reduce customer returns through proactive engagements that address critical needs with superb response times	▪ 55% reduction in RMAs since 2008 ▪ Consistently resolved customer issues within committed time expectancy
Reduce no evidence of failure (NEOF) field application engineer (FAE) cases through FAE learning and 100% post-case customer engagement	▪ 10% reduction of NEOF identified cases in 2010 ▪ Educated CMs on EOS causes ▪ Drove closed-loop process with customers to identify root cause issues
Monitor and optimize customer satisfaction levels	▪ Modified RMA portal based on customer feature feedback ▪ RMA portal expanded for visual mechanical RMAs

Xilinx customers have responded positively, giving Xilinx consistently high net promoter scores (NPS) throughout 2010. In 2011, Xilinx will continue to place emphasis on speedy issue resolution and work with customers to further evolve processes that drive up product quality.

RMA Commitments



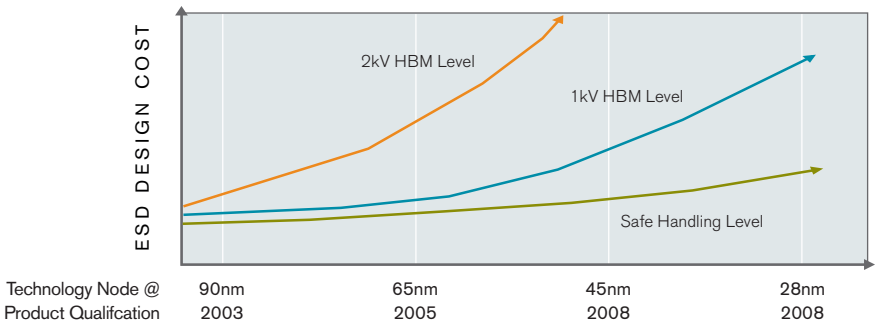
Customer Satisfaction



INDUSTRY ESD TRENDS

Over the last 40 years or more, electrostatic discharge (ESD) requirements have become an increasingly important consideration in electronics design and operation. As device geometries shrink, ESD assessment becomes even more critical. As a result, Xilinx invests resources and expertise each year to help customers better understand the risks and adopt optimal approaches for managing ESD.

Cost of ESD Protection



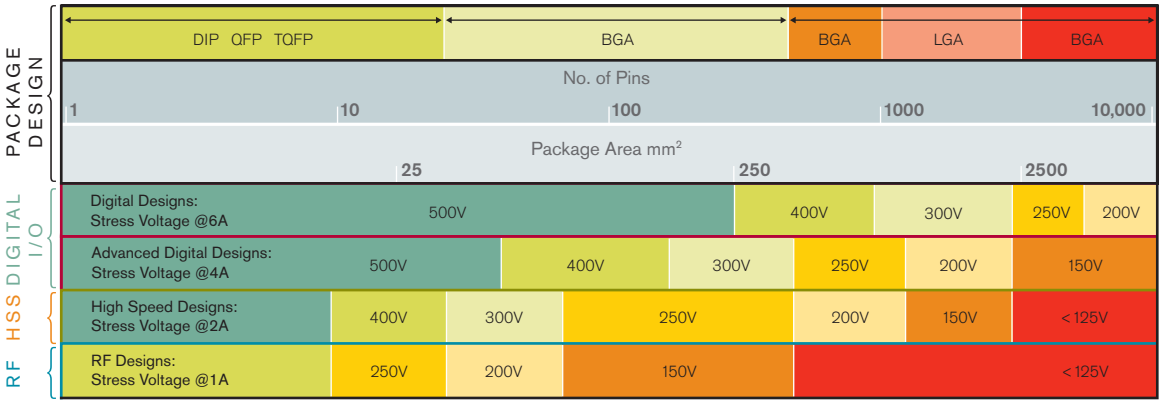
Source: JEDEC (JEP155)

Challenges Surrounding Smaller Devices

New technology nodes bring improved speed and power. The design changes required to improve performance make it more difficult to protect the devices, given the continuous drive toward smaller features, thinner oxides, lower breakdown voltages, and high-performance I/O. As a result, breakdown voltages are reduced, leaving devices more susceptible to ESD damage. All of these elements combine to make maintaining existing ESD levels a significant challenge.

Putting Focus on the Right Parameters

In 1995, the 2kV human body model (HBM) and 500V charge device model (CDM) were the standard. Today, the ESDA, JEDEC, and AEC organizations are all evaluating lowering ESD limits to keep pace with current semiconductor trends.



CDM package map projected for 22nm designs. Products with >1000 pins or 1200mm² area would be limited to <150V CDM passing voltage for all HSS and RF designs.

Source: JEDEC (JEP155)

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The costs associated with protecting devices have been rising. But the benefits of minimizing field risk come through pursuit of controls around CDM as opposed to HBM. Many ESD experts have concluded that HBM has been overspecified since the failure rate due to electrical stress is independent of the achieved HBM level > 500V.

CDM is now evolving to become the key parameter for ESD-related investments, particularly in view of CDM-related drivers, such as large packages and pin counts, thinner metal and higher current density, and higher-speed pins.

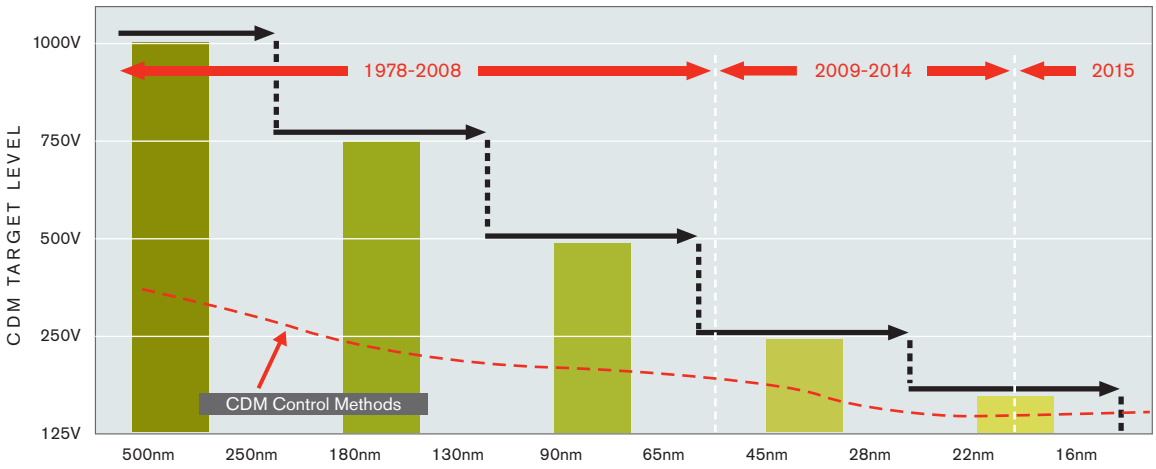
A Key Consideration

Many real-world failures attributed to electrical overstress (EOS) are actually caused by ESD failures beyond the device level, such as charged board events (CBEs) and charged cable events (CCEs). Printed circuit boards (PCBs) have much higher capacitance than individual devices; consequently, the damage associated with a CBE is much more severe than a CDM/HBM ESD event and is often mistaken for EOS. Even if all the individual components used for a given PCB have high device-level ESD robustness, one or more of these components may be very susceptible to ESD damage when mounted on a PCB. Therefore, before attributing an IC failure on a PCB to EOS, the possibility of CBE-related ESD damage should be explored.

The failure analysis data of more than 11 billion devices collected by the members of the JEDEC Council showed that EOS/ESD failures can appear in the field independent of the CDM robustness level from less than 100V to greater than 2,000V. Case studies showed that most of the field failures in the data are due to EOS or CBEs. These EOS-like failures normally did not occur on the weak pins but on more robust pins that are somewhat exposed. Also, these CBE-like failures are not directly comparable to CDM failures. Rather, they have their origin in the charging of the board, which can be assessed in the same way as legitimate CDM failures.

A Proactive Approach

Companies can avoid costly field failures by proactively preventing failures in the factory. Investments in factory controls for comprehensive ESD protection can be based on standards such as ANSI/ESDA S20.20 or IEC 61340-5-1. These broadly accepted standards have been proven to be effective by many OEMs and contract manufacturers. Xilinx also aims to maintain the ESD levels for HBM and CDM as high as possible while reducing the feature size.



Source: JEDEC (JEP155)

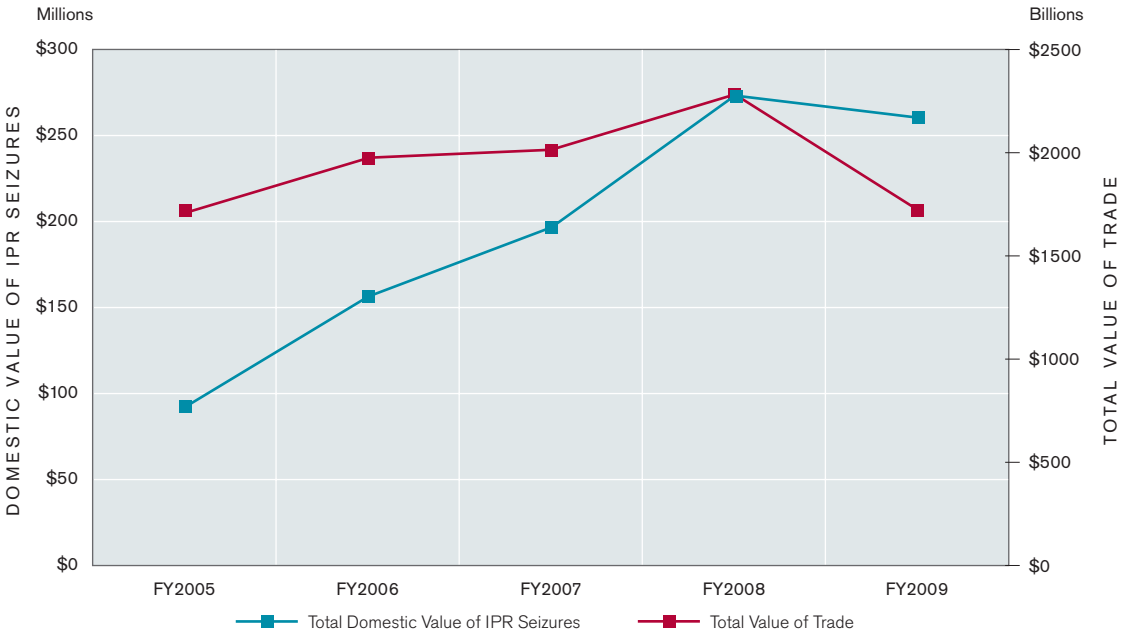
ANTI-COUNTERFEIT MEASURES AND PRACTICES

Over the past five years, there has been a dramatic increase in the numbers and types of counterfeit devices being sold in the aftermarket. Xilinx has taken decisive actions to protect its authorized supply chain and combat the spread of counterfeit materials. Like many semiconductor companies, Xilinx protects its trademarks in the United States and internationally.

Economic slowdowns, like any market parameter that reduces demand, can result in excess inventories of electronic components. It is not unusual in times like these to see some of this inventory diverted from authorized distribution channels into a "gray market" for subsequent sale by electronic component brokers and aftermarket resellers.

CASE STUDIES

Counterfeit Seizures in the U.S.



Recently, Xilinx has observed a rise in the electronic component gray market and Internet marketplaces, some of which may have connections with otherwise reputable distributors. While the gray market may offer short-term price advantages compared to authorized distribution channels, the quality and reliability of those parts cannot be assured. As there are no standards, controls, or records to verify proper storage and handling, Xilinx does not authorize the pass-through of its warranty for devices sold in unauthorized channels.

Xilinx invests significant resources and energy to ensure that reliable, high-quality components are supplied to customers. These standards of quality and reliability are maintained through exhaustive efforts internally within Xilinx, and formalized procedures and audits with our authorized distributors. The Xilinx warranty applies only to products purchased directly from Xilinx or its authorized distributors. A list of authorized distributors can be found at: *http://www.xilinx.com/company/sales/ww_disti.htm*

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Xilinx uses a unique traceability mechanism that deters device counterfeiting. On the newest generations of Xilinx components, a programmed internal code is used in conjunction with the device markings.

U.S. Customs and Border Protection, in partnership with trademark holders, has been identifying counterfeit materials at various points of entry. The table below shows areas with increased levels of counterfeit traffic. For a complete report from the U.S. Customs and Border Protection organization, please visit:

http://www.cbp.gov/linkhandler/cgov/trade/priority_trade/ipr/pubs/seizure/fy09_stats.ctt/fy09_stats.pdf

The chart on the previous page and the table to the right illustrate the intellectual property right (IPR)-related seizures for the U.S. ports of entry. Xilinx IPR seizures are included in the domestic totals.

SAFETY AND SECURITY FY 2009	DOMESTIC VALUE	PERCENT OF TOTAL
Pharmaceuticals	$ 11,026,260	34%
Electrical Articles	$ 4,317,499	13%
Critical Technology Components	$ 3,756,638	12%
Perfume	$ 3,709,303	11%
Sunglasses	$ 2,924,812	9%
Cigarettes	$ 2,578,415	8%
Batteries	$ 1,850,463	6%
Exercise Equipment	$ 833,724	3%
Personal Care	$ 819,167	3%
All Other Commodities	$ 615,516	2%
Total FY 09 Domestic Value	**$ 32,431,797**	
Total Number of Seizures	**1,543**	

* *2010 data will be published mid-2011. Please see http://www.cbp.gov/linkhandler/cgov/trade/priority_trade/ipr/pubs/seizure/fy09_stats.ctt/fy09_stats.pdf*

XILINX®

ENVIRONMENT, HEALTH AND SAFETY

Making a Positive Difference

Recognized as a technology industry leader, Xilinx is proud of its reputation for environmental stewardship and its commitment to healthy, safe workplaces for employees. The needs of the global community are carefully considered when designing company processes and products, and establishing goals, objectives, and performance measurement criteria. Xilinx business decisions are aligned with sustainability practices.

CASE STUDIES

QUALITY OBJECTIVES	KEY RESULTS IN 2010
Minimize the environmental impact of Xilinx devices	Xilinx 7 series FPGAs require 50% less power than previous generation
Be a socially responsible neighbor	REACH/RoHS* compliance – Substances of very high concern (SVHCs) added to Annex XIV of the regulation (authorization list): ▪ No listed substance is present in quantities over one (1) ton per year ▪ No listed substances are present in Xilinx devices above a concentration level of 0.1% w/w ▪ Xilinx complies with all necessary requirements (Article 7(2) and Article 33) of the regulation
Provide employees with a workplace free from occupational hazards	Successfully completed OHSAS18001 global audit along with re-certification to ISO14001

* *European Union's (EU) Registration, Evaluation and Authorization of Chemicals (REACH); Restrictions of Hazardous Substances (RoHS)*

Xilinx Code of Social Responsibility

The Xilinx Code of Social Responsibility guides day-to-day activities as well as business decisions. The key elements define the company's management principles, ethics, labor guidelines and policies, and environmental, health, and safety (EHS) programs. The commitment to this Code of Social Responsibility leads Xilinx to continually evaluate and improve its focus, and to strive to gain better leverage and investment returns in a challenging global economic environment. Ultimately, Xilinx's dedication benefits both shareholders and local communities where the company operates.

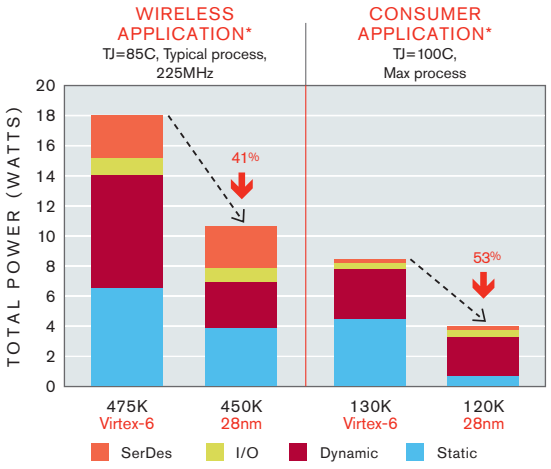
Highlights of accomplishments in 2010 include:

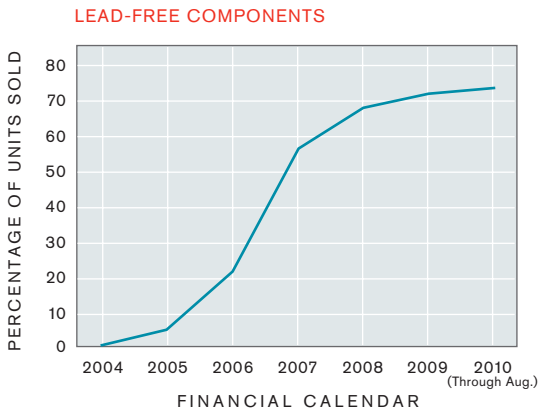
- ***Mitigation of carbon dioxide emissions:*** *Going back to 2005, Xilinx became a U.S. Environmental Protection Agency Green Power Partner and has since offset some carbon dioxide emissions each year with the purchase of Renewable Energy Credits (RECs). For every kilowatt hour of RECs purchased by Xilinx, an equal amount of electricity from renewable resources such as wind is being delivered to the electrical grid, helping to offset the need to generate electricity from other, more polluting sources.*
- ***Elimination of lead:*** *In 2010, almost 80% of Xilinx products sold were lead free, and the company continues to drive its Pb-free road map ahead of industry demands.*

CONT'D. >>

- ***Energy-efficiency:*** *Xilinx FPGAs are designed to meet a diverse set of application needs for automotive, broadcasting, consumer electronics, industrial, medical, test and measurement, video, wired and wireless communications, and other markets. Xilinx architectural and process innovations in 2010 resulted in the Xilinx 7 series 28nm FPGA family, reducing power by 50% while improving system performance by 50% or more.*

EHS PROGRAMS	MILESTONES & ACHIEVEMENTS IN 2010
Compliance	No fines or citations for breaches of EHS legislation in 2010
	Complete compliance with REACH/RoHS and China RoHS
Energy-Efficient Solutions	50% reduction in power and 50% increase in device performance by driving innovation in process selection, architectural design, fine-grain clocking, place-and-route algorithms, and device packaging
Material Composition	Almost 80% of Xilinx products sold are lead free, with expectations that the sale of lead-free devices will continue to grow. *(NOTE: Although removing lead from any single component results in a minute reduction in lead, sales of millions of lead-free parts results in a significant reduction of lead in the environment.)*
Material Minimization	Revolutionary 28nm Xilinx 7 series (Artix™-7, Kintex™-7, and Virtex®-7 families): ▪ Up to 3x increase in logic cell capacity ▪ 2x increase in transistor density ▪ More system functionality in smaller form factor (Artix has same functionality as Spartan®-6 but with a 50% smaller footprint) ▪ Unified architecture allows product migration across families as well as within a family, reducing board space, cost, and power
Health and Safety Management	Nurtured a Health & Safety culture within the company that fosters support, ownership, and accountability for the system by implementing OHSAS18001
	Expanded the EHS Internal Audit program to Xilinx Hyderabad





* *Benchmarks based on actual Virtex-6 customer designs*

SCALABLE DEVELOPMENT KITS

Xilinx Targeted Design Platforms let system designers increase productivity and minimize development costs. These programmable platforms provide simpler, smarter methodologies for creating system-on-chip solutions, speed time to market, and ultimately free designers to focus on innovation and differentiation.

The integration of FPGA devices, design tools, and IP into targeted reference designs that run on development or evaluation boards creates a robust development and run-time environment. The platforms help designers more quickly learn about FPGAs, and accelerate development with a variety of customizable tools and IP.

CASE STUDIES

Xilinx's relentless commitment to quality is evident in every layer of a Targeted Design Platform. Starting with the silicon, extensive verification and characterization drive repeatable processes that are aimed at zero defects. Methodologies pioneered to maximize results within fabless manufacturing are also applied to the production of Xilinx and partner software and IP. Extensive knowledge sharing and qualification processes have contributed to an industry-leading ecosystem that helps customers accelerate quality into every FPGA-based application.

Quality-centric design and integration methodologies allow Xilinx to offer customized base, domain-specific, and market-specific variations of our targeted design platforms that fully meet customer expectations. Quality standards for each layer benefit both hardware designers and software application developers.

Scalable development kits make it easy to order pretested, proven Targeted Design Platforms, including hardware, software, IP, and targeted reference designs. These fully integrated kits simplify evaluation and development with Xilinx FPGAs to maximize the value-added productivity gains and cost benefits and avoid the risks inherent in custom development system assemblies.

Xilinx evaluation and development kits provide a flexible, comprehensive environment for higher-level system design. Base development boards with industry-standard FPGA mezzanine card (FMC) connectors facilitate scaling and customization for specific applications and markets. Integrated tool suites streamline creation of systems solutions that adhere to complex design requirements. Preverified Targeted Reference Designs help to jump-start application development, and multiple design examples offer best practices for implementing system IP to optimize each unique application.

For a comprehensive list and the latest information on Xilinx and third-party development kits as they become available, visit: *http://www.xilinx.com/products/boards_kits/index.htm*.

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VIRTEX-6 KITS
Virtex-6 FPGA DSP Kit by Avnet
Virtex-6 LXT FPGA Characterization Kit
Virtex-6 FPGA ML623 Characterization Kit
Virtex-6 LXT FPGA ML605 Evaluation Kit
Virtex-6 LXT FPGA Broadcast Connectivity Kit
Virtex-6 FPGA Embedded Kit
Virtex-6 FPGA Connectivity Kit
Virtex-6 FPGA X8 PCI Express® Gen2 Kit

SPARTAN-6 KITS
Spartan-6 FPGA Embedded Kit
Spartan-6 FPGA Connectivity Kit
Avnet Spartan-6 FPGA DSP Kit
Spartan-6 FPGA SP623 Characterization Kit
Spartan-6 FPGA SP605 Evaluation Kit
Avnet Spartan-6 LX150T Development Kit
Spartan-6 FPGA SP601 Evaluation Kit
Avnet Spartan-6 LX16 Evaluation Kit
Avnet's Spartan-6 LX9 MicroBoard
Spartan-6 FPGA Broadcast Connectivity Kit
Spartan-6 FPGA Consumer Video Kit
Spartan-6 FPGA Industrial Ethernet Kit
Spartan-6 FPGA Industrial Video Processing Kit
Avnet's Spartan-6 / Intel Atom Development Kit