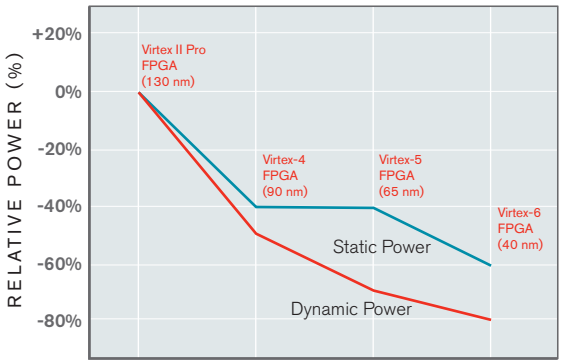
CASE STUDIES

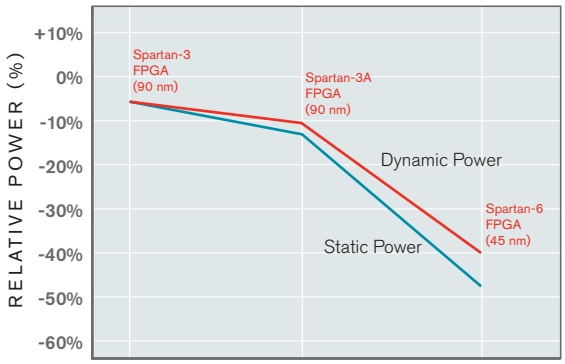
ENVIRONMENT, HEALTH AND SAFETY

Code of Conduct Extends Beyond Compliance

Xilinx is recognized as an industry leader committed to product stewardship, keeping pace with changing environmental regulations, and providing a healthy, safe and secure work environment for our employees. We believe that by serving as a responsible business, employer, and member of the global community, we strengthen our ability to deliver products in a manner which improves the quality of life.

QUALITY MILESTONES	KEY RESULTS
Provide Xilinx employees with a workplace free from occupational hazards	Obtained OHSAS18001 certification for Health and Safety Management Systems, adding to Xilinx Environmental ISO14001 certification
Minimize Xilinx environmental impact and be a socially responsible neighbor	Delivered next-generation Virtex®-6 FPGA and Spartan®-6 FPGA families with 50% less power consumption than previous generations
Maximize Xilinx shareholder value	Recognized among "100 Best Corporate Citizens" by CRO/Business Ethics Magazine for third consecutive year
	Asia headquarters in Singapore continues to receive numerous community awards, including ASEAN Energy Award and PUB Award in 2009





Xilinx Code of Social Responsibility

The Xilinx Code of Social Responsibility is founded on a participative approach to Environmental, Health & Safety (EHS) management that extends well beyond compliance. It fosters EHS as an element of everyday life, guiding key business decisions and day-to-day activities to ensure that our company and our customers gain better leverage and investment returns in today's challenging global economy. To this end, we have implemented a number of focused programs with systems and processes that are designed to produce tangible results while enabling us to actively serve our shareholders and the communities in which we live.

For example, we host company-wide electronics recycling events for Xilinx employees. We participate in the U.S. EPA Green Power Partnership Program, commissioned a study in 2009 to help us evaluate our carbon footprint, and have developed programs to further reduce our impact in 2010.

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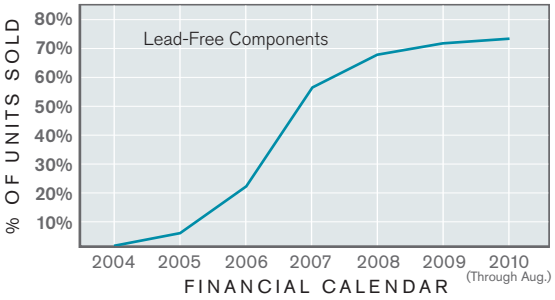
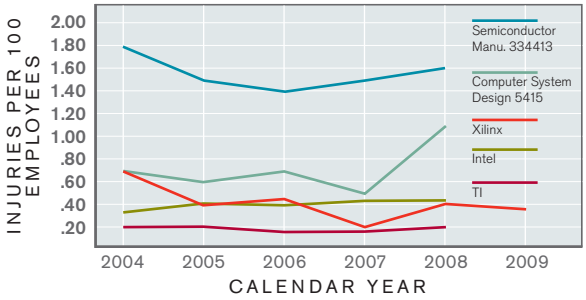
We take proactive steps to maximize the efficiency of our power usage, for which both our corporate headquarters in San Jose, California, and Asia-Pacific headquarters in Singapore have received awards. Each year, we offset nearly 700,000 pounds of carbon dioxide emissions through the purchase of renewable energy credits. We are delivering energy-efficient product solutions with lower-power FPGAs that also have simpler power system requirements. We work with our ecosystem partners to design and manufacture programmable platforms that are safe and friendly to the environment. In 2009, over 70 percent of the products we sold were lead free, and our Pb-free roadmap is driving toward complete Pb-free package availability in 2010 with the conversion of all packages by 2012.





AREAS COVERED	KEY STEPS & HIGHLIGHTS
Compliance	Comply with European Union RoHS (Restriction of Hazardous Substances) Directive, Reach Regulation (EC) No. 1907/2006, and China 'RoHS' No fines or citations for breaches of EHS legislation in 2009
Energy-efficient Solutions	Virtex-6 FPGA Family (40-nanometer): ▪ 30% lower static and dynamic power than previous generations ▪ Provides 15% lower power consumption with 15% higher performance than competing 40-nm FPGA offerings ▪ Enables design of 'greener' central offices and data centers Spartan-6 FPGA Family (45-nanometer): ▪ 50% lower static and 40% lower dynamic power on average than previous generations ▪ Built with lower power 1.0V core voltage option ▪ Reaches zero power with unique 'hibernate power-down' mode
Material Composition	Restrict use of lead, mercury, hexavalent chromium, cadmium, PBB and PBDE Complied with European Union R0HS directive (2002/95/EC) four years before regulation's effective date of July 1, 2006 ▪ Launched 'green' initiative in 1999 to design lead-free parts ▪ Removed lead for all devices by 2002*
Material Minimization	Led industry drive to reduce product size with 40-nm Virtex-6 FPGAs: ▪ 2X increase in transistor density ▪ Smaller, lighter FFG1156 package with mass of only 10.55 grams ▪ More system functionality in smaller form factor ▪ More hard IP to reduce external components and board size ▪ Single-chip solutions reduce board space, cost and power
Health and Safety Management	Certification to OHSAS18001 and ISO14001, and full compliance with legislative requirements in three major sites (San Jose, Dublin, and Singapore) Injury rate below industry average with goal for achieving injury-free work environment

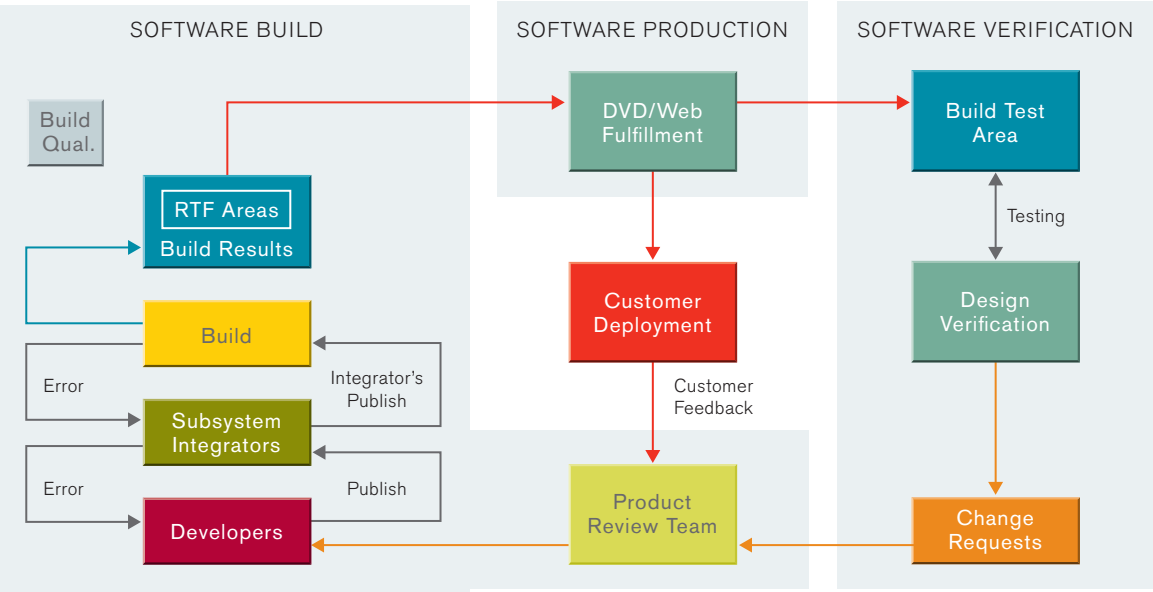
** Excluding flip-chip parts, which are compliant by exemption and contain under 0.2% lead by package weight*

CASE STUDIES

INTEGRATED SOFTWARE QUALITY

Designing Quality into the Development Process

Xilinx ISE® Design Suite Software Production System Architecture



Initiative Goal: Reduce Build Cycle for Software Products From 10 Days to 1 Day

QUALITY MILESTONES	KEY RESULTS
Technology and related methodology to accelerate build process and improve repeatability/stability of releases	Implemented series of process, tools and infrastructure improvements to reduce build convergence time to 1 day from 10 days
IT infrastructure with network and hardware configuration optimized for targeted results	Integrated software build process to deliver all ISE® products in 24-36 hours worldwide
More upfront effort to qualify code coming into integrated build across worldwide development and testing organizations	Quality issues found prior to code check-in and system integration for quicker feature implementation and higher release quality
Seamless transition ensuring that process and solution changes do not create disruption or add work for developers	Increased scalability of system to maintain consistent turnaround times with larger software code builds and device files
Easy-to-use and informative metrics system for driving continuous improvement	26% reduction in customer-generated change requests

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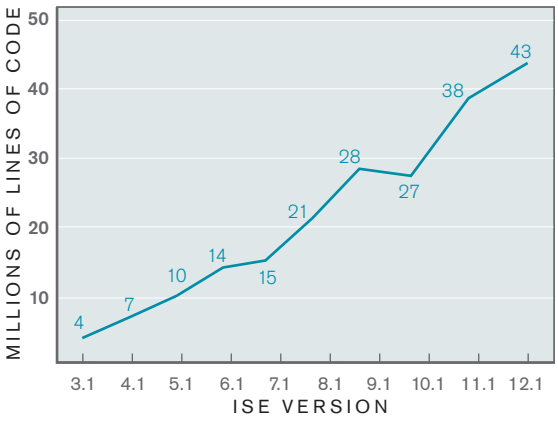
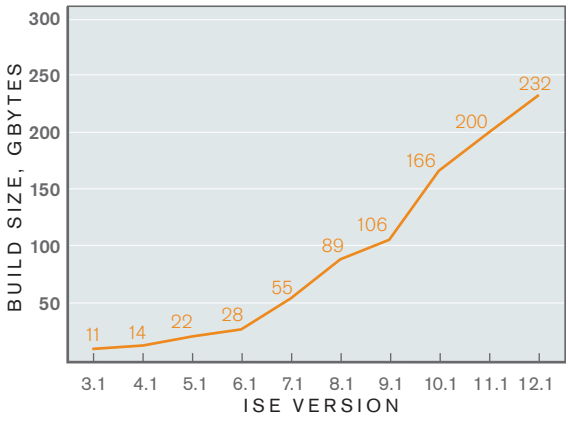
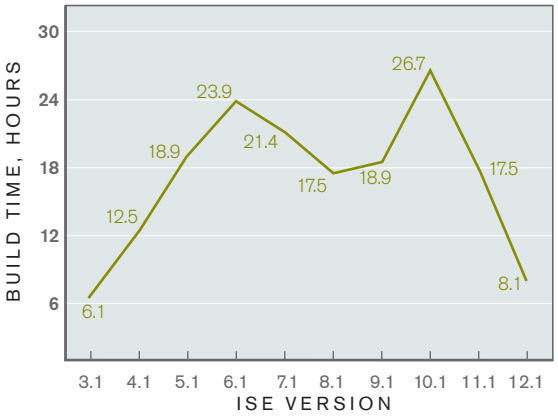
Early feedback is one of the keys to improving the development process and creating products with higher levels of quality. We have learned that the key to improving bug-find-fix cycles was tied to how quickly we could build and deliver clean builds to our developers and testers around the world. We resolved these issues using high-performance automated make technology in combination with network infrastructure improvements.

AREAS COVERED	KEY STEPS
Find solution to fix compile time issues	Use of available parallelization technologies
	More efficient use of filer technologies to avoid redundant read/write in builds
	Utilize information from previous builds
	Improve methodologies for conducting Windows OS-based builds
Address the IT infrastructure problem	Create an insulated build network
	Reduce traffic between various components of the build system
Review development process by introducing new feedback cycles	Add weekly clean branch builds from the biweekly builds
	100% increase in rate of integration builds
Create better workflow integration	Bring multiple ISE software build components together as one integrated build even when using separate processes
	Implement customized workflow integration tool

Scaling for Code Growth: Xilinx ISE Design Studio Suite





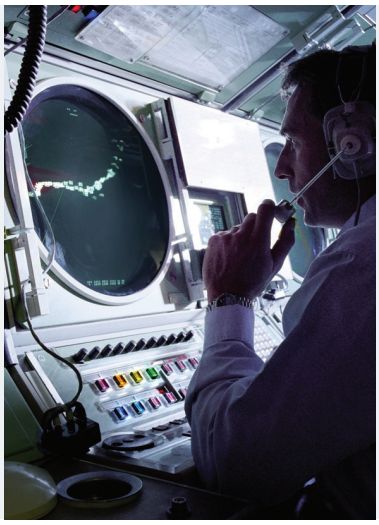


- In spite of increasing code requirements impacting build size and complexity, we have been able to reduce the overall build time, and expect to continue this trend.
- By using specialized suites of design inside the daily development flow, many more issues can be resolved now prior to integration and build, thus simplifying the resulting product.

CASE STUDIES

DRIVING TOWARD ZERO DEFECTS

Customer Success = Xilinx Success



Xilinx has a long legacy of delivering high-quality products and support to developers of automotive, aerospace and defense, and medical electronics. To meet the stringent requirements of these and other demanding markets, Xilinx offers customers access to a quality-driven infrastructure that is designed to provide defect-free product experiences. While this takes a tremendous level of focus and partnership, the rewards can be extraordinary. Xilinx remains committed to this mission and the belief that customer success is the ultimate metric for our own success.

PRODUCT QUALITY FOR LIFE	QUALITY IMPLEMENTATION
Design for quality and reliability	Design-for-manufacturability (DFM) and design-for-test (DFT) methodologies
Manufacturing readiness	Metrics for engineering samples and production units
	Defect density, line yield, assembly yield, test coverage, test yield, qualification
New product evaluation (NPE) and new product introduction (NPI) compliance	Design tapeout release
	NPE/NPI checklists
	Hard production review and release criteria
Organize to drive new product introduction	Functional organization alignment
	Global integration of QA & NPI engineering

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QUALITY MILESTONES	KEY RESULTS
Eliminate defects for customer applications	Shipped over 11.4 million units with zero PPM for high-volume consumer application
	Other customers achieving similar results
Address manufacturing variability	Manufacturing corner material available for better qualification of customer designs*
Improve robustness of qualification efforts	Passed PURE audit in October 2009: ▪ Met AEC-Q100/101/200 stress test requirements ▪ Qualified as FPGA vendor at all locations and divisions for SAAB, Thales, Hispano-Suiza (Safran Group) and CNES
	Automotive "XA" products successfully qualified to AEC-Q100 and beyond
	Aerospace & Defense "XQ" products successfully passing MIL-STD883 or MIL-PRF-38535H

** To learn if your company qualifies for this program, contact the Xilinx quality team at: wwcqe@xilinx.com*

High-volume customer applications can achieve zero defects. Xilinx has proven this repeatedly through structured customer collaboration. This disciplined approach leverages the synergy between Xilinx and our customers through joint design reviews, manufacturing corner material, and focused teamwork. This collaborative effort often involves a commitment to support contract manufacturers. We believe this process delivers superior results and creates a valuable advantage in working with Xilinx.

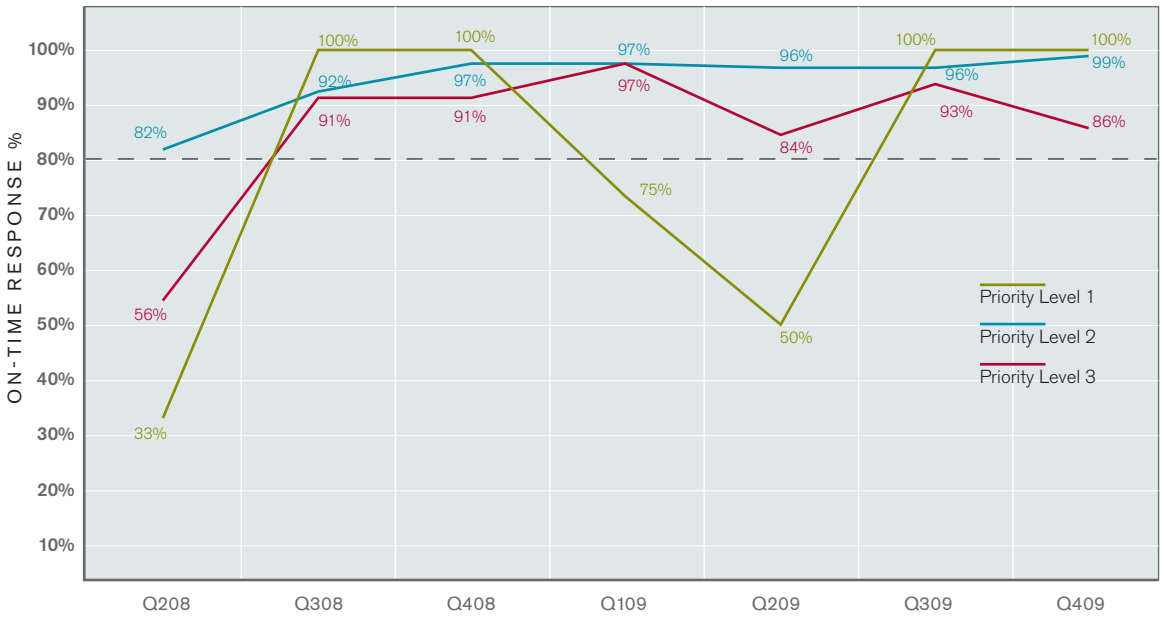
AREAS COVERED	KEY STEPS & HIGHLIGHTS
Collaborate during early development process	Validate interoperability
	Build final bill of materials
	Create and validate customer design
	Initiate and verify prototype build
Quality training to aid the design process	Online training focused on improving design margin
	FPGA Design Quality Checklists to avoid common mistakes*
	FAE support to drive best practices
Reduce/eliminate in-line manufacturing issues	Work closely with contract manufacturers to: ▪ Increase troubleshooting capabilities and signature analysis ▪ Address common manufacturing issues such as electrical overstress damage ▪ More direct customer involvement

** For more information, visit: http://www.xilinx.com/products/quality/fpga_best_practices.htm*

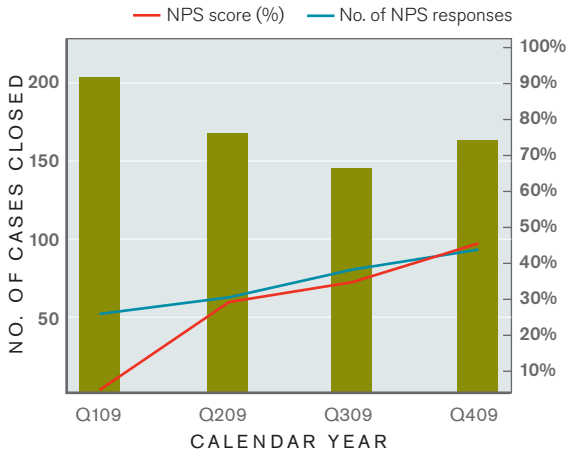
CASE STUDIES

PRODUCT QUALITY ENGINEERING

Executing for Best Customer Experience



QUALITY MILESTONES	KEY RESULTS
Reduce customer returns through proactive engagement	21% reduction in RMAs 2009 vs. 2008
Strive for on-time response % commitment 80% of the time for all priority cases while focusing on best customer experience	Exceeded target goal in 2nd half of 2009 ▪ 100% on Priority Level 1 cases ▪ >96% on Priority Level 2 cases ▪ >86% for Priority Level 3 cases
Use of improved RMA processes for rapid case resolution	Impressive increase in net promoter score (NPS) every quarter of 2009 ▪ From 0% in Q109 to 45% in Q409



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KEY STEPS	AREAS COVERED
Providing quality solutions	Smooth and seamless hand-off process for silicon through application issues
	Proactive relevant data/case information collection
	Hardware and design tool readiness
Early PQE engagement with NPI team	Virtex-6 FPGA and Spartan-6 FPGA early engagement
	Acquire knowledge on silicon issues and fixes from tapeout to production
	Rapid learning curve in resolving new product quality issues
Improved RMA processes	Return Materials Authorization Quality Issue Management System (RMA QIMS)
	QES (RMA Quality Escalation System) and best practices deployed globally to capture and escalate quality issues in timely manner

When there is a need to assess potential quality problems, contain risk, and ensure uninterrupted production processes, customers require a timely response and a clear root cause.

At Xilinx, we take this obligation seriously by engaging customer issues early using FAEs, diagnosing problems through rigorous case review, appropriately assigning case priority to meet customer urgency, and ensuring customers are kept informed through real-time updates through our online RMA portal.

Since 2008 Xilinx has set and achieved cycle time targets for RMA cases based on customer need. Using on-time delivery metrics we have been able to improve our capabilities and ensure a more predictable response. Our customers have recognized this improvement through increases in our net promoter score (NPS) throughout 2009.

Going forward, we will be making further improvements in how we handle RMAs to identify issues earlier and speed customer response in 2010.