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XILINX
INNOVATION

IP QUALITY

Improving Customer IP Experience

Xilinx IP and development tools enable customers to accelerate the development of innovative products. The goal is to give designers a predictable, trouble-free experience with every Xilinx product. As a result, Xilinx implemented a number of architecture, process, test, and development improvements in 2012 to raise the quality of Xilinx ISE® and Vivado™ design tools, and to meet increasingly stringent customer IP expectations. Vivado integration with IP not only allowed Xilinx to optimize the overall design tools testing, but provides the following benefits to customers:

- *A unified interface for improved testing and a more predictable IP experience*
- *Single point of access to the Xilinx IP portfolio*
- *Faster synthesis and implementation times, facilitating more design turns*
- *Predictable and reproducible results using a powerful Tcl ("Tickle") interface*
- *Ease of migration from inconsistent and incompatible legacy flows (CORE Generator™ vs. EDK, for example)*

With Vivado integration, Xilinx has also enhanced its IP release criteria and convergence process to ensure a more-timely handling of defects and enhancement requests. Intuitive dashboards and detailed checklists are routinely reviewed to drive quality. A key focus area is customer-critical change requests. Xilinx aims to respond to all critical-level requests within three working days; all internal change requests are now independently verified within two weeks after being fixed. A new two-week verification window for change requests has minimized delinquent (verified and assigned) IP change requests.

Xilinx has introduced stricter control on its convergence process, which offers a balance between development agility and minimized risk. This has led to more change requests being fixed earlier, before final release phases *(see Figure 1)*.

Together, these efforts have resulted in a more predictable, error-free target customer IP experience.

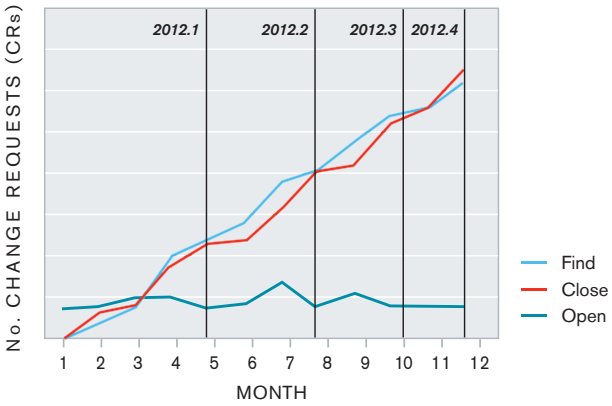

Figure 1. Horizontal and Embedded IP Change Request (CR) Trend:
Zero Defect Initiative and resulting low numbers of open change requests

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Zero-Defect IP Mindset

Driving to "zero defects" is not restricted to silicon. This engineering mindset is at the core of the Xilinx IP development process. As reported in 2011, IP quality improvement efforts started with the goal of reducing customer-triggered defect reports by 10%. After years of effort and an extensive overhaul of the IP development and testing infrastructure, Xilinx has achieved a reduction of more than 33% in customer-triggered IP defect reports. In 2012, Xilinx upheld the same goals, even with the expanded product portfolio, more-complex and higher-value IPs, and support for two design flows (ISE and Vivado). The efforts that went into the continued improvement of IP quality include:

- *Increased testing year after year to keep up with increased volume of IP*
- *Maximized functional coverage for interactions among processor, logic, and IP by including partners and using real-world systems for testing; IP pass rates are tracked for customer designs even in beta cycles*
- *New system-level validation, extended IP testing, and increased hardware validation during system-level testing*
- *Availability of development boards to allow earlier validation of silicon*

Xilinx and its technology suppliers, partners, and customers form a very interdependent community that collectively contributes to IP quality. Xilinx has earned the trust of its partners by driving up the quality of the overall solution as well as the quality of the devices. Besides in-house efforts, comprehensive evaluation by and feedback from the Xilinx Alliance partners are part of the release process for Xilinx tools and IP:

- *7 series devices, tools, and IP testing leveraged the ecosystem during testing and qualification; partners were invited in earlier and became more involved in the process than they did at previous generations.*
- *Real-time debugging (Vivado beta) was carried out by ecosystem partners:*
  - *Partners used their own IP/designs to exercise Vivado and uncover errors earlier.*
  - *An extended testing period enabled higher-quality results and led to increased numbers of first-time successes.*
- *The annual partner qualification requirements were expanded to cover Zynq™-7000 and Vivado expertise, and to promote quality at all levels of the ecosystem.*

PROGRAMMABLE 3D ICs

XILINX INNOVATION

To date, each new generation of FPGAs has followed Moore's Law, doubling logic capacity every 18 months to two years, while cutting costs by half. However, as the role of the FPGA migrates toward the heart of the system, designs are growing larger and more complex. This phenomenon calls for higher logic capacity and more on-chip resources. Designers who want the benefits of programmable silicon technology for their most advanced electronic systems are finding that their designs require more resources than are available in the largest monolithic FPGAs. Moore's Law no longer keeps up with accelerating market requirements.

In response, Xilinx has developed an innovative approach for stacked silicon integration that employs microbumps and through-silicon vias (TSVs) to integrate multiple FPGA die slices placed side-by-side on a passive silicon interposer.

3D Packaging

As the interconnect density continues to shrink, and the cost of fabricating finer-pitch substrates increases, flip-chip packaging with the conventional organic buildup substrate is facing a major challenge related to fine-pitch wiring. TSV interposer technology has emerged as a good solution, providing high-wiring-density interconnects, minimizing coefficient of thermal expansion (CTE) mismatch between the copper/low-k die and the copper-filled TSV interposer, and improving electrical performance due to shorter interconnects from the chip to the substrate.

Stacked Silicon Interconnect Technology (SSIT)

Since the advent of integrated circuit technology in 1958, the industry has focused primarily on monolithic integration. Unfortunately, due to physical and economic issues, the vast majority of high-performance analog chips, high-performance digital chips, and high-density memory chips are each built on separate technologies. Therefore, in order to deliver optimum system performance, power, and cost, it is desirable to integrate multiple different die, each using its own optimized technology, in a single package.

For multi-die implementations, Xilinx optimized system performance by integrating digital FPGA die and separate high-speed analog SerDes die on a silicon interposer. The underlying interposer technology allows up to 10,000 interchip connections with signaling power levels approaching intra-die connections. The industry's first homogeneous SSIT device, the Xilinx Virtex®-7 2000T, is a major milestone, with:

- *Four-layer metal Si interposer with TSV*
- *Four FPGA sub-die, with 10,000 inter-die connections*
- *6.8B transistors; 2M logic cells*
- *2,000 BGA balls, 20,000 C4 bumps, and 200,000 microbumps*

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3D Integration and Scalability

The XC7VH580T is the first commercial FPGA built with heterogeneous SSIT, and is the first in a family of three FPGAs with 28Gbps transceivers. The device consists of a passive silicon interposer and three active die: an 8 x 28Gb/s transceiver IC (GTZ-IC) and two FPGA ICs known as Super Logic Regions (SLRs). *(See Figure 1.)*

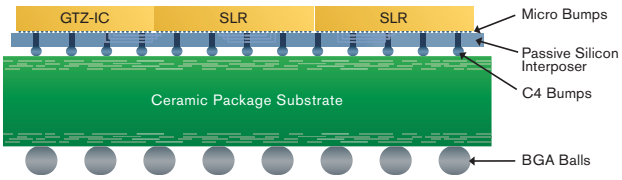

Figure 1. Conceptual Cross-Section, XC7VH580T: *An organic package with 180µm-pitch C4 bumps enables a high-performance logic package with Cu TSV interposer.*

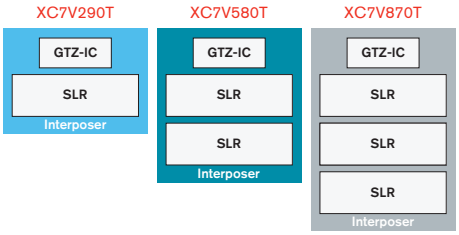

Figure 2. Bird's-Eye View, Scalable FPGAs (not to scale): *SSIT integrates multiple FPGA slices side-by-side on a passive silicon interposer. Thousands of die-to-die connections (passive traces fabricated on the silicon interposer) provide high connectivity and low latency (~1ns) without incurring the power penalty of traditional I/O structures.*

Two additional products are derived from these building blocks: the XC7VH290T with one fewer SLR, and the XC7VH870T with one additional GTZ-IC and one additional SLR. *See Figure 2.* The XC7VH870T consists of sixteen 28Gbps transceivers and seventy-two 13.1Gbps transceivers, which allows the delivery of the previously unattainable bandwidth of 2.78Tbps.

TSV Interposer Reliability

As in a standard flip-chip package, due to the CTE mismatch between interposer and substrate, the interposer undergoes global stress. Inside the interposer, copper TSV expands at a different rate than the bulk silicon and because of this, applies additional local stress on the area surrounding the copper via. Therefore, Xilinx carefully studied interposer stress and delamination risk through simulation and actual thermal cycling. Simulation results indicated that the overall stresses (global and local) in silicon, silicon-oxide oxidation, and copper via are below fracture toughness of these materials, and there was no delamination or fracture risk for the interposer. Actual reliability data confirmed these findings.

STRESS	CONDITIONS	STATUS
HTOL	T_J=125°C, V_{CC}max, Dynamic	✓
THB	MSL4: T_A=85°C, RH=85%, Alternated Bias	✓
HTS	3x reflow: T_A=150°C	✓
TC	MSL4: -55°C/+125°C	✓
PC	3x reflow Ramp up: 30°C to 130°C in 3 min. Hot Dwell: 6 min. at 127°C to 130°C Ramp down: 130°C to 30°C in 3 min. Cold dwell: 27°C to 30°C	✓
ESD and Latch Up	▪ HBM: ANSI/ESDA/JEDEC JS-001 ▪ CDM: JESD-22-C101 ▪ Latch-up: JESD-78 (±200 mA and 1.5 x VDD at 125°C)	✓
BLR	0 to 100°C: 10 min. ramp and 10 min. dwell	✓

The impact of moisture and temperature cycling on the microbumps, TSV integrity, and adhesion of the underfill to the top FPGA die and the thin TSV interposer were studied. Samples were subjected to HTOL, Level 5 preconditioning, and thermal cycling (TCB). All the samples were tested and passed opens and shorts after every read point. C-SAM was also performed after 1,000-cycle TCB and no delamination was found.

Table 1. SSIT 3D Packaging Qualification Stress Tests Passed Successfully: *Many DOEs and prequalification using die from the previous process node allowed Xilinx to break through the limitations of monolithic FPGAs; SSIT enables super-high-capacity FPGAs with unmatched chip-to-chip bandwidth and the highest quality.*

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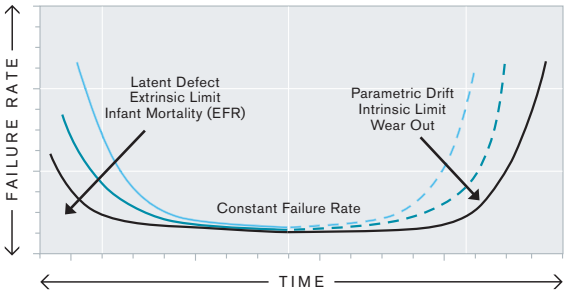
20nm READINESS

XILINX INNOVATION

As with any generation of technology, the key to a successful product is to understand the challenges and weaknesses early in the development cycle. Doing so requires the ability to prove the fundamental building blocks as well as the process match with the design technology. Over the past 25+ years of technology development, Xilinx engineers have overcome each generation's unique challenges including pushing beyond the limits of Moore's Law to meet the latest demands for power, performance, and features. Solutions to these problems drive constant innovation in design, device lithography, verification, testing, and reliability.

IC Reliability: Increasingly Important

The future of CMOS hinges on the rapidly evolving, high-volume consumer markets such as mobile communications. Within these markets the IC reliability margin is shrinking, as illustrated by the "shrinking bathtub" curve *(Figure 1)*. Reliability at the product or system level requires application and use conditions where a "one-size-fits-all" reliability FIT calculation may no longer be optimal. A new approach to design for reliability (DFR) is required to support IC scaling without lowering the reliability of electronics systems.



- Extrinsic Limit Infant Mortality (EFR)
  - Defect reduction
  - Outlier elimination
  - Electrical voltage stress screens
- Intrinsic Limit Wear Out
  - Realistic use condition
  - Appropriate model
  - Design for reliability
  - Longer / newer tests

Figure 1. Shrinking Bathtub: *High-volume consumer markets such as mobile communications are shrinking the IC reliability margin. By focusing on design reliability, Xilinx has been able to deliver and meet the reliability requirements at 28nm and will continue to drive this area at 20nm.*

Xilinx DFR Methodology

In preparation for 20nm, Xilinx methodology includes evaluating intrinsic (DFR, reliability guardband) and extrinsic limits (defect reduction and outlier elimination). As appropriate, reliability design budgets were established, or guardbands were added, to the production test program to address post-stress degradations *(see Figure 2)*.

	VMIN			NOM	VMAX		
Vccint	0.93	0.95	0.97	1.00	1.03	1.05	1.07
Vccint (LV)	0.83	0.85	0.87	0.90	0.93	0.95	0.97
Vbram	0.93	0.95	0.97	1.00	1.03	1.05	1.07
Vccaux(s)	1.67	1.69	1.71	1.80	1.89	1.91	1.93
VccIO(s)	1.67	1.69	1.71	1.80	1.89	1.91	1.93
VccADC	1.67	1.69	1.71	1.80	1.89	1.91	1.93
VccBATT	0.96	0.98	1.00	1.50	1.98	2.00	2.02
MGTAVCC	0.93	0.95	0.97	1.00	1.03	1.05	1.07
MGTAVTTRX	1.13	1.15	1.17	1.20	1.23	1.25	1.27
MGTAVTTTX	1.13	1.15	1.17	1.20	1.23	1.25	1.27
MGTAVTTRCAL	1.13	1.15	1.17	1.20	1.23	1.25	1.27
MGTAVCCAUX	1.67	1.69	1.71	1.80	1.89	1.91	1.93

Figure 2. *Production guardband methodology has always been part of Xilinx DFT and DFR. This table illustrates the continuation at 20nm.*

NOM
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CLASS
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Reliability Estimator

The Xilinx Reliability Estimator (XRE) tool was developed to help customers estimate the reliability performance for Xilinx 7 series products, and has been extended for 20nm. Designed from the ground up, the calculator estimates the failure rates (FITs) for various customer-specified use conditions and durations *(see Figure 3)*. The fundamental concepts of the XRE tool include:

- *Separating the chip into small components according to their characteristics and applications*
- *Calculating the failure rate of each component using a reliability aging model*
- *Summing up the failure rate of each component to calculate the failure rate of the chip*
- *Taking into consideration the reliability physics for gate oxide, transistor, and interconnects, as well as:*

– *Design characteristics (voltage, current, area, complexity)*

– *The physics of failures: wear-out (BTI/HCI, TDDB, EM) data from foundries*

– *Parametric drift (BTI/HCI) data from CAD simulations, mitigated with test guardband data*

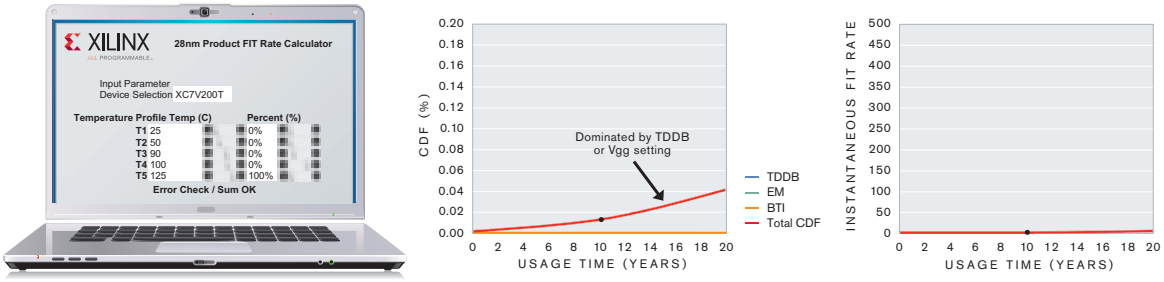

Figure 3. Example of 28nm FIT Rate Calculation: *The XRE tool takes into consideration the reliability device physics, along with the appropriate models and customer profiles to calculate an accurate FIT rate.*

For additional information, contact your local customer quality engineer (CQE) or sales representative.