VERIFICATION AND CHARACTERIZATION

XILINX QUALITY

Verification and characterization (V&C) activities are the cornerstone of the Xilinx New Product Introduction (NPI) process *(see Figure 1)*. The Xilinx NPI process was established and refined over the last three generations of Xilinx technology, culminating in our 28nm products, which include our Zynq™-7000 devices with dual-core ARM® Cortex™-A9 processing system (PS).

Xilinx V&C ensures that products operate over the specified voltage and temperature ranges. V&C starts with building in sufficient margin in the design phase, which is then validated during simulation prior to product tapeout. Critical circuits are verified using test vehicles. Finally, production-ready product quality is characterized based on the datasheet and Xilinx IP across all process corners, voltage, and temperature (PVT) combinations. The data is used to evaluate product performance against the published datasheet and established production test margins. Scope-of-performance validation includes hardened IP as well as the design tools needed for performing power estimations and static timing analysis for application logic in the fabric.

Figure 1. *NPI process integration with product life cycle*

Key characterization activities include:

- *Performance validation over process corners, to check for margin over PVT for manufacturability*
- *Comprehensive attributes, with sweeps above and below default settings to confirm margin and highlight sensitivities to PVT, with higher focus on applicable MGT, BRAM, and MMCM*
- *Improved dynamic power characterization to better isolate specific power blocks, with extensive validation of Xilinx Power Estimator (XPE) and Xilinx Power Analyzer (XPA) models over toggle rates and PVT*
- *DC characteristics over recommended operating conditions (HR I/O banks)*
- *FPGA logic and clocking switching characteristics for all speed grades*
- *Configuration switching characteristics*
- *GTX transceiver transmitter switching characteristics*
- *SSO with signal specification (see Figure 2)*

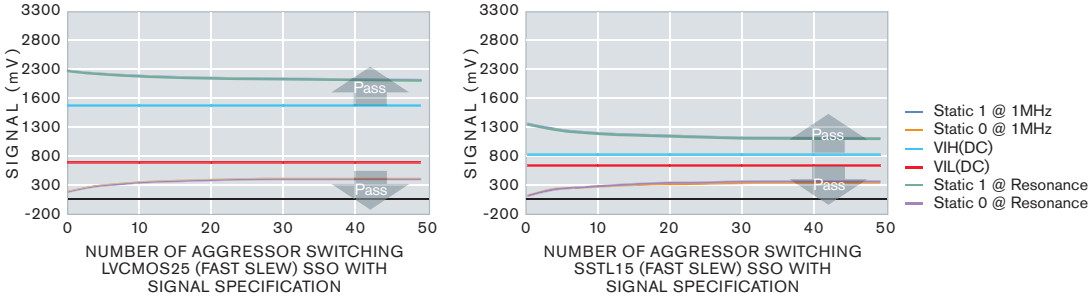

Figure 2. SSO Data: *With package complexity, SSO characterization data validates Xilinx simulation methodologies that contribute to packaging design.*

CONT'D. >>

V&C efforts also focus on evaluation of timing paths within the FPGA fabric, as well as hardened complex logic IP blocks on silicon and other functional IP. These are all key for meeting specifications and customer design targets.

The following steps depict the key milestone criteria prior to release of characterization reports and product specifications *(see Figure 3)*:

- *Test patterns for all blocks, during both automated and bench testing*
- *Verifications of full functionality across speed, process, and temperature*
- *Power and performance verifications, corner cases, and system testing*
- *Volume automated test equipment (ATE) characterization*

This work culminated in a deep understanding of FPGA capabilities needed for Targeted Reference Designs (TRDs). Customers facing the challenges of increasing complexity and increasing competition use Targeted Design Platforms, preverified system platforms, to significantly reduce design cycle times.

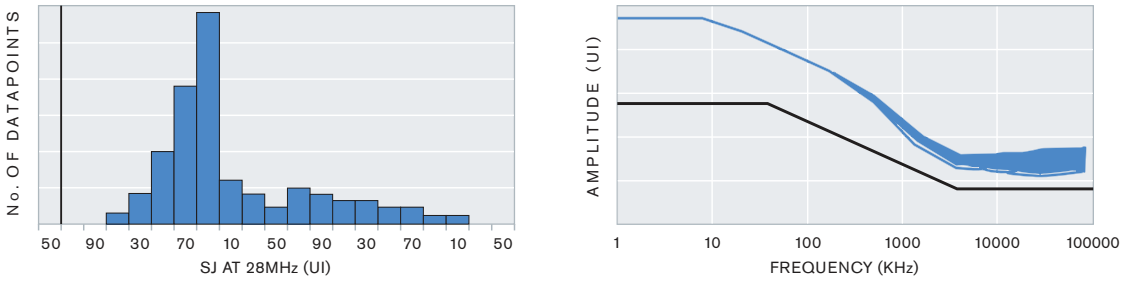

Figure 3. Sample Characterization Report: *With every product release, Xilinx publishes characterization reports that validate product datasheet specifications and give customers a better understanding of Xilinx methodologies and techniques.*

System-level testing is increasingly important to achieve this goal out of the box. Exhaustive (>50M data points) characterization ensures accuate datasheet specifications, and verifies supporting documentation, which ultimately facilitate more robust designs. Xilinx is uniquely able to leverage a long history and real-world experiences with telecommunication, wireless, automotive, consumer, aerospace and defense, and medical applications to define and carry out extremely stringent system-level testing. In the process of developing TRDs for Zynq-7000 devices, for example, Xilinx thoroughly researched the co-development of hardware and software. By staying ahead of customers, Xilinx is able to extend the same level of quality that characterizes Xilinx hardware into the realms of system software.

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PRODUCT QUALITY AND FAILURE ANALYSIS ENGINEERING

At Xilinx, we've proven that achieving a high standard of quality is no accident. It is a result of the relentless drive to discover root causes of failures. The efforts of both internal engineering and customer teams enable discoveries that in turn increase the true understanding of Xilinx products and services, which translates into very real, bottom-line benefits to customers. *(See Figure 1.)*

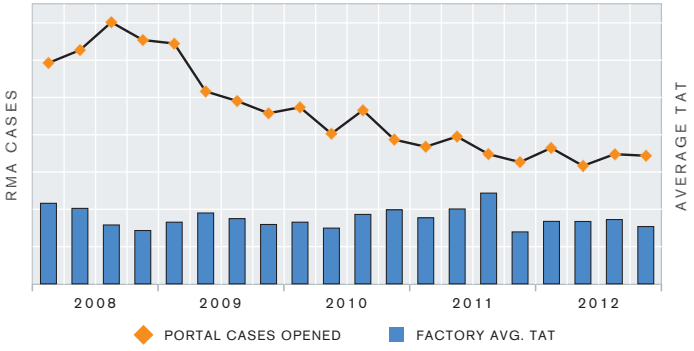

Figure 1. *Year-over-year reductions for returned material authorizations (RMAs) have resulted from closed-loop root cause analysis with customers.*

PROCESS TECHNOLOGY	DEVICE HOURS AT T_J = 125°C	FIT
28nm	495,908	17
40nm	1,623,961	16
45nm	1,223,275	10
65nm	2,722,938	15
90nm	10,819,831	5

Figure 2. *FIT rate by process technology, clearly demonstrating that Xilinx design approach DFT and DFR methodologies are yielding extremely reliable products.*

This achievement is accomplished through a focus on die, package, and test-level defect reduction initiatives. At the same time, through continuous improvement, our product improvement and reliability monitor programs continue the preventive drive to ensure world-class field quality. The success of this effort can be seen both in the line quality measured at customer sites and in the low FIT rates *(see Figure 2)* published quarterly on the web in the Xilinx reliability report (UG116).

Type	Classification	Geometry	Fab Site	Q1 HTOL	Q1 DRB	Q1 HTOL	Q1 DRB	Q1 HTOL	Q1 DRB	Q1 HTOL	Q1 DRB
FPGA	≤ 4 Year Process	*0.028uμ	TSMC								
		0.045uμ	SAMSUNG								
		0.04uμ	UMC12A								
	> 4 Year Process	0.065uμ	TOSHIBA								
			UMC12A								
		0.09uμ	TOSHIBA								
			UMC12A								
		0.13uμ	UMC12A								
		0.15uμ	UMC12A								
			UMC8C								
		0.18uμ	UMC8D/F								
		0.25uμ	SE-TOHOKU								
			UMC8C								
SoC	≤ 4 Year Process	0.28uμ	TSMC								
PROM	> 4 Year Process	0.35uμ	UMC8A/B								
CPLD	> 4 Year Process	0.18uμ	UMC8E								
		0.35uμ	UMC8A/HJ								

Package Family	Package Type	Assembly Site	Q1 THB / HAST	Q1 TC	Q1 AC / μHAST / TH	Q1 HTS	Q2 THB / HAST	Q2 TC	Q2 AC / μHAST / TH	Q2 HTS	Q3 THB / HAST	Q3 TC	Q3 AC / μHAST / TH	Q3 HTS	Q4 THB / HAST	Q4 TC	Q4 AC / μHAST / TH	Q4 HTS
FCBGA (*F/K/I substrate)	SSIT	TSMC																
	FC (Ceramic)	TSMC/ATK																
	FC (Bare Die)	SPIL																
	FC (LowK Process)	ATK/SPIL																
	FC	ATK/SPIL																
WBBGA (CU Wire)	Chip Scale	ATK/SPIL																
	PBGA	ATK/SPIL																
WBBGA (AU Wire)	Chip Scale	ATK/ATP/SPIL																
	PBGA	ATK/ATP/SPIL																
	SBGA	ATK																
WBLF (AU/CU Wire)	PLCC	ATP																
	PDIP	ATP																
	SOIC	ATP																
	TSSOP	ATP																
	MLF	ATK																
	TQFP/VQFP	ATK/ATP/SPIL																
	PQ(G)	ATK/SPIL																

Figure 3. Xilinx Monitoring Programs *continue to evolve from previous generations to improve sampling for the Process and Package Monitor Programs (colors represent specific tests).*

CONT'D. >>

The Xilinx 28nm portfolio introduces various new technologies such as 3D packaging and ARM® processor subsystems. Reliability monitoring was expanded and modified to include dedicated sampling addressing these new technologies *(see Figure 3)*.

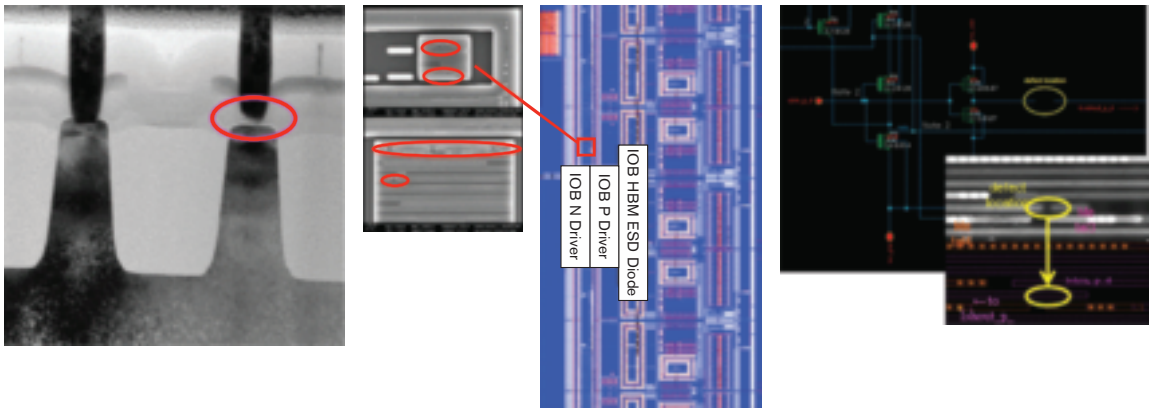

Figure 4. Examples of Failure Analysis: *Xilinx continually invests in new failure analysis equipment and techniques to enhance root-cause analysis and drive the appropriate process improvements.*

To build reliable products requires a deep understanding of the technology. By investing heavily in top-of-the-line analysis tools and equipment, Xilinx promotes:

- *Yield improvement analysis*
- *Diagnostics on production in-line failures (see Figure 4)*
- *Support for Reliability Engineering practices*
- *Assisting customers to help them improve their processes, product qualification, and issue resolution*

Xilinx failure analysis capabilities span all devices and components as a standard part of the New Product Introduction (NPI) process. After products are released to production, technical evaluations and root-cause identification of failures continue to improve reliability and prevent future failures, thereby improving the performance of Xilinx products and processes over time. Technical data is also provided to assist customers with failure root-cause determination.

At Xilinx, product engineering is continually developing new tools and expertise to debug any device issues, including those relating to the Zynq™-7000 SoC and 3D packaging technology. Virtex®-7 3D ICs, with increased FPGA density and more on-chip functions, pose diagnostic complexity because of the >50,000 chip-to-chip connections. With FPGA programmability, this challenge is overcome by intelligent debug scripts to test every connection.

The Zynq-7000 poses similar complexity issues, which are again addressed with on-chip diagnostics. The programmable-logic diagnostics use DFT methodologies and use various configurable FPGA resources. To ensure products work as specified, the processor subsystem is equipped with approximately 400,000 scan cells that are structurally tested to detect at-speed transition faults and stuck-at faults. On-chip memory and caches are analyzed using memory built-in self-test (MBIST) techniques.

For more information about quality, reliability, verification and characterization, please contact your local customer quality engineer (CQE) or sales representative.

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WORLD-CLASS TEST COVERAGE FOR ABSOLUTE QUALITY

XILINX QUALITY

"If you can't test it, then don't design it." This is the mandate from Vincent Tong, the executive vice president of quality and new product introduction at Xilinx. To comply, Xilinx design engineers place priority on the ability to detect problems quickly and identify root causes that enable solutions. The Xilinx approach starts with design-for-test (DFT) methodologies and the New Product Evaluation (NPE) process, and extends throughout the complete product life cycle.

Design for Test and Test Coverage

Xilinx continuously improves the test coverage of its products by implementing various DFT methods *(see Table 1)*. These techniques span digital logic, IP, memory elements, I/O boundary scanning, and many other areas. Recent improvements include achieving the highest test coverage, and are measured against PPM results from customer returns that are published on www.xilinx.com. Xilinx 28nm products introduced a new level of DFT and built-in self-test (BIST), test methodology, patterns, and tools development, including:

- *Extended existing random and continuous testing*
- *Expanded data collection and test cases for verification and characterization (including system-level test)*
- *Known-good die testing at wafer sort, which is critical due to 3D slice density and yield*
- *Ability to select low-power products with our Xilinx methodology to meet customers' needs and ensure that Xilinx products meet published specifications*
- *Die selection, power die optimization, and performance to address the most stringent requirements (power vs. performance)*
- *Test methodologies for processor subsystem (PSS) and FPGA interaction, to meet performance, specification, and quality requirements*
- *Proprietary tools and BIST testing, for characterization and production test*

Test Coverage and Characterization

Excellent coverage and a redesigned characterization process allowed the launch of the Xilinx 28nm families with zero production errata. Circuits are tested for overall voltage, temperature, and frequency ranges. Learning on the Xilinx 6 series and early learning on the 7 series provided deeper collaboration and engagement sooner in the design stage. Yields consisting of 50x more samples with first silicon, along with greater access to engineering boards for verification and characterization, allowed the highest data collection across functional teams compared with previous generations. As a result, the 7 series exceeded 99% of target goals on time *(refer to main report for details)*, without any changes in specifications *(see Table 1)*.

CONT'D. >>

CIRCUIT UNDER TEST		PRIMARY FAULT TARGET AND TYPE	TEST METHODOLOGY	TEST COVERAGE METRIC
TYPE	EXAMPLE			
Digital Logic	Combinational and sequential circuits	Single stuck-at faults	Deterministic ATPG, LBIST and fault-graded functional vectors	Overall entire FPGA > 99%, individual IP blocks range from 98% to 99.9%
		At-speed transition faults	Deterministic transition ATPG or LBIST	80-92% depending on IP block
		Path delay faults	Path delay ATPG	First 500
IP	High-speed I/Os, e.g., SerDes and BER DDR	BER	PRBS loopback (both near end and far end for SerDes)	100% industry-standard testing
			PRBS loopback for DDR, embedded BERT, Tx to Rx internal parallel loopback	100% industry-standard testing
	PLL	Jitter, frequency	Embedded BIST	100% functional test
	Mixed-signal IPs	Analog defects (no digital type of defects)	Functional vectors or functional BIST	100% functional test
Memory elements	Embedded memory	Cell stuck-at, stuck-open, coupling, transition, address decoder, transient R/W, data retention, and port fault for multiport memory	Mats = algorithm for all port widths: 13n moving inversion algorithm; two-port memory tests; at-speed tests	100% industry-standard testing
I/O boundary scan		Open, short, stuck at	Boundary scan IEEE 1149.1 for all I/Os and IEEE 1149.6 for high-speed I/Os	100% functional test
Misc. / Other	Temp sensor	Measure on-die temperature	JTAG accessible	100% functional test
	Voltage sensor	Measure on-die voltage	JTAG accessible	100% functional test
	Electronic chip ID	Device ID including wafer lot, wafer number, X/Y coordinates	JTAG accessible	100% functional test

Table 1. Key Manufacturing Tests: *These test examples illustrate the test methodology innovation and continuous improvements that are intrinsic parts of the Xilinx engineering culture. Learnings from previous generations and excellent coverage are leveraged to overcome the challenges with newer technology and ultimately enable the release of high-quality All Programmable solutions.*

Conclusion

With the challenges related to shrinking process nodes, DFT expectations keep increasing to sustain the excellent results, demonstrated by 2012 customer-experienced PPM results *(see Table 2)*.

Spartan FPGA		
Product	Technology Node	PPM
Spartan-II/IIE	.22µm/.18µm/.15µm	0.0
Spartan-3	90nm	0.3
Spartan-3E	90nm	0.0
Spartan-3A/3AN	90nm	0.4
Spartan-6	45nm	0.7

Virtex FPGA		
Product	Technology Node	PPM
Virtex/-E	.25µm/.18µm	0.0
Virtex-II/IIP	.15µm/.13µm	0.6
Virtex-4	90nm	1.8
Virtex-5	65nm	4.6
Virtex-6	40nm	4.9
7 series	28nm	0.0

Table 2. Customer Overall PPM: *Based on customer return data, Xilinx FPGAs deliver world-class quality.*

Note: This year, Xilinx has expanded its approach, and customers can see the results of these efforts through special characterization and testing reports published by Xilinx (Ref: RPT125, RPT126, RPT127). For more information, please contact your local customer quality engineering team or sales representative.