



Xilinx XtremeDSP Newsletter - November 2006

Top XtremeDSP News

[Change Your DSP WorldView – New BDTI DSP Benchmark Data](#)

Download visionary article titled “[Challenging Your DSP WorldView](#)” by Omid Tahernia, VP and GM of Xilinx Processing Solutions Group
See how Xilinx outperformed Altera by a factor of 2X in BDTI’s latest independent technical DSP benchmark study called “[FPGAs for DSP](#)”

[New Virtex™-5 LX/LXT FPGAs Help Reduce DSP Power Consumption by 40%](#)

[Get On The XtremeDSP Fast Track with Low Cost Productivity Packages](#)

In This Issue

- [XtremeDSP Collateral](#)
- [XtremeDSP Solutions for Multimedia, Video & Imaging](#)
- [XtremeDSP Solutions for Digital Communications](#)
- [XtremeDSP Solutions for Defense Systems](#)
- [General Purpose XtremeDSP Solutions](#)
- [XtremeDSP Support & Services](#)
- [DSP Tradeshows, Events & Seminars](#)

XtremeDSP Collateral

Latest Xilinx XtremeDSP Selection Guide

Make sure you have the most up to date XtremeDSP product and solution information by downloading the latest XtremeDSP Selection Guide.

[Download here](#)

New Texas Instruments DSP Resource Guide

Get information on Xilinx XtremeDSP co-processors and development solutions for Texas Instruments DSPs.

[Get the latest TI DSP Resource Guide here](#)

XtremeDSP Solutions for Multimedia, Video & Imaging

Sundance’s new [SMT339 image processing module](#) is based on the Xilinx Virtex-4 FX-60 FPGA and a TI TMS320DM642 DSP. This hardware is supported by Parallel Application Rapid Simulation (PARS) software which enables an entire application development environment for FPGA and DSP development from within The MathWorks Simulink tool.

XtremeDSP Solutions for Digital Communications

New WCDMA/WiMAX Development Platform with Reference Designs

This new development platform integrates many radio card functions (e.g. DUC, DDC, CFR, CPRI/OBSAI) and significantly helps to increase power amplifier (PA) efficiency while reducing development time and risk. The development platform includes [hardware](#) developed by AXIS Network Technologies and [WiMAX and WCDMA reference designs](#) from Xilinx.

[Enhanced FEC Algorithms \(IP cores\) – Update #2 for ISE 8.2](#)

There are a number of enhancements to Forward Error Correction (FEC) cores in the latest release.

Reed-Solomon Decoder v6.0

Now with Virtex-5 LX/LXT support and increased functionality

Viterbi Decoder v6.0

Now with Virtex-5 LX/LXT Support (DSP48E optimized), 313MHz performance (-3 speed grade), half the BRAM needed, increased flexibility and functionality

802.16 TCC (CTC) Encoder v2.0

Now with Virtex-5 LX/LXT support and IEEE802.16e-2004/Cor1/D5 compliance

3GPP TCC Encoder v3.0, 3GPP TCC Decoder v3.0, Interleaver v5.0 Improvements over previous versions

Now with Virtex-5 LX/LXT support

XtremeDSP Solutions for Defense Systems

[Software Defined Radio \(SDR\) Development Platforms at the SDR Forum 2006](#)

Come and see the latest SDR development kits for reducing system size, power and cost at the SDR Forum Conference (see Tradeshow and events below). We invite you to the following sessions with Xilinx presenters:

- Tutorials
 - Reconfigurable Technology for MIMO-OFDM Systems with a Focus on 802.16/802.16e - R. M. Rao, C. Dick (9.00-12.30pm, November 13)
- Other Technical Papers
 - Architecture and Simulation of Timing Synchronization Circuits for the FPGA Implementation of Narrowband Waveforms (C. Dick, Fred Harris)
 - Dynamic Radio Location Under Extreme Multipath Conditions (B. Egg, C. Dick, Fred Harris)
 - Moore or Less? A Critical Comparison of Bandwidth vs. Resolution (B. Egg, C. Dick, Fred Harris)
 - Ultra Low Phase Noise DDS (Chris Dick, Fred Harris, R Jakel)
 - FPGA-Based Single Chip Cryptographic Solution (J. Moore, M. McLean)
 - New Architecture Development Platform Targeted for Portable Applications (M.Uhm, R Saththappan, M. Dumas)

Also register for the Xilinx Customer Hospitality suite to discuss your design needs and find out about our forthcoming products. Contact cindy.spina@xilinx.com to register a time slot.

General Purpose XtremeDSP Solutions

Reduce DSP Power Consumption by up to 40% with Virtex-5 LXT & LXT FPGAs

Gain a competitive advantage and reduce DSP power consumption by up to 40% by designing using the world's only 65nm FPGAs. Virtex-5 LX and LXT FPGAs. These new FPGAs give you access to new DSP48E slices, memory, logic and serial interfaces. DSP48E slices feature high precision 18x25 multipliers/48-bit adders for extra dynamic range and new features such as support for SIMD, pattern detection and dedicated C-inputs.

[Learn more here](#)

Evaluate The Latest Xilinx XtremeDSP Software Tools

Make sure you have the latest DSP software to build optimal designs whether you are an Algorithm Developer, System Engineer or Hardware Engineer.

[Evaluate System Generator for DSP 8.2 Tool](#)

The new System Generator for DSP tool now supports Xilinx 65nm Virtex-5 LX/LXT and Spartan™-3E FPGA families. Designers, like you, are reducing development time using System Generator for DSP.

[View this customer's story](#)

[Evaluate AccelDSP™ 8.2 MATLAB-to-RTL-Synthesis Tool](#)

The new AccelDSP tool now supports Xilinx 65nm Virtex-5 LX /LXT and Spartan-3E families.

New Xilinx Productivity Advantage (XPA) Packages

Two new Xilinx Productivity Advantage packages are available to help you gain easier access to our state of the art DSP design tools and make significant package cost savings:

- XtremeDSP XPA for Model-Based Design (Part # DS-XPA-10K)

- This contains the System Generator for DSP 8.2 Tool, AccelDSP 8.2 Tool, ISE Foundation (including ISIM) Tool and 4 days of training

- XtremeDSP XPA for MATLAB (Part # DS-XPA-25K)

- This contains the AccelDSP 8.2 Tool, AccelDSP Communications Toolkit, AccelDSP Advanced Math Toolkit, ISE Foundation (including ISIM) and 2 days of training

[Ask your local Xilinx Sales representative about these new packages](#)

Enhanced General Purpose DSP Algorithms (IP cores) – Update #2 for ISE 8.2

ISE 8.2 IP Update #2 is now available. It includes enhancements to three important DSP IP cores:

- **FIR Compiler v2.0**

- Now with support for Virtex-5 LX/LXT FPGAs (including DSP48E & 6LUT), fixed fractional interpolation/decimation, zero packed interpolated filters, Hilbert Transforms, coefficient symmetry support for multi-rate filters, floating Point coefficient entry.

- **DDS Compiler v1.0**

- Now with support for Virtex-5 LX/LXT FPGAs (including DSP48E & 6LUT), improved clock performance (429 MHz average clock frequency) and improved design exploration capabilities.

- **Floating Point Operators v3.0**

- Now with support for Virtex-5 LX/LXT FPGAs (including DSP48E & 6LUT), improved clock performance, increased floating point operator coverage, and improved design exploration capabilities and instantaneous resource estimation of DSP48/DSP48E and BRAM

XtremeDSP Support & Services

XtremeDSP Classes for Customers

Take a Xilinx DSP Class near you. We offer two comprehensive classes that will help you to design optimal designs

- DSP Design Flow Class
- DSP Implementation Techniques Class

[View the agendas & register here](#)

DSP Tradeshows, Events & Seminars

Discuss your DSP design needs with Xilinx XtremeDSP engineers at these upcoming events:

Software Radio Forum

- Orlando, USA; November 13-17
- Come and see the latest SDR development solutions for reducing cost and power
- Discuss your design needs by registering for the Xilinx customer hospitality suite by emailing: cindy.spina@xilinx.com

Electronica 2006 (Hall A4, Booth 576)

- Munich, Germany; November 14-17
- See XtremeDSP solutions are being used for medical image processing and video over Ethernet. Also ask about new pricing discount bundles for XtremeDSP software.
- Schedule a meeting with the Xilinx team at Electronica 2006, by contacting your Xilinx sales representative or Mrs.Ute Brandhorst in our Munich office, tel. +49 89 93088 2110 or email: ute.brandhorst@xilinx.com

Tackling FPGA Design Challenges for Embedded Systems Seminar (Pentek)

- This short seminar will cover FPGA system design guidelines, pitfalls to avoid and tips for choosing the best FPGA strategy. FPGA chip design philosophies, new product announcements and specifications will also be discussed.
- [Learn more & register here](#)

© Copyright 1994-2006 Xilinx, Inc. All Rights Reserved

This email was sent to: %%emailaddr%%

This email was sent by: %%Member_Busname%%
%%Member_Addr%%
%%Member_City%%, %%Member_State%%, %%Member_PostalCode%%
%%Member_Country%%

Xilinx does not rent, sell or lease customer information. We respect your right to privacy - [view](#) our policy.

You are currently subscribed to receive Xilinx email communications.
Go [here](#) to view/modify your preferences.

Go [here](#) if you no longer wish to receive Xilinx email.

If you have difficulties or questions about this process, please contact: xilinxmail@xilinx.com