



Tips and Tricks for IP Integrator

Presented By

Daniel E. Michek
Interaction Design
2 October, 2018



The Evolution of IP Integrator

2013 - IPI
IP Integrator debut – replaces XPS

2015 - HLx
Vivado HLx Methodology – IP Integrator for shell
SDx / HLS for differentiation

Next – ACAP
Versal ACAP debut – IP Integrator enables H/W shell with Versal heterogeneous features
IP Integrator improves WYSIWYG RTL

What You'll See in this Presentation



> Technical, demo centric, methodology tips presentation

- >> Helpful today
- >> Needed for tomorrow

> We'll see, using a real-world design

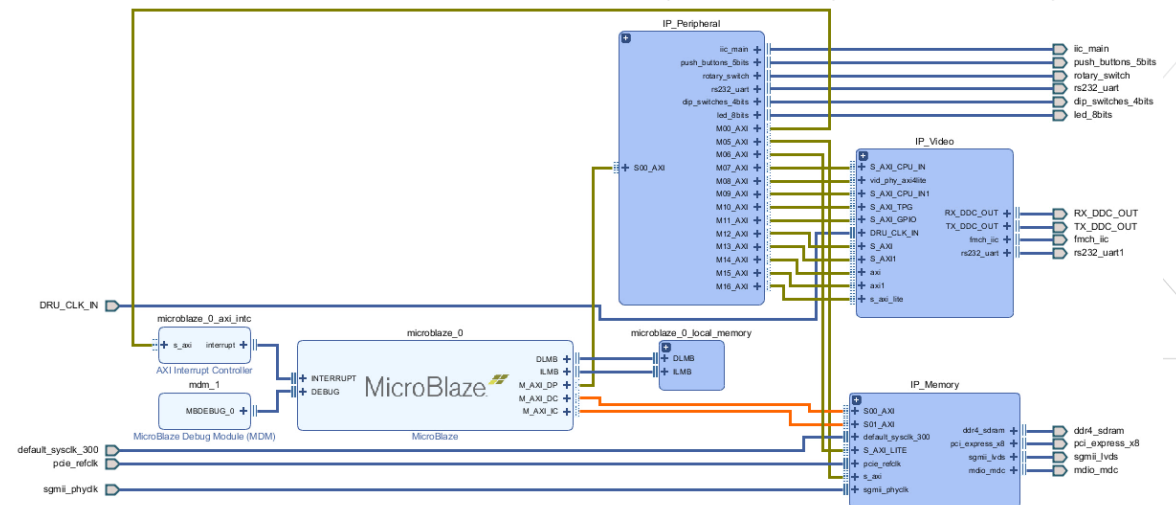
- >> Features of IP Integrator to rapidly build designs with complex IP
- >> New Ease-of-Use features (Find, Pinning)
- >> New Design Migration capabilities
- >> New Design Differencing

Most Common Requests for IP Integrator

> Ease-of-Use

> Migration Hurdles

> Team Based Design



Most Common Requests for IP Integrator

> Ease-of-Use

- >> Finding IP, Freezing IP
- >> Example Designs in IP Integrator

> Migration Hurdles

- >> Selectively updating IP
- >> Migrating to next generation devices

> Team Based Design


- >> Enable teams to work in tandem (Spring 2019)
- >> Visualize differences between Block Diagrams



Visual Walkthrough

> Start to End

1. Creating a new design for the KCU105
2. Creating an example design for HDMI
3. Using Find and hierarchical partitioning
4. Migrating from ProjectA.bd to ProjectB.bd
5. Cross Probing with timing closure
6. The toolbar review
- 2018.3 Preview ---
7. Selective migration from Vivado 2018.1 to 2018.3
8. What changed during upgrade in the block diagram
9. Migrating to the Versal NoC

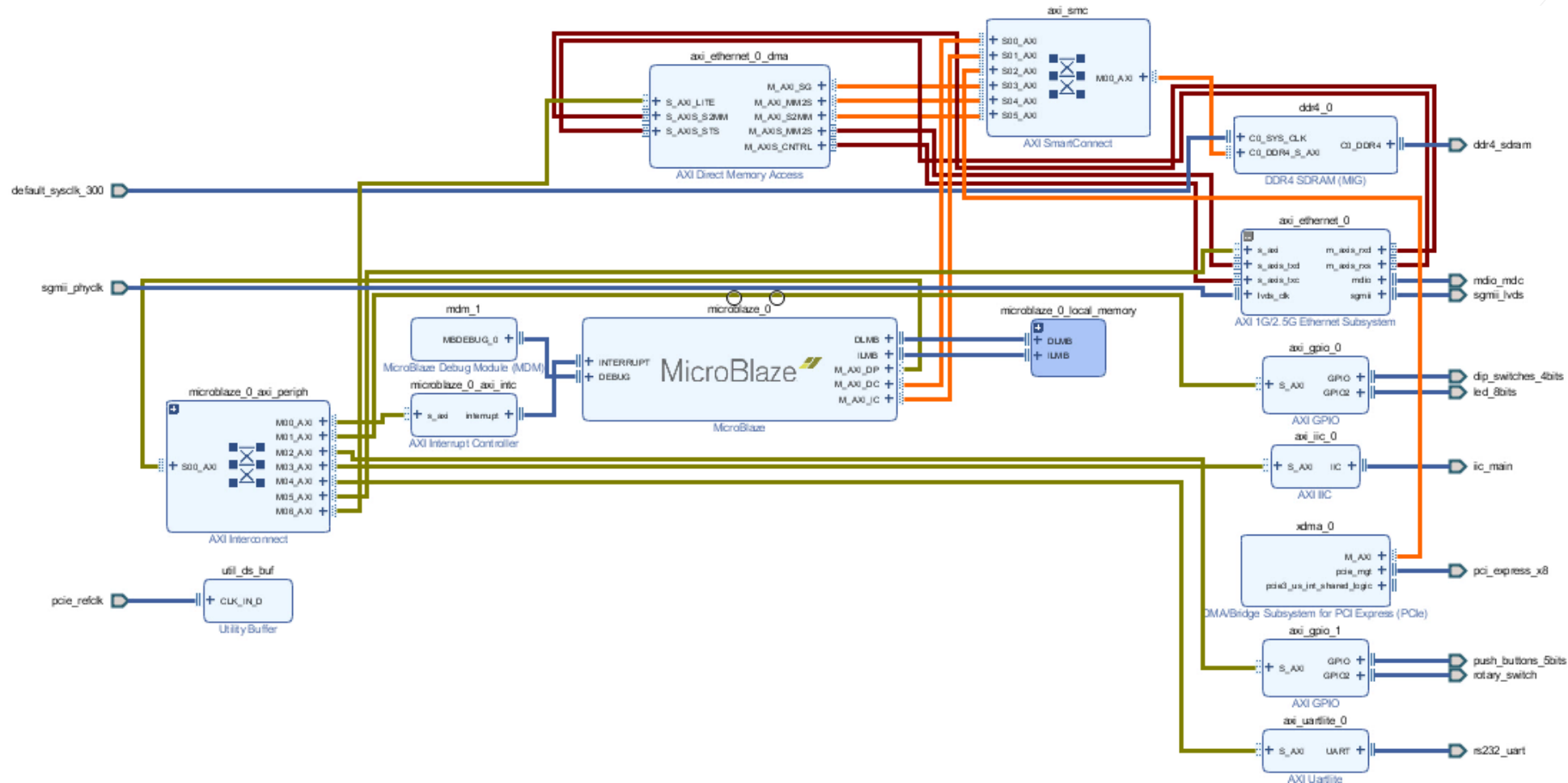


Working with complex IP
Ease of Use

Team Based Design
Migration
Next generation devices

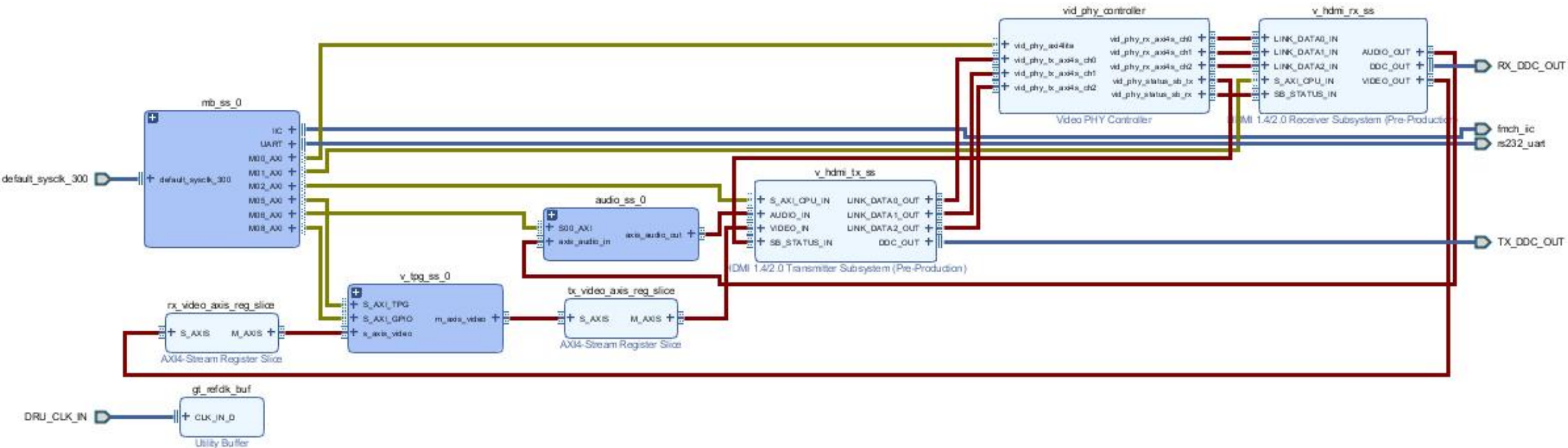
1. Ease of Use – Designer Assistance

> Board, Block, and Connectivity Automation helps to put together systems



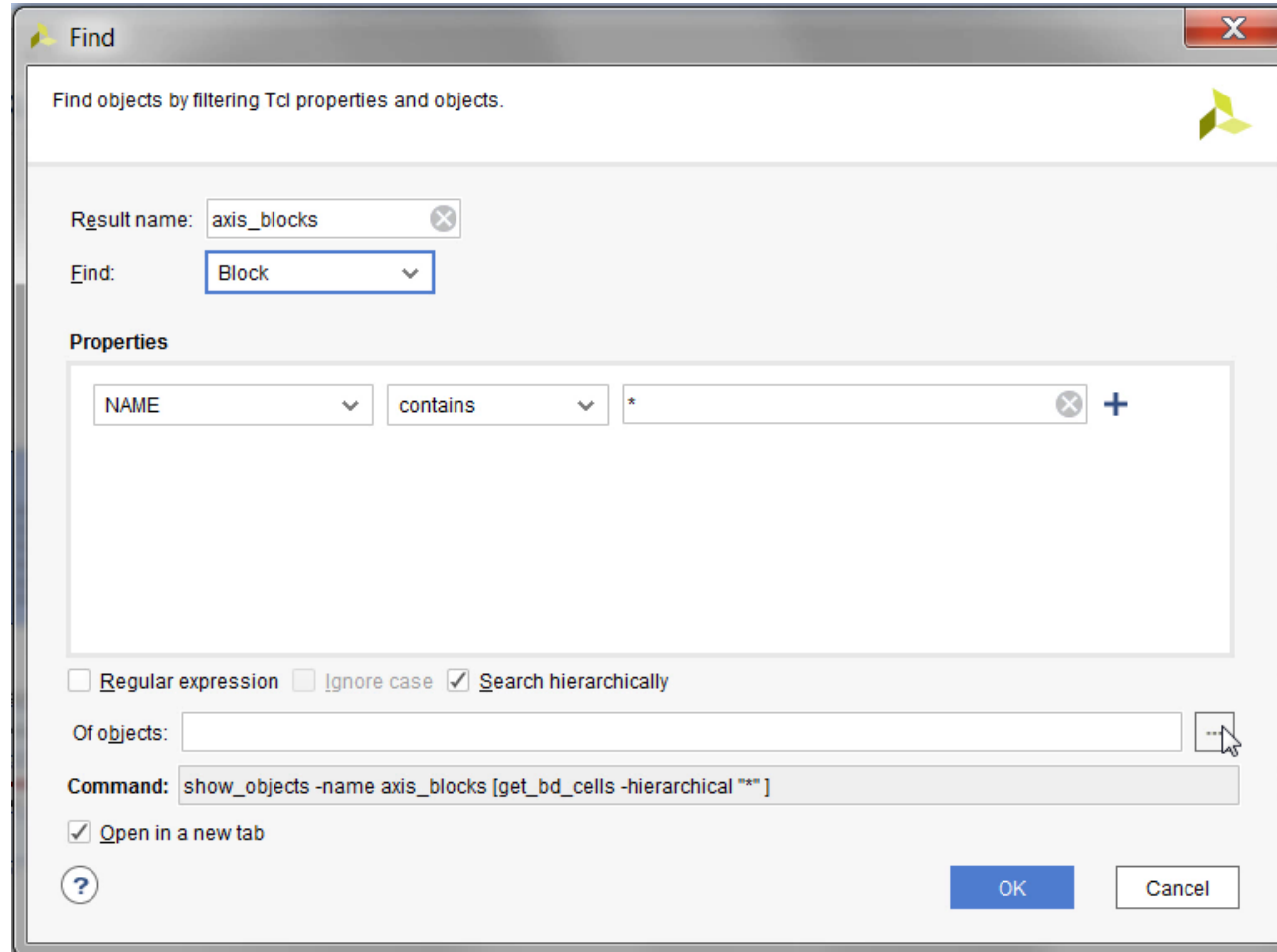
2. Example – Example Designs

> Example Designs can be launched from IP Integrator or IP Catalog



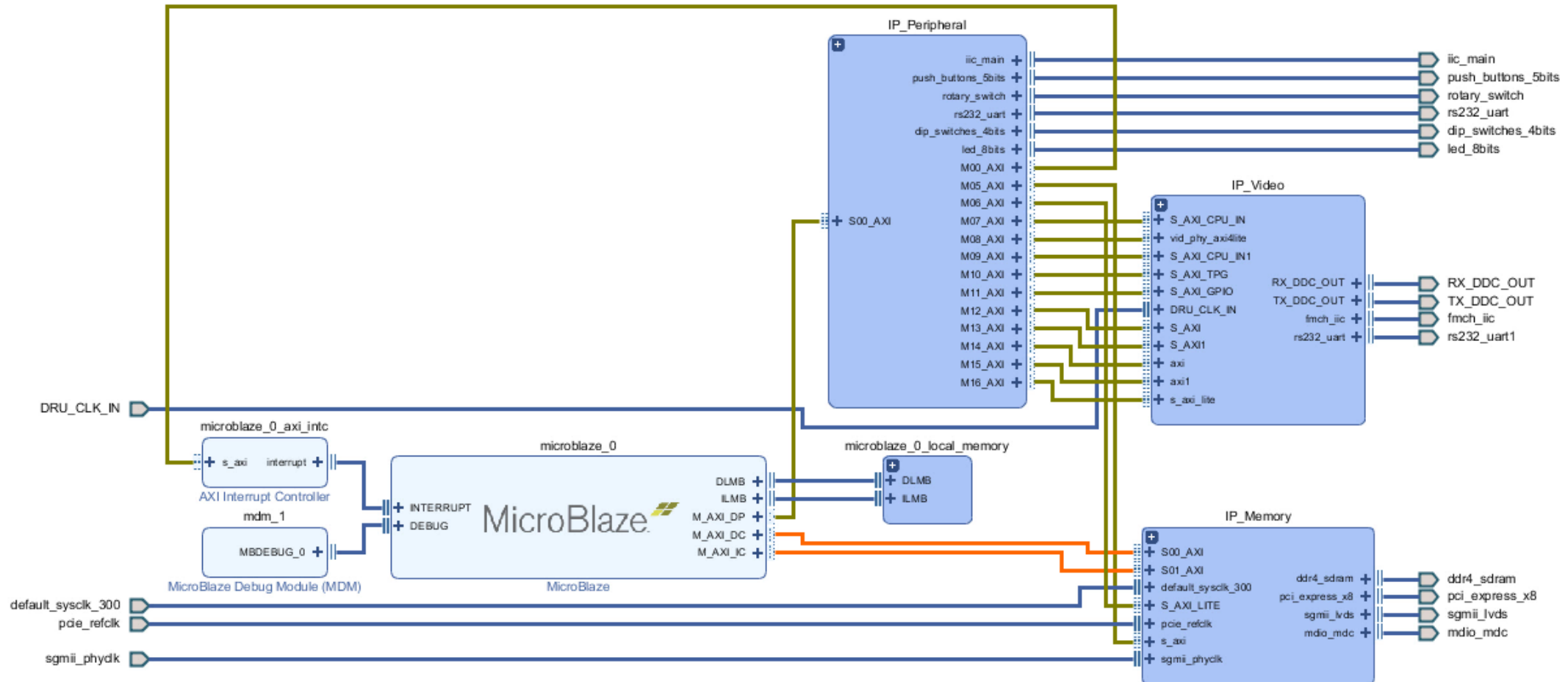
3. Ease of Use – “Super Find” in IP Integrator

- > Find items on the canvas based on connectivity, naming, or properties



4. Migration – From One Block Diagram to Another

> Block diagrams should be in the same project



5. Ease of Use – Cross Probe from Timing Analysis

- > Quickly find areas that need improvement

The image displays two side-by-side screenshots of the Xilinx Vivado IDE. The left window, titled 'IMPLEMENTED DESIGN - xcku040-ftva1156-2-e (active)', shows a Netlist with a list of components and a Timing Summary table. The right window, titled 'BLOCK DESIGN - video_400', shows a block diagram with a path highlighted in yellow.

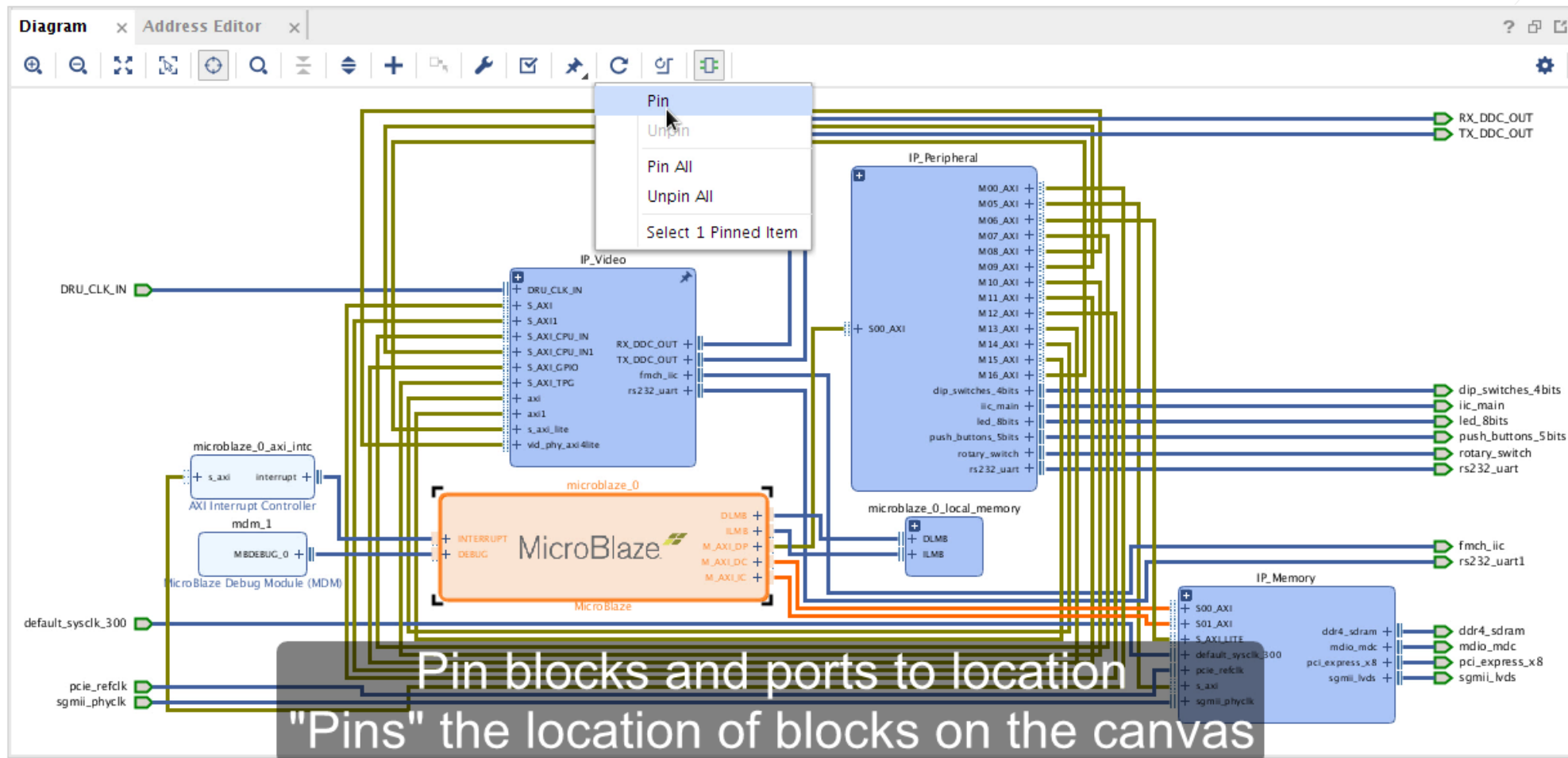
Timing Summary - impl_1 (saved)

Slack	Levels	High Fanout	From
Setup -0.022 ns (10)	-0.022	2	37 video_400_i/MicroBlaze_subsystem/microblaze_0_axi_periph/m01_couplers/auto_cc/inst/gen_clock_conv/gen_sync_conv/gen_conv_read_ch_ar_...
Hold -0.038 ns (10)	-0.022	2	37 video_400_i/Mic...oab_r_reg[8]/C
m01_couplers to m01_couplers	-0.016	2	
m01_couplers to m01_couplers	-0.016	2	
Other Path Groups	-0.016	2	
User Ignored Paths			

Select Failing Timing Paths

6. Ease of Use – Stop Squirming - Pin IP on Canvas

> A review of the toolbar actions



Preview: Get the Latest Boards Right From Vivado

The image shows two overlapping windows from the Vivado IDE. The top window is the 'New Project' dialog, which has a 'Default Part' section and a 'Boards' tab. A green box highlights the 'Manage Board Repositories' button in the 'Boards' section. The bottom window is the 'Settings' dialog, with the 'Board Repository Defaults' section selected in the left sidebar. This section contains a 'Download location' field, a 'Refresh Catalog' button, an 'Install Latest Version' button, and a 'Board Repository Search Paths' list. A green box highlights the 'Board Repository Defaults' section in the sidebar.

The image shows a GitHub repository page for 'Xilinx / XilinxBoardStore'. The repository is on the '2018.1-dev' branch. The page shows a commit by 'rkunwar-xilinx' titled 'Revised avnet board files' from 5 days ago. Below the commit, there is a list of files:

File Name	Description	Last Commit
minized	Revised avnet board files	5 days ago
ultrazed_3eg_iocc	Revised avnet board files	5 days ago
ultrazed_3eg_pciecc	Revised avnet board files	5 days ago
ultrazed_3eg_som	Revised avnet board files	5 days ago

<https://github.com/Xilinx/XilinxBoardStore/tree/2018.1-dev>

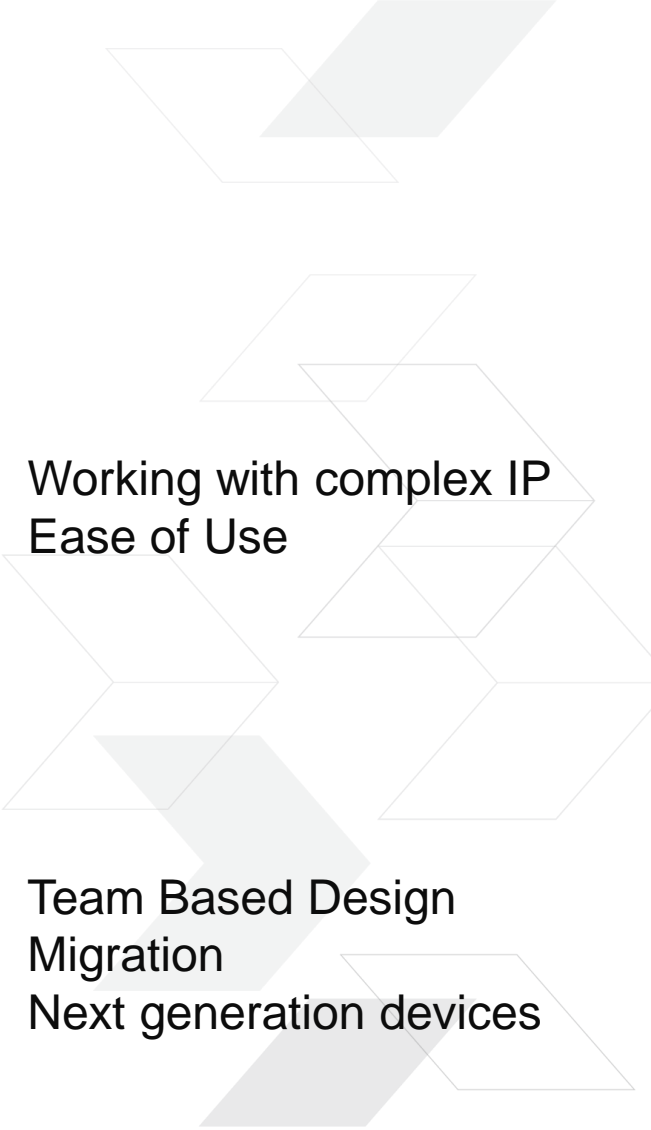
A Preview of IP Integrator's Migration Assistance in 2018.3



Visual Walkthroughs

> Start to End

1. Creating a new design for the KCU105
2. Creating an example design for HDMI
3. Using Find and hierarchical partitioning
4. Migrating from ProjectA.bd to ProjectB.bd
5. Cross Probing with timing closure
6. The toolbar review
- 2018.3 Preview ---
7. Selective migration from Vivado 2018.1 to 2018.3
8. What changed during upgrade in the block diagram
9. Migrating to the Versal NoC

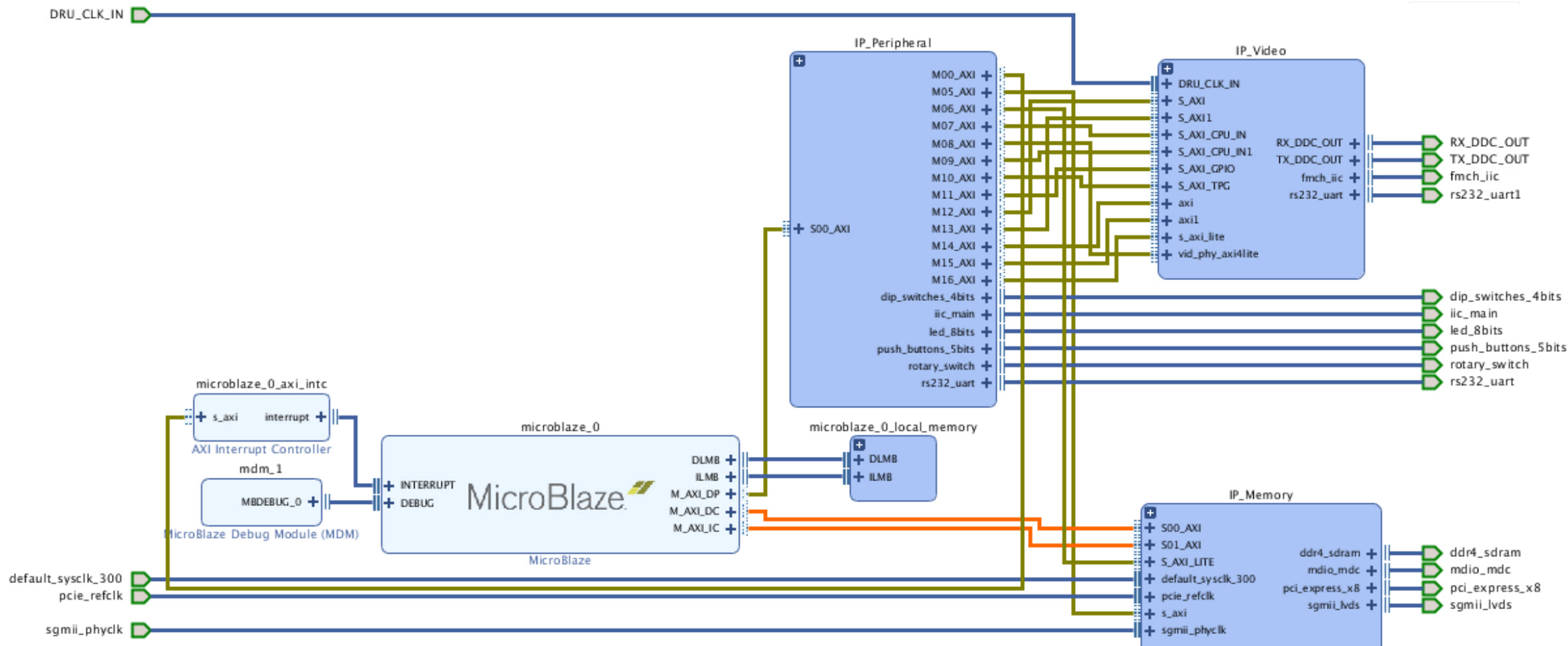


Working with complex IP
Ease of Use

Team Based Design
Migration
Next generation devices

7. Migration – Vivado Versions via Partial Update

> Keep the blocks which have been previously validated in-system



8. What Changed In the Upgrade?

> New interactive report shows differences between block diagrams

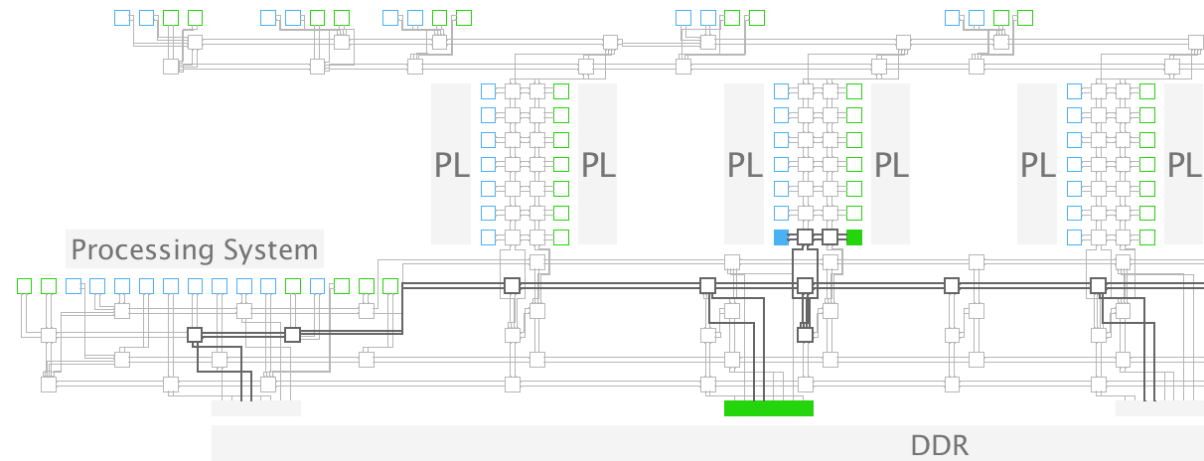
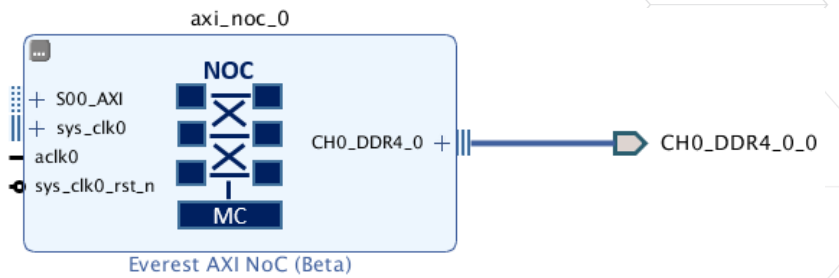
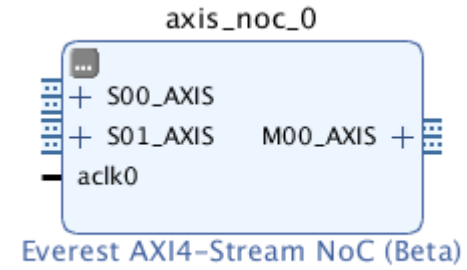
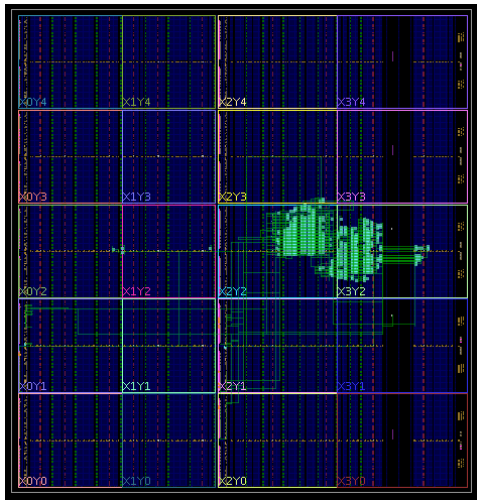
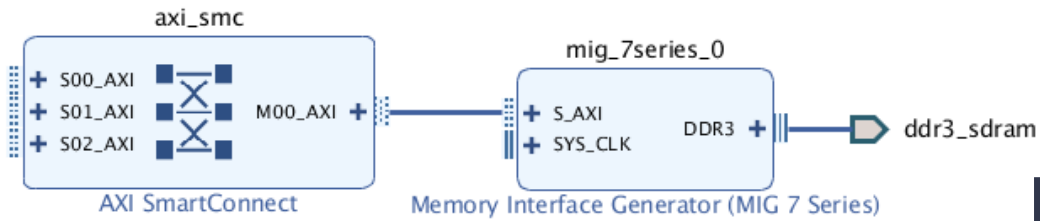
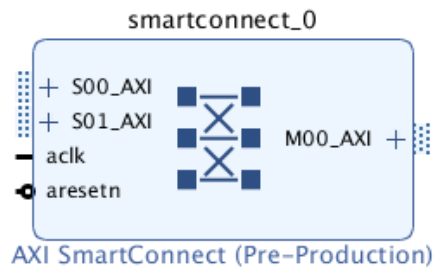
Block Diagram Differences

Previous Next Show Filter Expand All Expand Diffs Collapse All

Copyright © 2018 Xilinx Inc.

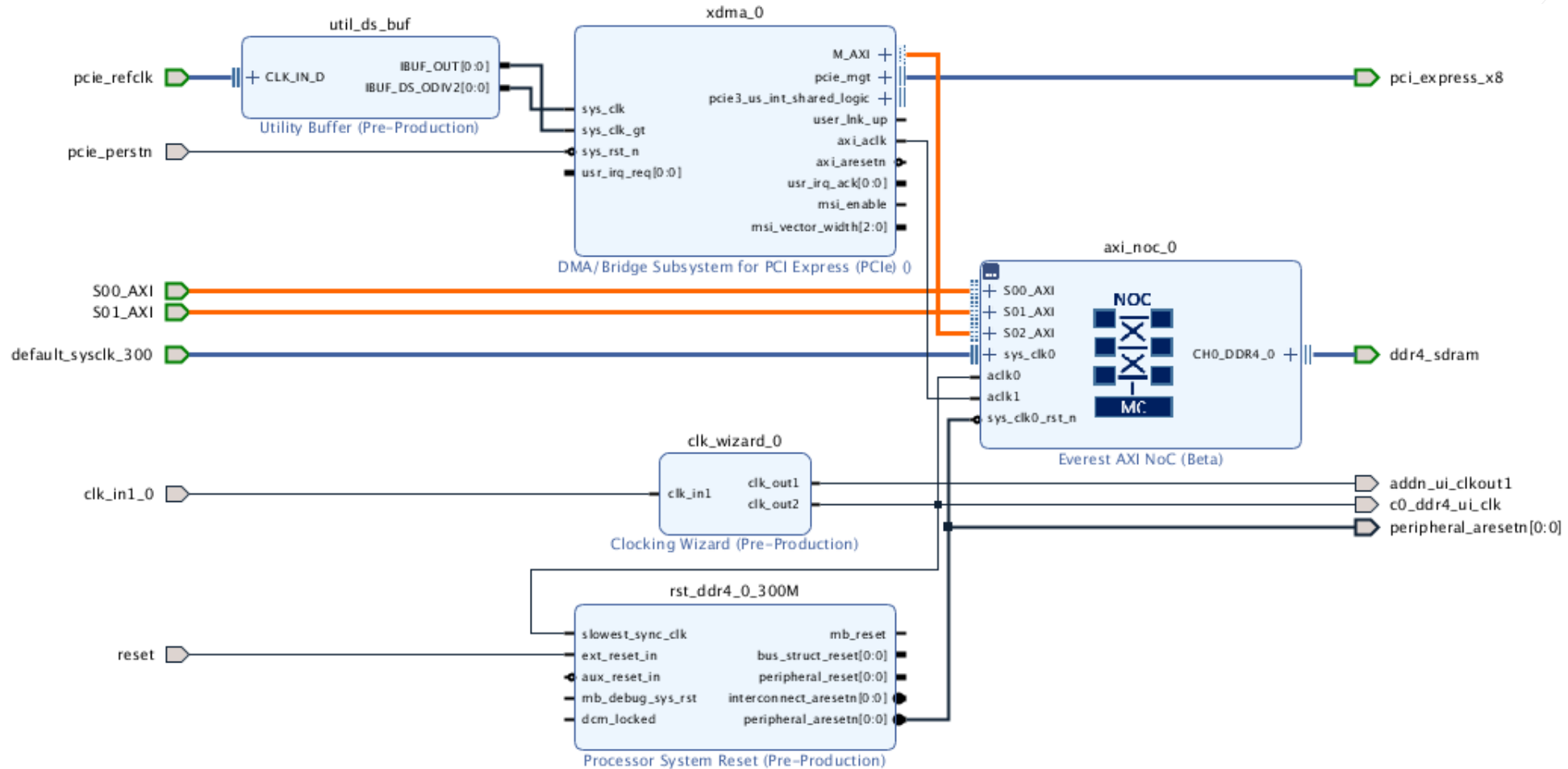
design_1.bd	/home/danielm/Desktop/vivLogs/XDF18/combined/combined/srcs/sources_1/bd/design_1/design_1.bd
<ul style="list-style-type: none">Design<ul style="list-style-type: none">Components (9)<ul style="list-style-type: none">IP_Memory<ul style="list-style-type: none">Components (3)<ul style="list-style-type: none">IP_DDR_MPMC<ul style="list-style-type: none">Components (3)<ul style="list-style-type: none">axi_smc<ul style="list-style-type: none">Interface Ports (7)<ul style="list-style-type: none">S00_AXI	<ul style="list-style-type: none">Design<ul style="list-style-type: none">Components (9)<ul style="list-style-type: none">IP_Memory<ul style="list-style-type: none">Components (3)<ul style="list-style-type: none">IP_DDR_MPMC<ul style="list-style-type: none">Components (3)<ul style="list-style-type: none">axi_smc<ul style="list-style-type: none">Interface Ports (7)<ul style="list-style-type: none">S00_AXI
	memory_map_ref=S00_AXI

Preview: Versal NoC!



9. Migrating to Versal ACAP

> Upgrading our current project to reduce programmable logic resources (area)



Changes to Our Release Schedule

- > **Vivado previously had four full releases per year**
 - >> 2017.1 & 2017.3 introduced new features
 - >> 2017.2 & 2017.4 improved quality – Many users installed only the even releases
- > **In 2018, we will have three full releases**
 - >> 2018.3 is coming soon
- > **And two in 2019**
 - >> Spring and Fall – No more wait states for new features or quality
 - >> Quality is our top priority



Most Common Requests for IP Integrator

> Ease-of-Use

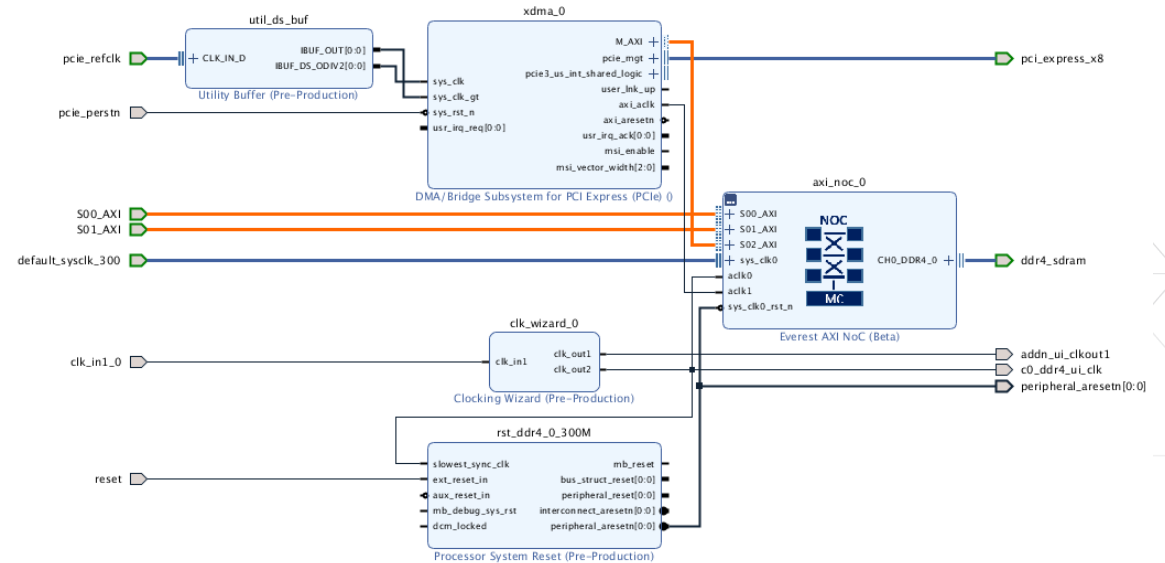
- >> Finding IP, Freezing IP
- >> Example Designs in IP Integrator

> Migration Hurdles

- >> Selectively updating IP
- >> Migrating to next generation devices

> Team Based Design

- >> Enable teams to work in tandem (Spring 2019)
- >> Visualize differences between Block Diagrams



Key Concepts: Vivado IP Integrator 2018.3

Board, Block, Connectivity, and Migration Assistance

- > Take advantage of IP Integrator's built in assistance to create your ideal processing system -- including adding customized interfaces for networking, video, and DSP

Getting ready to migrate to Versal ACAP

- > The migration to Versal ACAP will continue to add new assistance features and increase the traceability of IP Integrator



XILINX
DEVELOPER
FORUM

