



## 2017 Xilinx Security Working Group (XSWG) Munich, Germany Agenda

HILTON MUNICH AIRPORT, Terminal Strasse Mitte 20, 85356 Munich Airport, Germany

### Thursday December 7, 2017

Topic	Presenter	Time
Check In and Pre-Conference Luncheon		7:30am - 8:00
Welcome and Introductions	Xilinx	8:00 - 8:15
Next Generation Security Architecture	Xilinx	8:15 - 9:30
Using Security in Zynq UltraScale+ MPSoC Devices	Xilinx	9:30 - 11:00
Break		11:00 - 11:15
Isolation for Security in Zynq UltraScale+ MPSoC Devices	Xilinx	11:15 - 12:30
Lunch		12:30 - 1:30
Designing a Secure System with UltraScale/UltraScale+ MPSoC Devices	Xilinx	1:30 - 2:45
SecMon Update	Xilinx	2:45 - 4:00
Break		4:00 - 4:15
Security Lifecycle Manager	Xilinx	4:15 - 5:15
Day 1 Wrap Up	Xilinx	5:15 - 5:25
Evening Social and Partner Demonstrations		5:30 - 7:00



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### Friday December 8, 2017

<b>Continental Breakfast</b>		7:30 - 8:00	
<b>Day 2 Re-Greet</b>	<b>Xilinx</b>	8:00 - 8:15	
<p><b>Note on day 2 that attendees may choose from an alternate track for demo / walkthrough sessions. Contents of demo session I and demo session II are identical.</b></p>			
<b>Lecture Track : Main Assembly Room</b>		<b>Demo Track : Breakout Room</b>	
Accelerated TLS for Xilinx	wolfSSL	<b>Building a Zynq UltraScale+ MPSoC Devices, Secure Boot Design Cradle to Grave Session I Xilinx</b>	8:15 - 9:00
Trust in Xilinx Products: Assurance in Your Supply Chain	Xilinx		9:00 - 9:30
Cybersecurity Concept Design	Mocana		9:30 - 10:15
<b>Break</b>			10:15 - 10:30
Secure Device Provisioning	Xilinx	<b>Building a Zynq UltraScale+ MPSoC Devices, Secure Boot Design Cradle to Grave Session II Xilinx</b>	10:30 - 11:30
Design Guidance From an Expert: How To Be Successful with Your Next Xilinx Design	Xilinx		11:30 - 12:15
<b>XSWG2017 General Session Adjournment (Main Assembly Room)</b>			<b>12:15 - 12:30</b>
<b>Post Conference Luncheon</b>			12:30 - 1:30