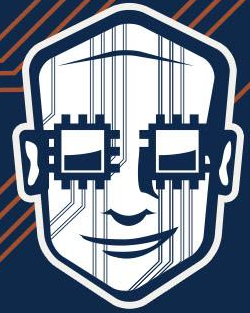


DESIGNCON[®] 2015



IBIS-AMI Model Simulations Over Six EDA Platforms



Romi Mayder, romi.mayder@xilinx.com

Ivan Madrigal, ivan.madrigal@xilinx.com

Brandon Jiao, brandon.jiao@xilinx.com

Hongtao Zhang, hongtao.zhang@xilinx.com

Geoff Zhang, geoff.zhang@xilinx.com

Disclaimer

This presentation is not intended to be a benchmark. We have done our best to ensure the information presented is accurate. However, the presentation might be subject to technical inaccuracies. As a consequence, we cannot guarantee the accuracy or completeness of the information presented.

Outline

- Motivation of this comparative study project
- IBIS-AMI high speed link system modeling highlight
- Description of three simulation cases over six EDA tools
 - Case 1: 25Gbps link, with no jitter or noise impairments added
 - Case 2: 25Gbps link, with added jitter and noise impairments
 - Case 3: 25Gbps link, with jitter, noise, and crosstalk impairments added
- Simulation results
 - Eye diagrams and eye metrics (EH and EW at BER=1e-12)
 - AGC, CTLE, DFE, CDR adaptations and convergences
 - Timing bathtub curves and BER contours
- Observations and discussions of simulation results
- Summaries

Motivation of the Work

- Throughout the years, Xilinx has been questioned by many its customers with regards to their IBIS-AMI simulation accuracy, speed, reliability, etc.
 - Xilinx completely renewed its IBIS-AMI model development process to address simulation speed in 2013.
 - Xilinx delivered its IBIS-AMI model correlation reports with both design and hardware.
- However, we also noticed that sometimes our simulation results did not correlate well with customers', depending on the EDA tool used.
 - It turned out that different EDA tools generated different simulation results, particularly as simulation conditions change.
- This prompted us to start the work, which resulted in this tutorial. The work is not intended to be a benchmark.
 - The six EDAs are named EDA-1, EDA-2, EDA-3, EDA-4, EDA-5, and EDA-6.

IBIS-AMI Modeling Highlights

IBIS-AMI Background

- IBIS-AMI model development goals are:
 - Interoperability: Models from different EDAs operate together.
 - Transportability: Models run across multiple EDA Tool platforms.
 - Performance: One million bits can be simulated in <10 minutes.
 - Usability: Models expose control parameters are configurable by user.
 - IP Protection: Models are proprietary and cannot be reverse-engineered.
- Specific requirements for IBIS-AMI were ratified in IBIS v5.0 in Aug 2008.
- Important improvements regarding modeling accuracy and capability were ratified in v5.1 in Aug. 2012 and v6.0 in Sept. 2013 subsequently.

Xilinx Commitment to IBIS-AMI

- Xilinx has developed IBIS-AMI compliant models since 2008, starting with Virtex-6 and continuing today in UltraScale family products.
- Xilinx has multiple means of generating transceiver IBIS-AMI models.
- Xilinx has a dedicated team responsible for IBIS-AMI model development.
- Xilinx has a good working relationship with multiple EDA companies. Together we serve our end users.
- Xilinx is a member of the IBIS committee and participates in all related working groups.

Xilinx IBIS-AMI Model Feature

- Xilinx newly developed IBIS-AMI models are all IBIS-AMI 5.0 compliant.
- Linear Time Invariant (LTI) modeling in the IBIS portion is assumed.
- The released model supports time-domain simulation mode.
- The released model supports clock tick output.
- The model supports Clock Data Recovery (CDR), Continuous-Time Linear Equalization (CTLE), and Decision Feedback Equalization (DFE) in the model, both manual and auto adaptation
 - All the adaptation convergences are transparent to the end user to facilitate system level simulation and parameter optimization
- The model contains most impairments and non-idealities in the silicon.
- The model contains multiple PVT corners (both TX and RX) for the customer to explore system margins.

Xilinx IBIS-AMI Model Availability

- To download the UltraScale GTY IBIS-AMI model, visit this link:
 - http://www.xilinx.com/member/ultrascale_ibis_ami/

UltraScale IBIS-AMI Models

Below is the latest version of the UltraScale™ IBIS-AMI Models

File Name	Size	Date
Xilinx_UltraScale_GTY_AMI_Kit_Ver2p1	25.00 MB	Aug. 28, 2014
Xilinx_UltraScale_GTH_AMI_Kit_Ver2p1.zip	56.00 MB	Aug. 7, 2014

- Revision Control with Xilinx
 - V1.x Architectural Model
 - V2.x Design Correlated Model
 - V3.x Hardware Correlated Model

Xilinx IBIS-AMI Transceiver Model

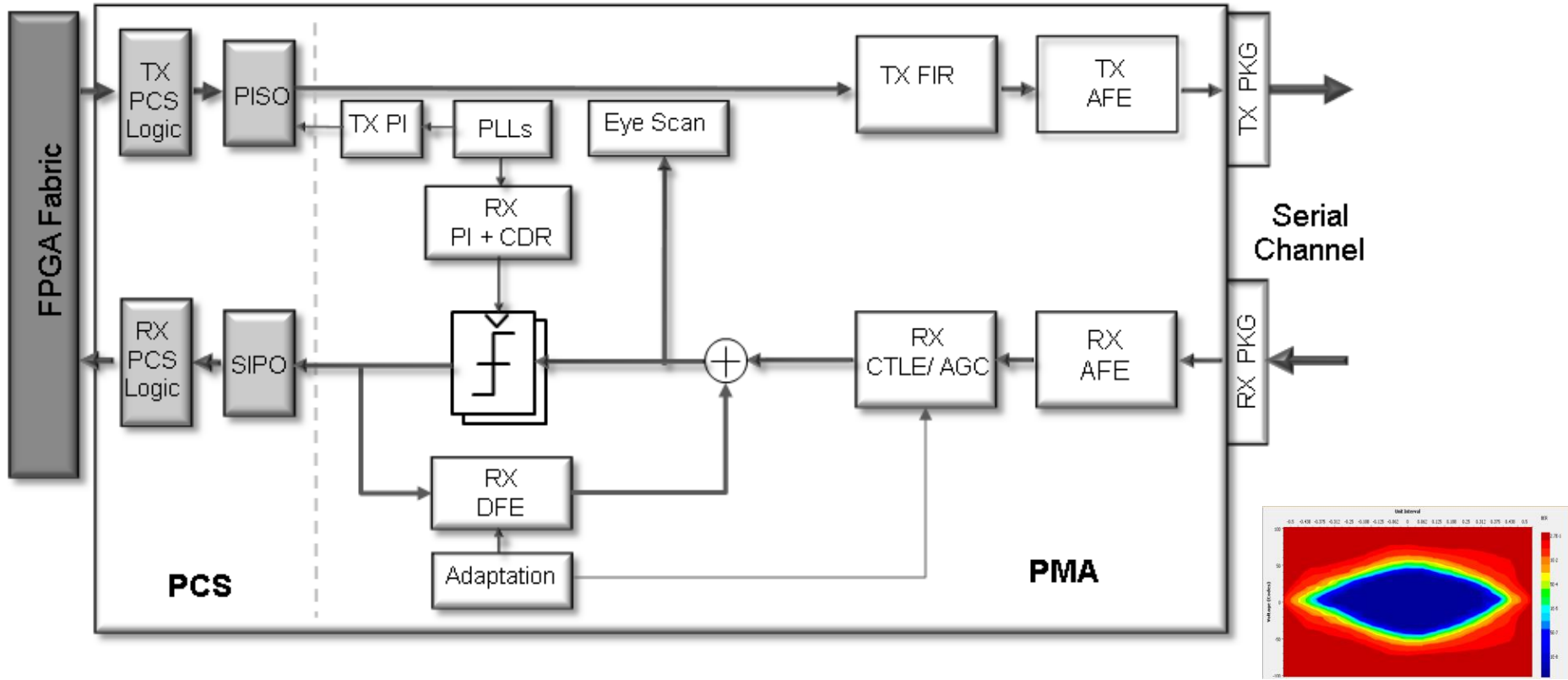
➤ Xilinx UltraScale IBIS-AMI transceiver model

- Virtex GTY (20 nm, 30.5 Gbps)
- Revision V2.1

➤ PVT definition used in this presentation

- Setting TXPVT to 0 implies the TX model is
 - ❖ Process = TT, Voltage = nominal, and Temperature = room model.
- Setting RXPVT to 0 implies the RX model is
 - ❖ Process = TT, Voltage = nominal, and Temperature = room model.

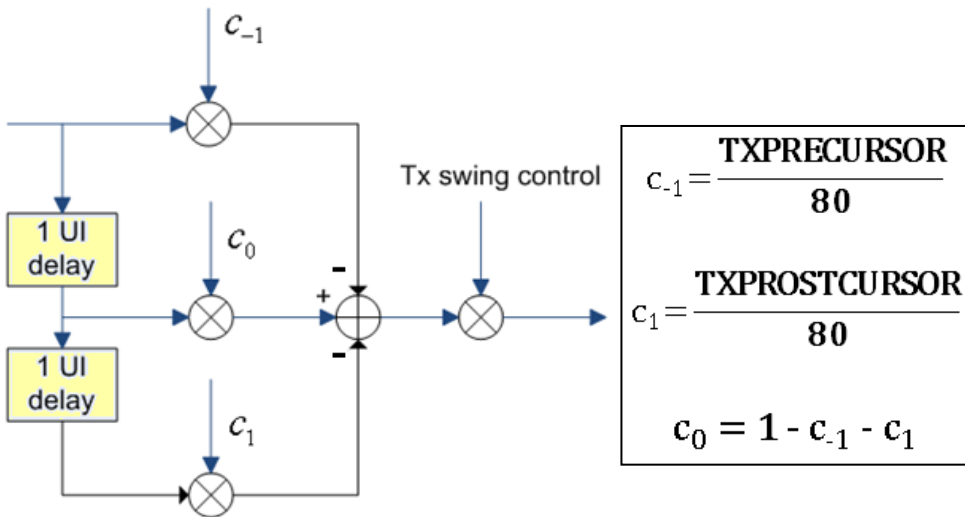
Xilinx Transceiver Architecture Overview



TX IBIS-AMI Model Parameters

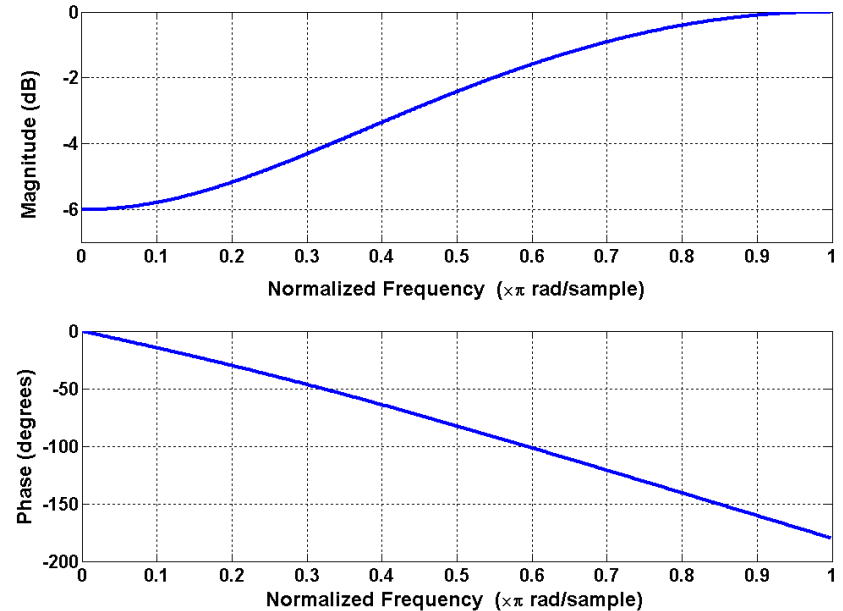
➤ TX FIR De-emphasis

- TXDIFFCTRL: TX swing control, 0 - 31.
- TXPRECURSOR: FIR pre-cursor, 0 - 16.
- TXPOSTCURSOR: FIR post-cursor, 0 - 31.



➤ TX FIR Equalization Example

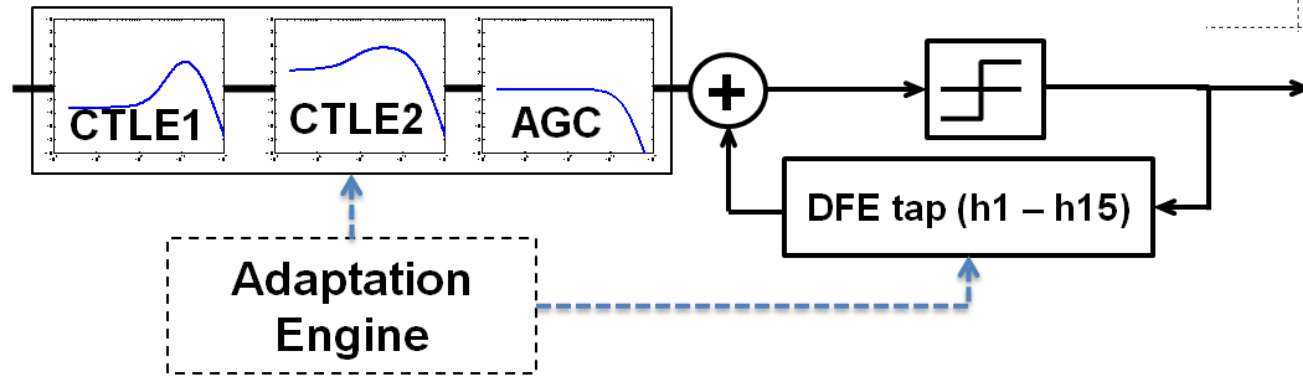
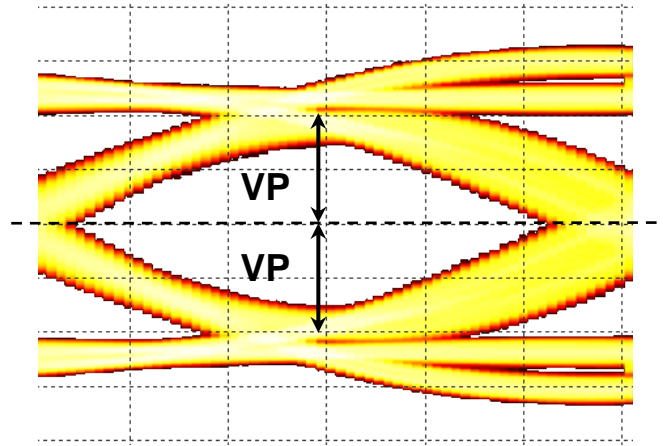
- TXPRECURSOR = 6.
- TXPOSTCURSOR = 14.



RX IBIS-AMI Model Parameters

➤ GTY RX EQ overview and terminology

- CTLE1 = KH
- CTLE2 = KL
- VP = h0 (error slicer level)
- UT = h1 (DFE first tap)



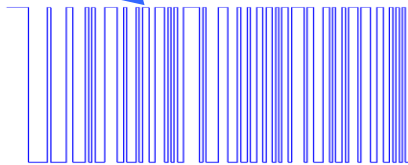
IBIS-AMI Simulation Flow Highlights

IBIS-AMI Model Vs. EDA Tools

- EDA tools compute the channel impulse response (including package, link channel(s), TX and RX IBIS portion).
- EDA tools send the ideal waveform to TX AMI model.
- TX AMI output data is convolved with the cascaded channel impulse response by EDA tools before the data is send to the RX model.
- RX AMI processes the received signal (equalization and time recovery, etc.) and sends the output to EDA tools.
- EDA tools do statistical post processing analysis (bathtub curves, eye diagram, BER contours, etc.) over the RX AMI output data.

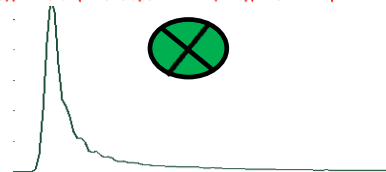
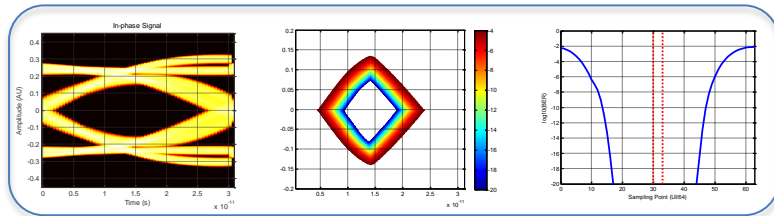
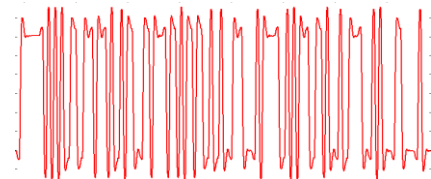
Time-Domain Simulation Data Flow

Data pattern
oversampled by SPB

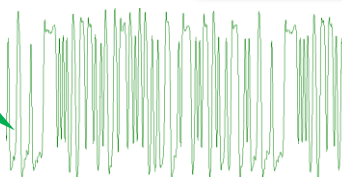


TX
GetWave

Data pattern
oversampled by SPB



Signal at
data
sampler

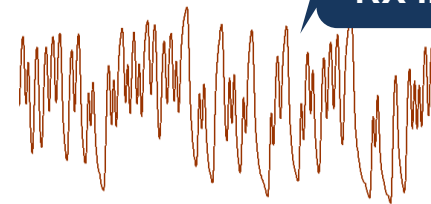


Clock
ticks



RX
GetWave

Signal at
RX input



Clock Ticks

- Clock ticks represent the adapted CDR sampling phase. They are the output from RX GetWave function.
- Xilinx transceiver IBIS-AMI models have an Rx AMI parameter to enable or disable clock ticks, while clock ticks are always available.
- Clock ticks are a function of time/bit sequence, i.e., the separation between two neighboring ticks are not always 1 UI apart.
- CDR sampling phase is not necessarily (not guaranteed) at the center of the eye, thus
 - Disabling clock ticks and relying on EDA's retiming is often incorrect.
 - CDR sampling phase depends on simulation specific conditions and/or the CDR architecture used in the SerDes design.

EDA Tool

User Interface Highlights

EDA Tools User Interface

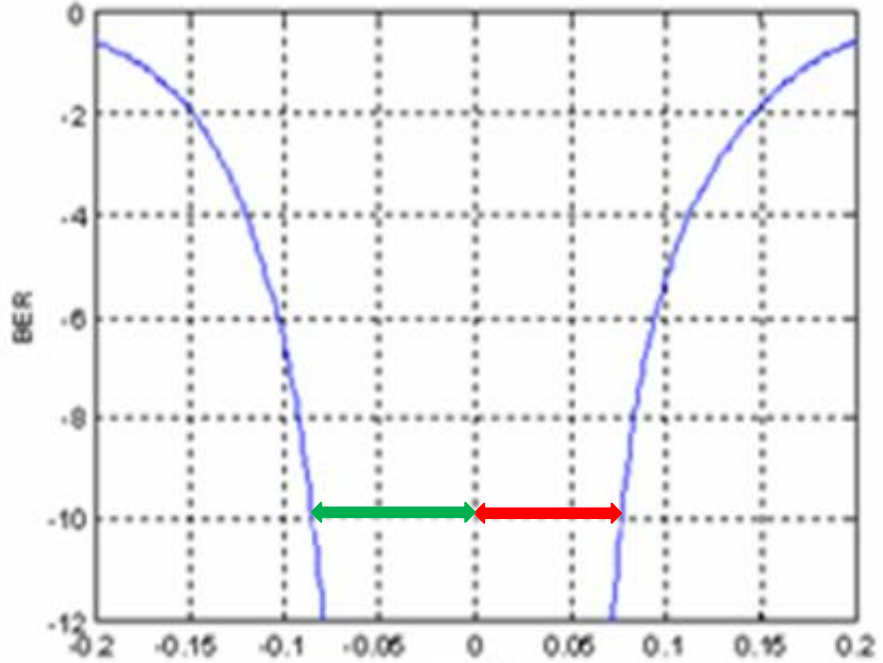
- All but one EDA tool are schematic based.
- For frequent users, both netlist and schematic interfaces are desired.
 - Running simulations in command line, automation, etc...
- Most tools are successful in incorporating all simulation and model parameters in a simple interface.
- Some tools still lack intuitiveness when setting important simulation parameters that can impact simulation results.
- Some jitter and noise parameters are not incorporated in the user interface input.

EDA Tools Results Viewers

- Channel characterization results, such as impulse response, are not easily available in some tools. In many cases the user has to enable a debug parameter in order to obtain these outputs.
- For eye diagrams, some tools have the ability to plot at different BER levels. The user has to be mindful when doing visual inspection.
- In some tools eye measurements (eye height and eye width) at a specific BER are not provided as part of the results.
 - For these particular tools, the user needs to derive the measurements using the bathtub curves and using simple math.
 - User must be careful when doing manual measurement on bathtub curves.

Eye Height Manual Computation

- Step 1:** Generate voltage (vertical) bathtub curve at the given BER, for example, at $1e-10$.
- Step 2:** Measure the upper and lower EH, UEH (red) and LEH (green).
- Step 3:** Compute EH based on $EH = 2 \times \min\{UEH, LEH\}$.

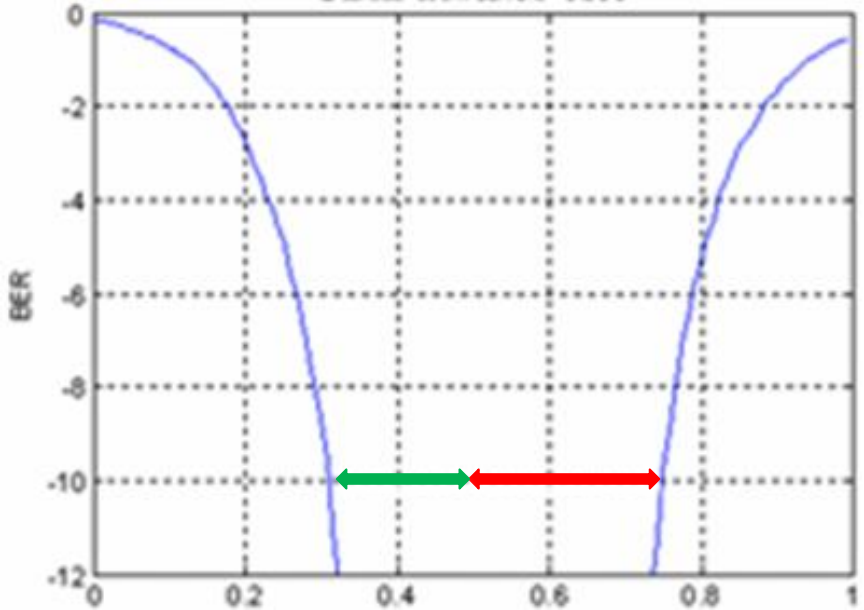


Eye Width Manual Computation

Step 1: Generate time (horizontal) bathtub curve at the given BER, for example, at $1e-10$.

Step 2: Measure the right and left EW, REW (red) and LEW (green).

Step 3: Compute EW based on EW = $2 \times \min\{\text{REW}, \text{LEW}\}$.



EDA Tool Simulation of Three Cases

Simulation Cases Description

➤ Case 1

- 25 Gbps serial link IBIS-AMI simulation with no jitter or noise impairments added to the analysis.

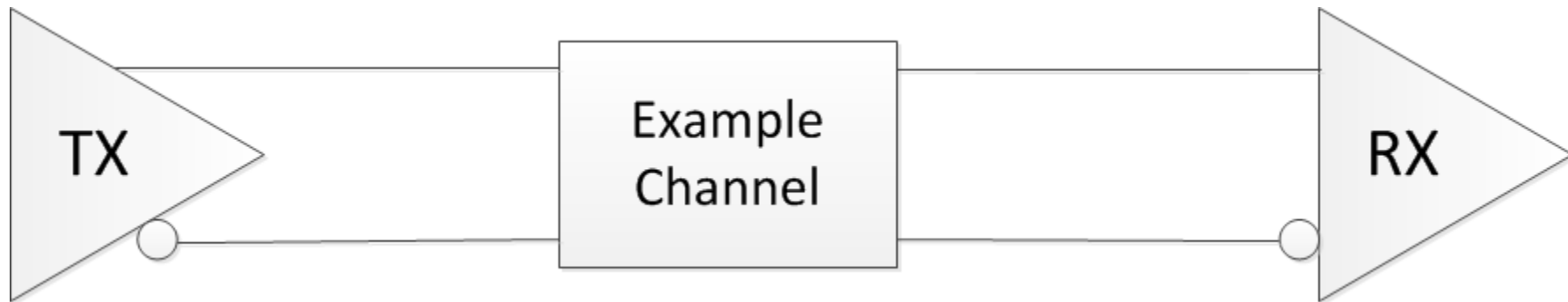
➤ Case 2

- 25 Gbps serial link IBIS-AMI simulation with jitter and noise impairments added to the analysis.

➤ Case 3

- 25 Gbps serial link IBIS-AMI simulation with crosstalk, jitter and noise impairments added to the analysis.

Simulation Case 1



**25Gbps Thru Channel Simulation
Without Jitter or Noise Impairments**

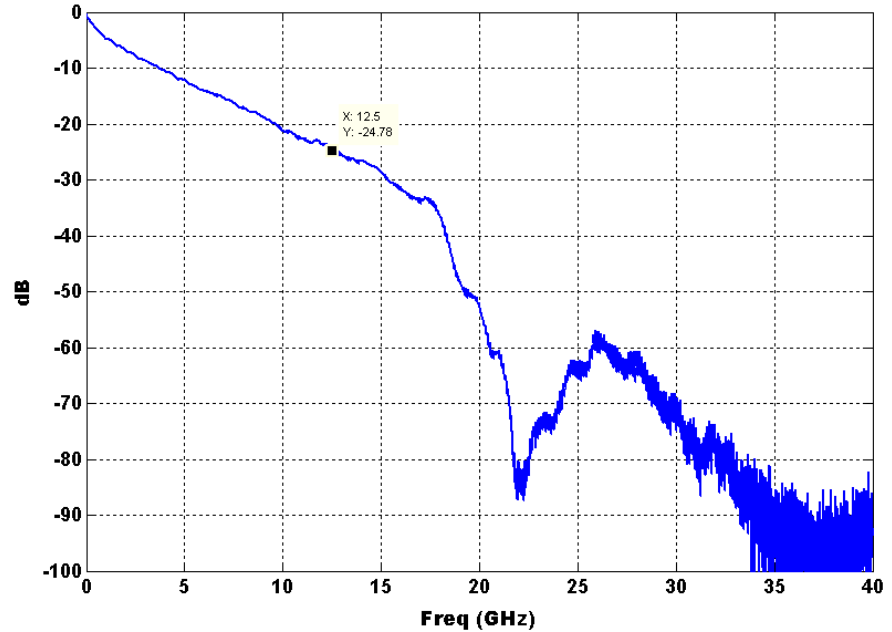
Simulation Configuration for Case 1

Simulation Setup	EDA Configuration		AMI Model Specific	
	TX	RX	TX	RX
Data Rate: 25Gbps	RJ 0	RJ 0	TXPVT 0	RXPVT 0
Pattern: PRBS-15	DJ 0	DJ 0	TXDIFFCTRL 31	DFE Auto-Adapt Enabled
Samples Per Bit: 64	DCD 0	DCD 0	TXPRECURSOR 6	CTLE Auto-Adapt Enabled
AMI Processing Block size: 4,096	-	RN 0	TXPOSTCURSOR 14	AGC Auto-Adapt Enabled
Ignore Bits: 250E3				
Recording Bits: 1E6				

Link Channel Description

➤ Thru Channel

- Data measured with Keysight N5245A
- S4P Touchstone File v1.0
- Frequency range: 10MHz to 40GHz
- Frequency step: ~3.124MHz



Channel IPR (Impulse Response)

- Impulse Response is defined as the response (output) from a system when an “impulse” is the input. Generally,

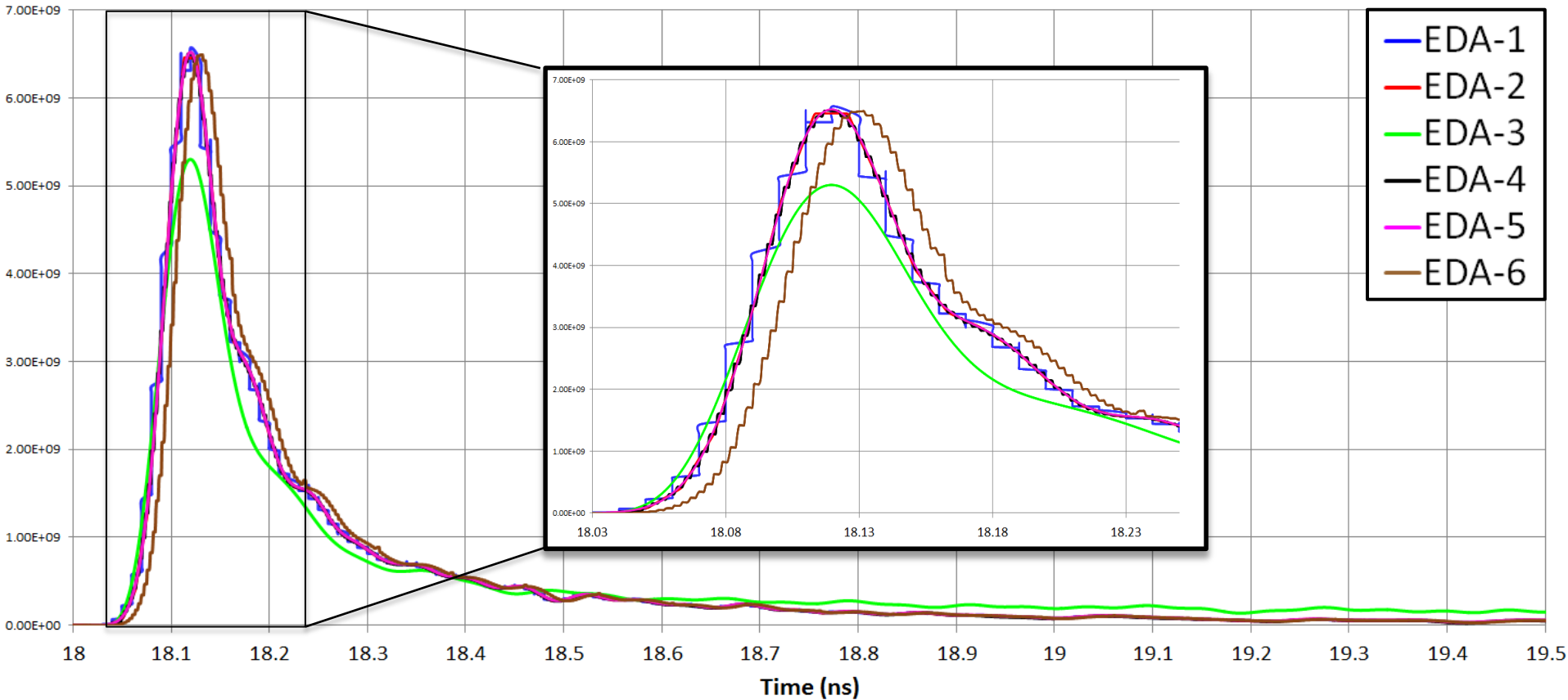


- When the impulse is the input to a system, the output becomes the impulse response.



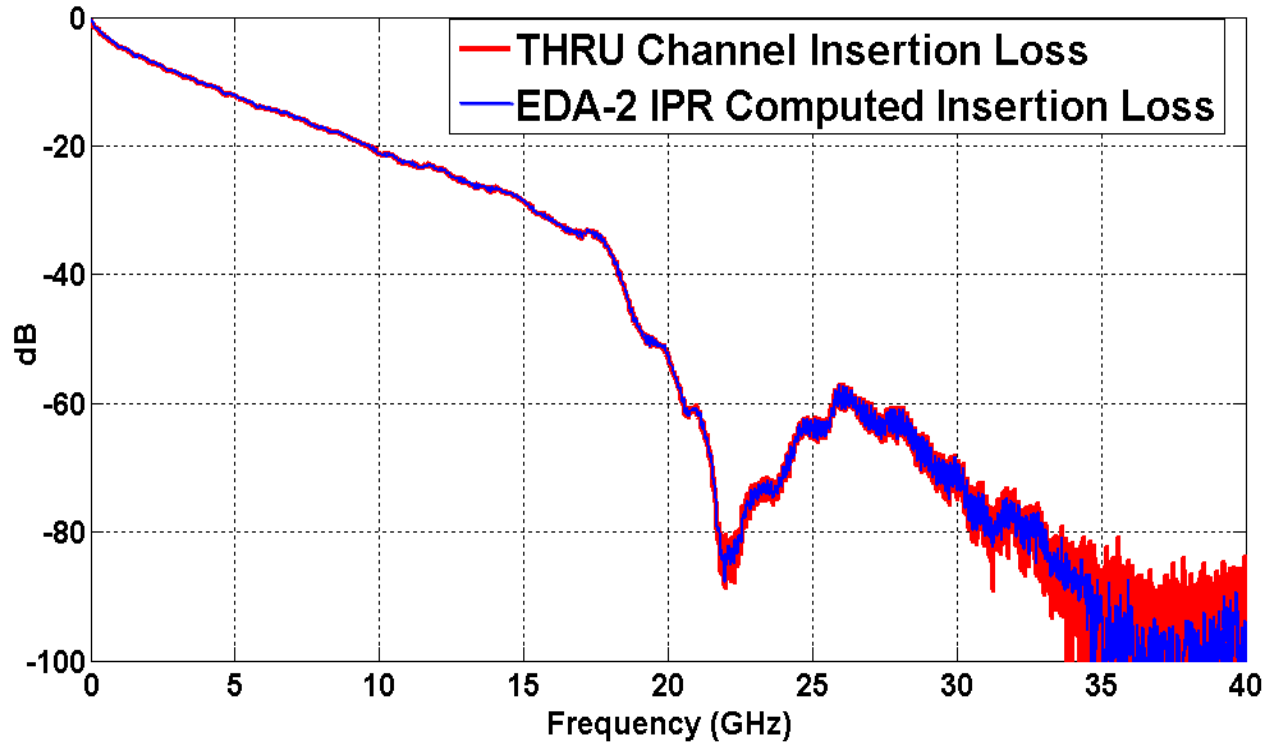
- The impulse response fully characterizes a LTI system.
- Most PCB (line cards, backplanes, etc.) and cables can be treated as LTI system.
- Once the impulse response and the input signal are known, the output of the system is obtained simply by taking the convolution of the input and the impulse response.

Channel IPR Generated by EDA Tools



IPR to THRU Channel Insertion Loss

- IPR from EDA-2 looks smooth and has the most commonality with other EDAs.
- We computed the THRU channel insertion loss and compared it with the original one. The match is reasonable.



Observations in Generated Channel IPR's

➤ The following are observed from the generated impulse responses

- Channel IPRs do not look the same: some are smooth, some are rugged; some small, some big; one has more delay than the others.
 - EDA-1's IPR looks the most rugged, and EDA-6 is the next most rugged.
 - EDA-3's IPR magnitude is much smaller (~20%) than the rest and has a different profile.
 - EDA-3's IPR also has a tail that decays more slowly than the rest.
 - EDA-6's IPR delay is much longer ($>UI/4$ at 25Gbps) than the rest.
- If IPR was truly used in generating channel output waveforms, its magnitude would affect adaptation, and its delay would affect CDR locking phase.
- It is noticed that eye diagrams do not quite show the differences; this is largely due to the fact that adaptations drive the equalized waveform to the same target.
- The differences in IPR magnitude or profile are more of a concern to the end users. System margin could be miscalculated without notice.

Output Eye Diagrams at BER 1e-6

EDA-1

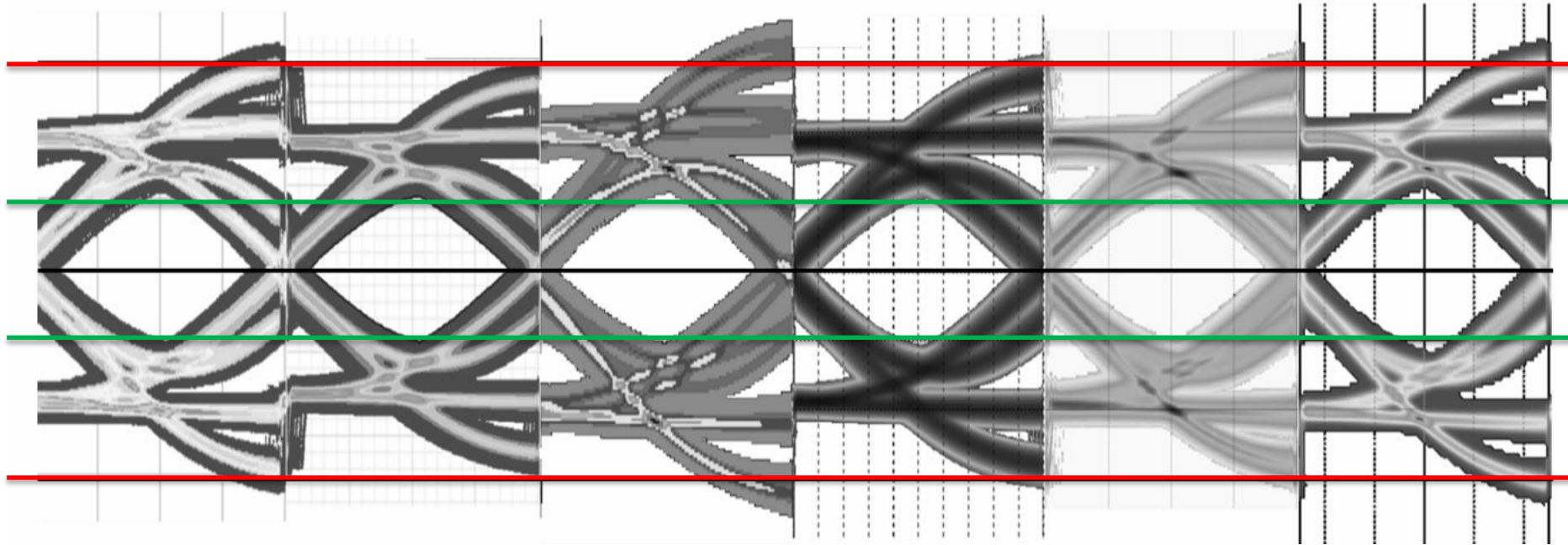
EDA-2

EDA-3

EDA-4

EDA-5

EDA-6

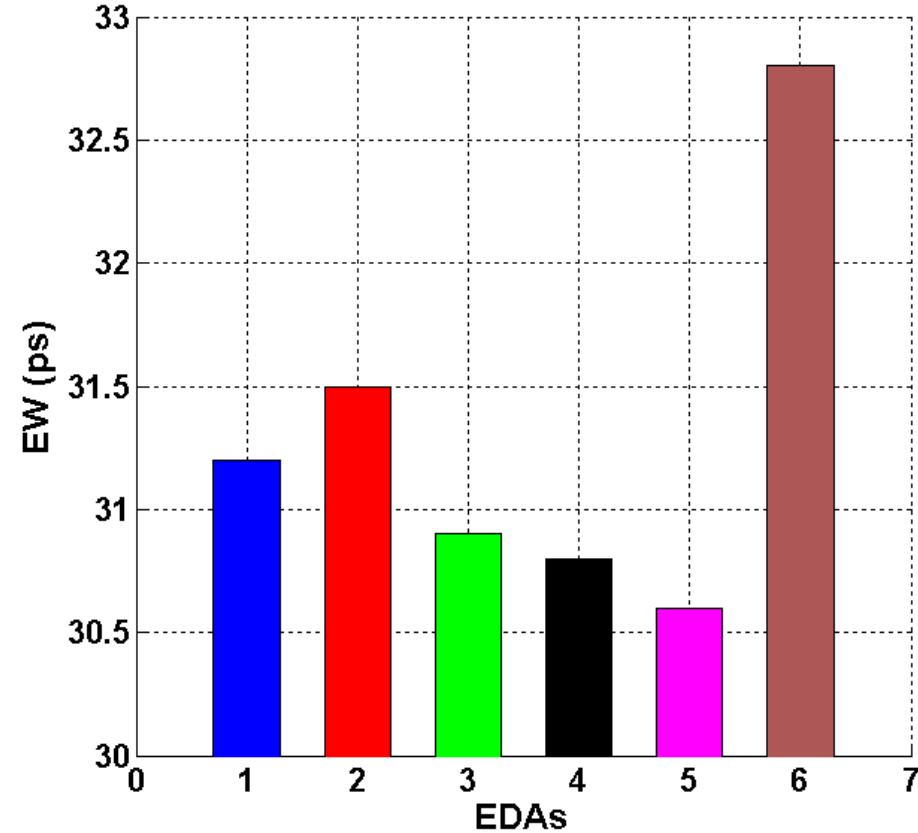
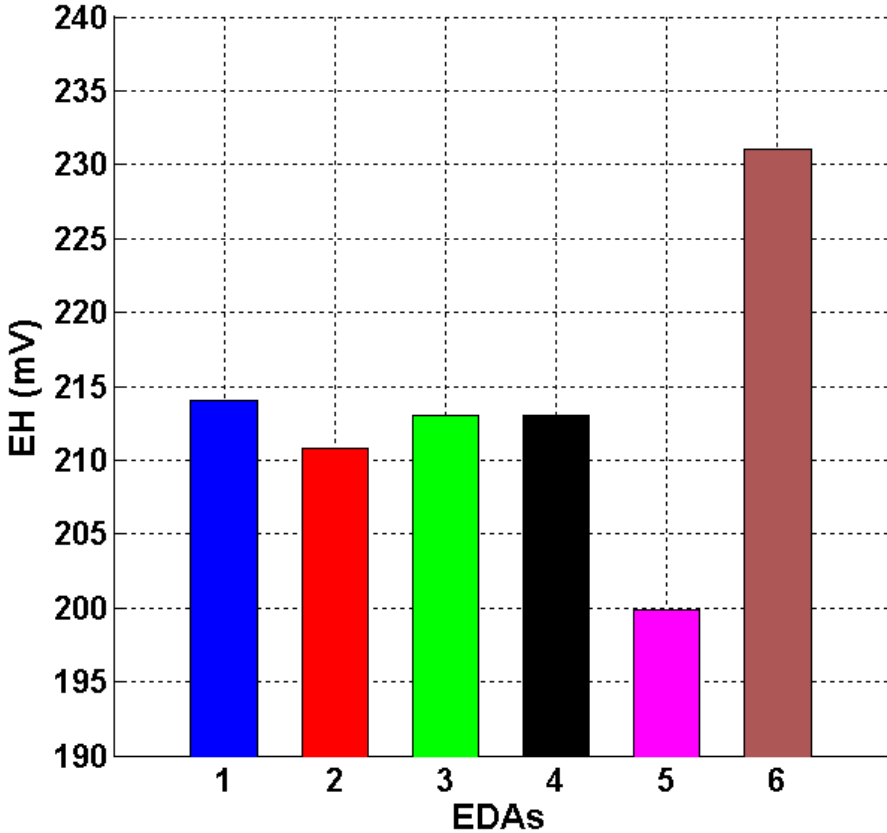


➤ Color mapping scheme could affect eye appearance

Eye Diagram Observations for Case 1

EDAs	EDA-1	EDA-2	EDA-3	EDA-4	EDA-5	EDA-6
Outer Eye	-	Smallest	Largest	-	-	-
Inner Eye	-	-	-	-	Smallest	Largest
Eye Shape	All look similar					
	-	-	The outermost traces bifurcated	-	-	-

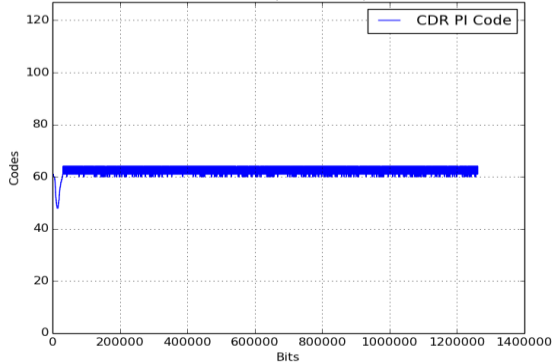
Eye Metrics @ BER = 1e-12 for Case 1



CDR Adaptations for Case 1

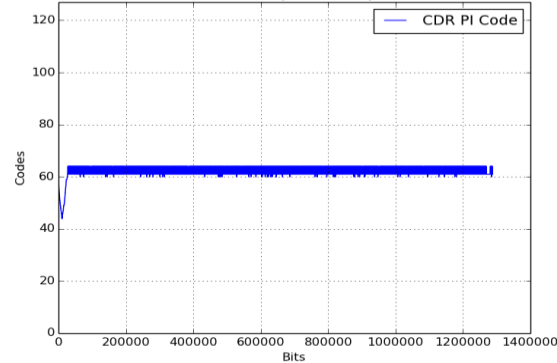
EDA-1

CDR PI Adaptation Output



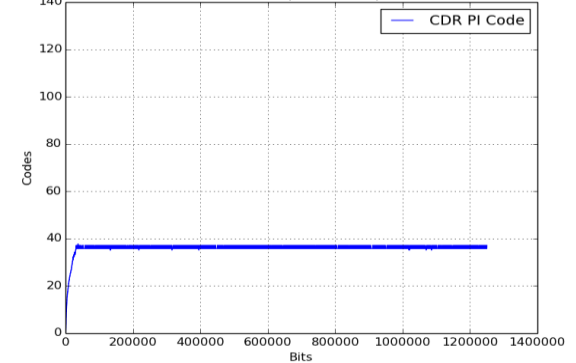
EDA-2

CDR PI Adaptation Output



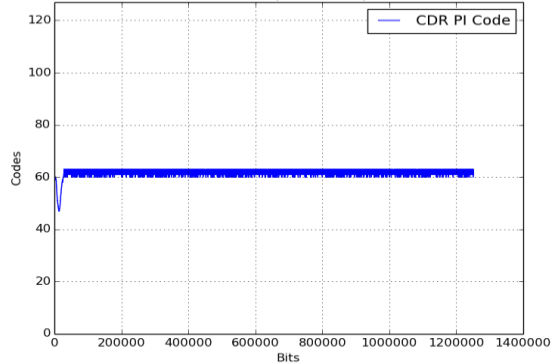
EDA-3

CDR PI Adaptation Output



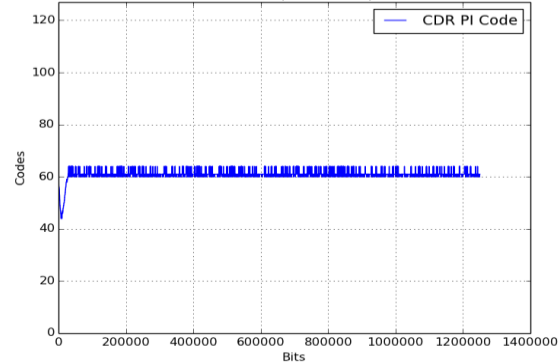
EDA-4

CDR PI Adaptation Output



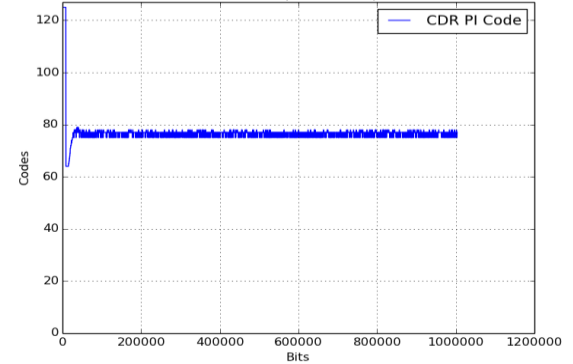
EDA-5

CDR PI Adaptation Output



EDA-6

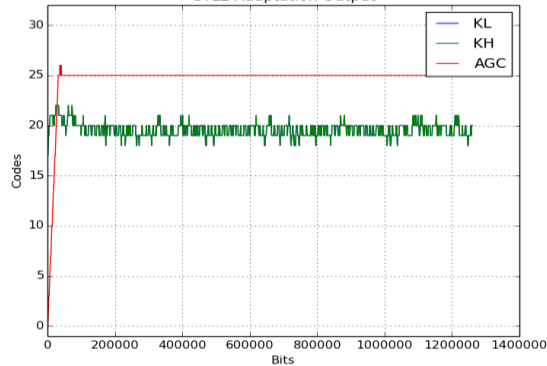
CDR PI Adaptation Output



CTLE & AGC Adaptation for Case 1

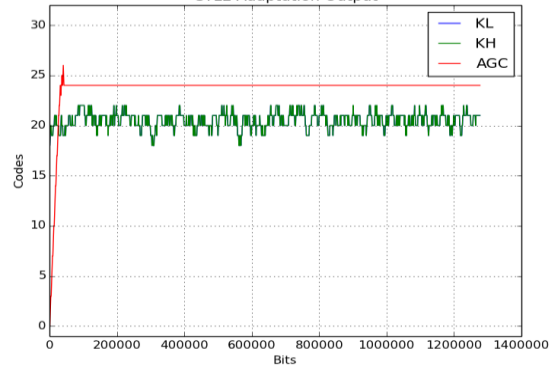
EDA-1

CTLE Adaptation Output



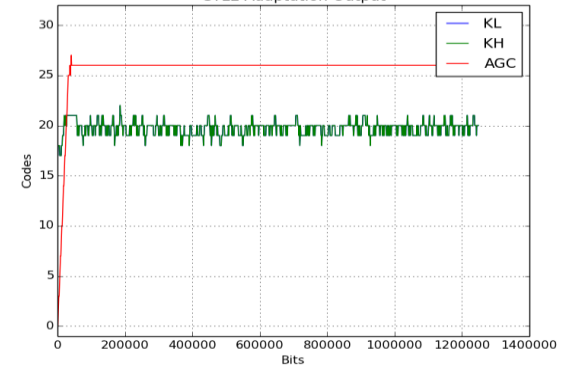
EDA-2

CTLE Adaptation Output



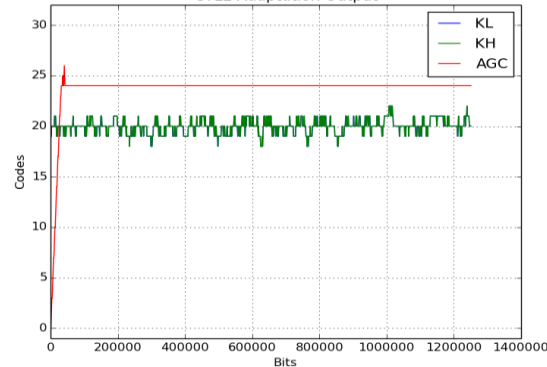
EDA-3

CTLE Adaptation Output



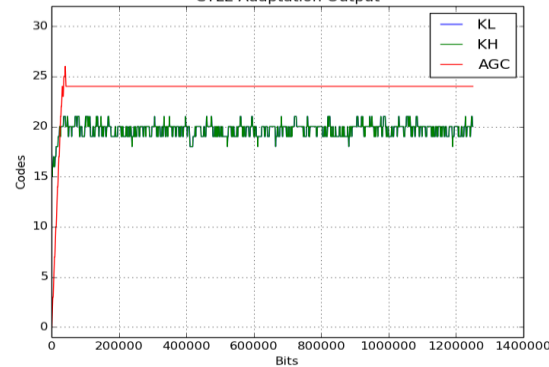
EDA-4

CTLE Adaptation Output



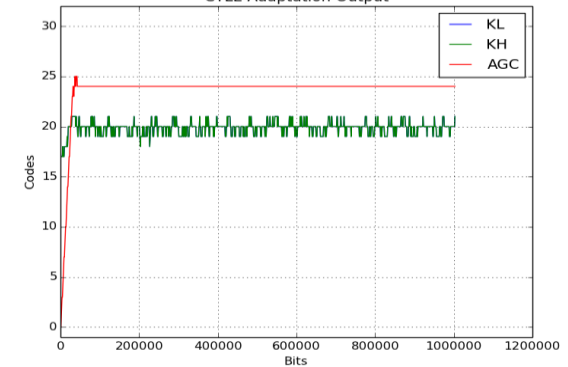
EDA-5

CTLE Adaptation Output



EDA-6

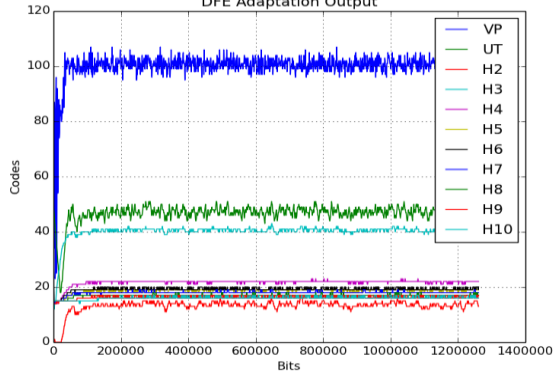
CTLE Adaptation Output



DFE Adaptations for Case 1

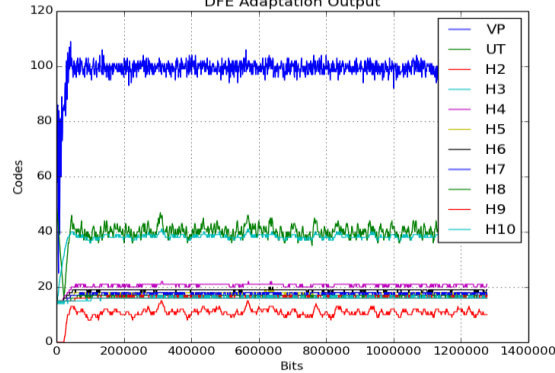
EDA-1

DFE Adaptation Output



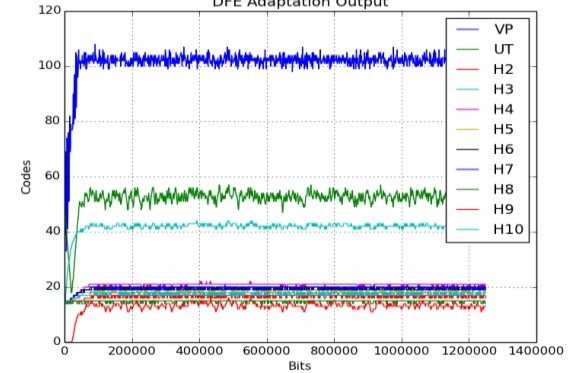
EDA-2

DFE Adaptation Output



EDA-3

DFE Adaptation Output



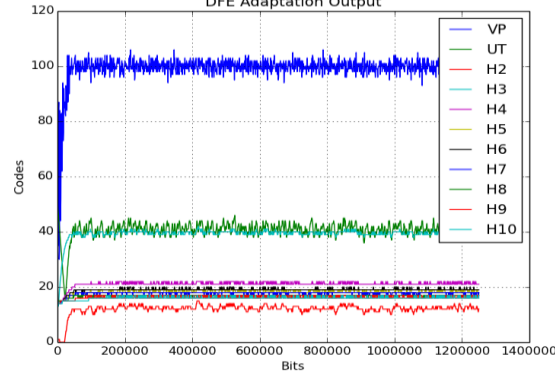
EDA-4

DFE Adaptation Output



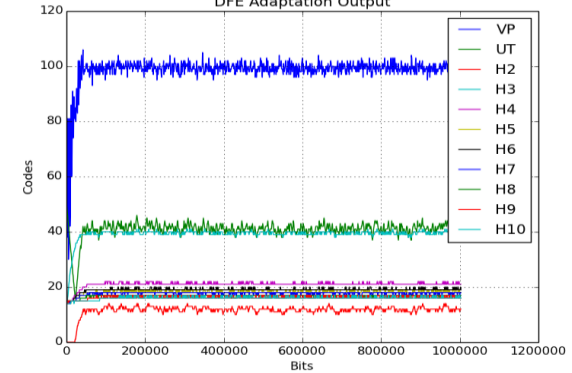
EDA-5

DFE Adaptation Output



EDA-6

DFE Adaptation Output



More Observations for Case 1

EDAs	EDA-1	EDA-2	EDA-3	EDA-4	EDA-5	EDA-6
AGC	25	24	26	24	24	24
CTLE	18 – 21	18 – 21	18 – 21	18 – 21	18 – 21	18 – 21
VP (h0)	~100	~100	~102	~100	~100	~100
UT (h1)	~48	~41	~55	~43	~41	~43
h2	~14	~12	~14	~12	~13	~12
h3	~41	~39	~43	~39	~40	~40
CDR	~62	~62	~38	~62	~61	~77
EH @ 1e-12	–	–	–	–	Smallest	Largest
EW @ 1e-12	–	–	–	–	Smallest	Largest

Discussion on Case 1 Simulation Results

➤ CDR adaptations

- EDA-3's CDR results are not expected from its IPR's delay.
- EDA-6's CDR is ~25% UI delayed, matching its IPR's delay compared with IPRs from other EDAs.

➤ CTLE adaptations

- All six EDAs yielded similar convergence.

➤ AGC adaptations

- Out of six EDAs, four resulted in AGC=24, one (EDA-1) in AGC=25, and one (EDA-3) in AGC=26.
- EDA-3's AGC adaptation result is likely due to its smaller IPR magnitude.

Discussion on Case 1 Simulation Results (Con't)

➤ DFE tap adaptations

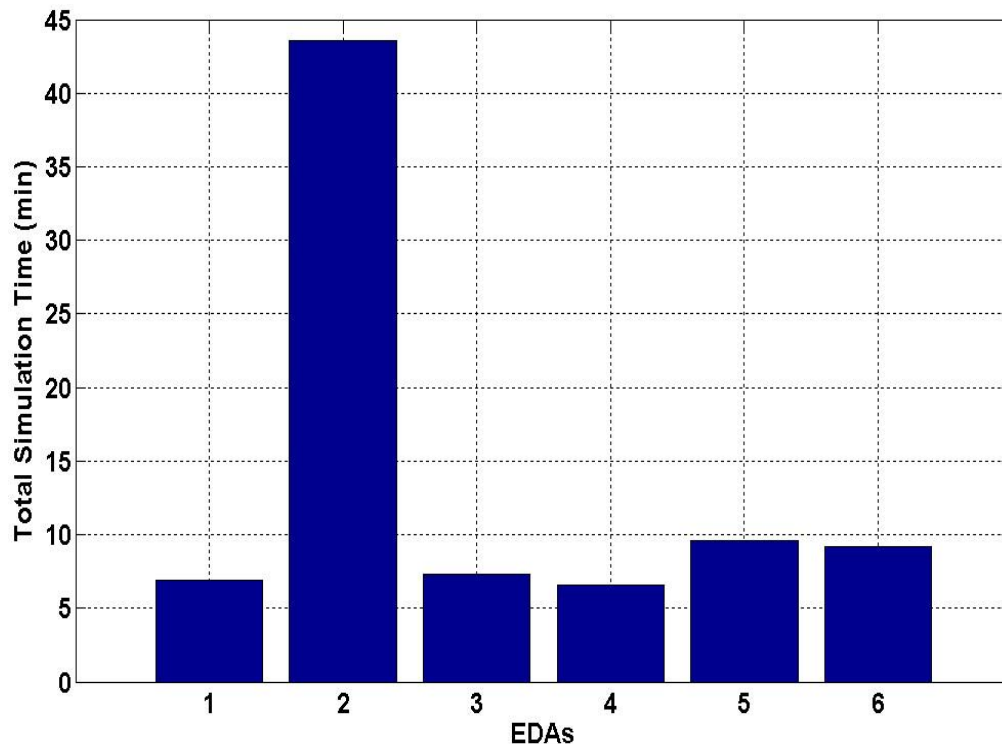
- VP adaptation results are almost identical among all six EDAs.
- For UT tap, four EDAs (2, 4, 5, 6) yielded about 41~43.
- EDA-1 generated a slightly larger value, about 48.
- EDA-3 produced a larger UT tap value, about 55 (related to IPR shape).
- EDA-3 produced a larger h2 tap value (related to IPR shape).

➤ Eye metrics (EH and EW at BER=1e-12)

- EDA-5 is on the most pessimistic side, smallest in both EH and EW.
- EDA-6 is on the most optimistic side, largest in both EH and EW.
- EDA-1, EDA-2, EDA-3, EDA-4 have similar EH and EW.

Simulation Time Comparison

- Simulation time is recorded for a total of 1.25M bits, for Case 1
 - Simulation time includes channel IPR characterization;
 - Five out of six EDAs showed a total simulation less than 10 min for 1.25M bits;
 - EDA-2 showed about 6x longer time. It is believed that a lot of time was spent on IPR generation.



Simulation Cases Description

➤ Case 1

- 25 Gbps serial link IBIS-AMI simulation with no jitter or noise impairments added to the analysis.

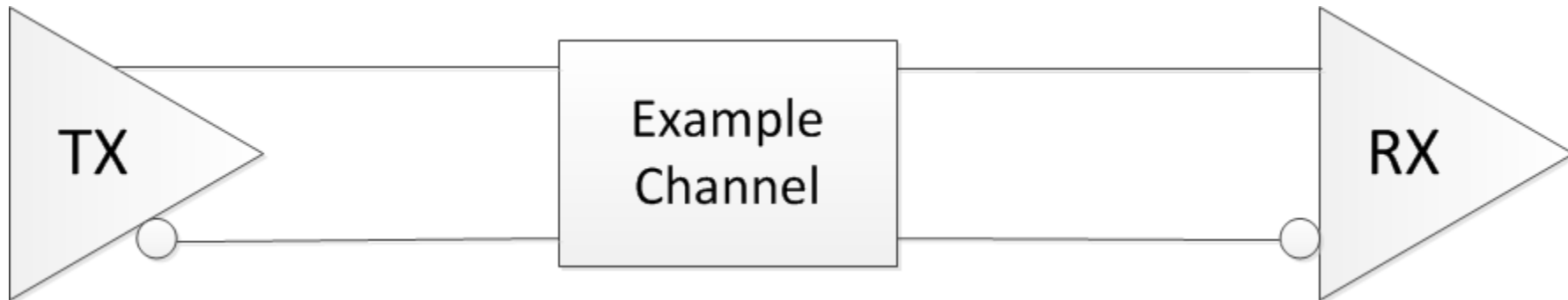
➤ Case 2

- 25 Gbps serial link IBIS-AMI simulation with jitter and noise impairments added to the analysis.

➤ Case 3

- 25 Gbps serial link IBIS-AMI simulation with crosstalk, jitter and noise impairments added to the analysis.

Simulation Case 2



**25Gbps Thru Channel Simulation
With Jitter and Noise Impairments**

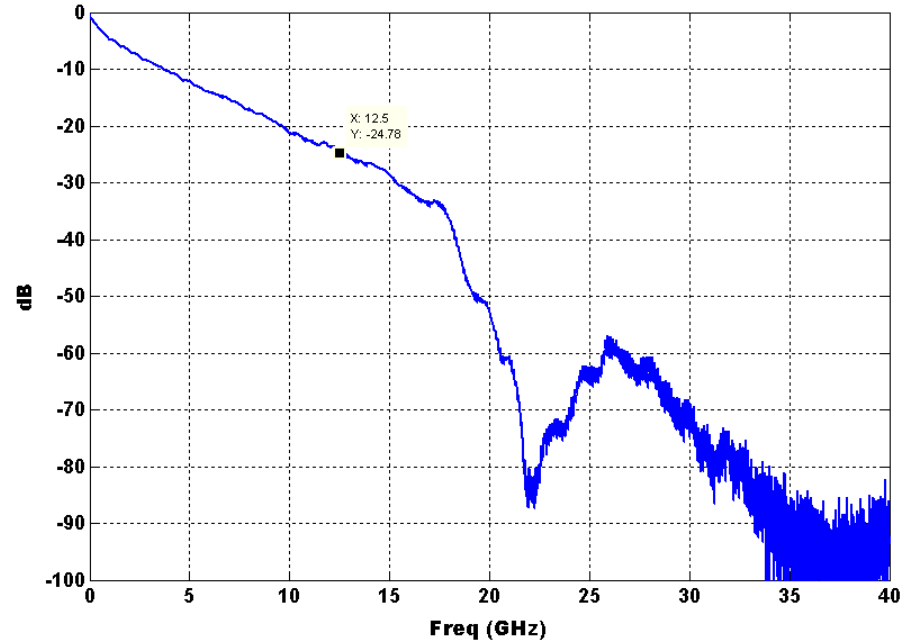
Simulation Configuration for Case 2

Simulation Setup	EDA Configuration		AMI Model Specific	
	TX	RX	TX	RX
Data Rate: 25Gbps	RJ	RJ	TXPVT	RXPVT
Pattern: PRBS-15	0.01 UI	0.01 UI	0	0
Samples Per Bit: 64	DJ	DJ	TXDIFFCTRL	DFE Auto-Adapt
AMI Processing Block size: 4,096	0.04 UI	0.025 UI	31	Enabled
Ignore Bits: 250E3	DCD	DCD	TXPRECURSOR	CTLE Auto-Adapt
Recording Bits: 1E6	0.02 UI	0.01 UI	6	Enabled
	-	RN	TXPOSTCURSOR	AGC Auto-Adapt
		2.5mV	14	Enabled

Link Channel Description

➤ Thru Channel

- Data measured with Keysight N5245A
- S4P Touchstone File v1.0
- Frequency range: 10MHz to 40GHz
- Frequency step: ~3.124MHz



Output Eye Diagrams at BER 1e-6

EDA-1

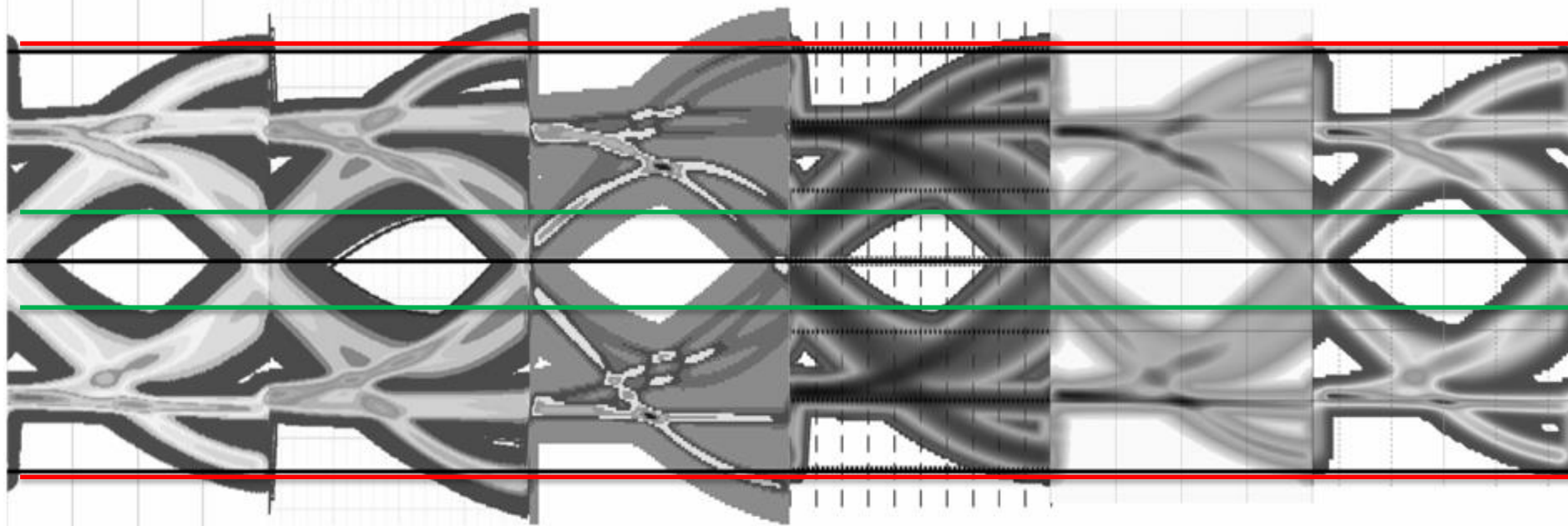
EDA-2

EDA-3

EDA-4

EDA-5

EDA-6

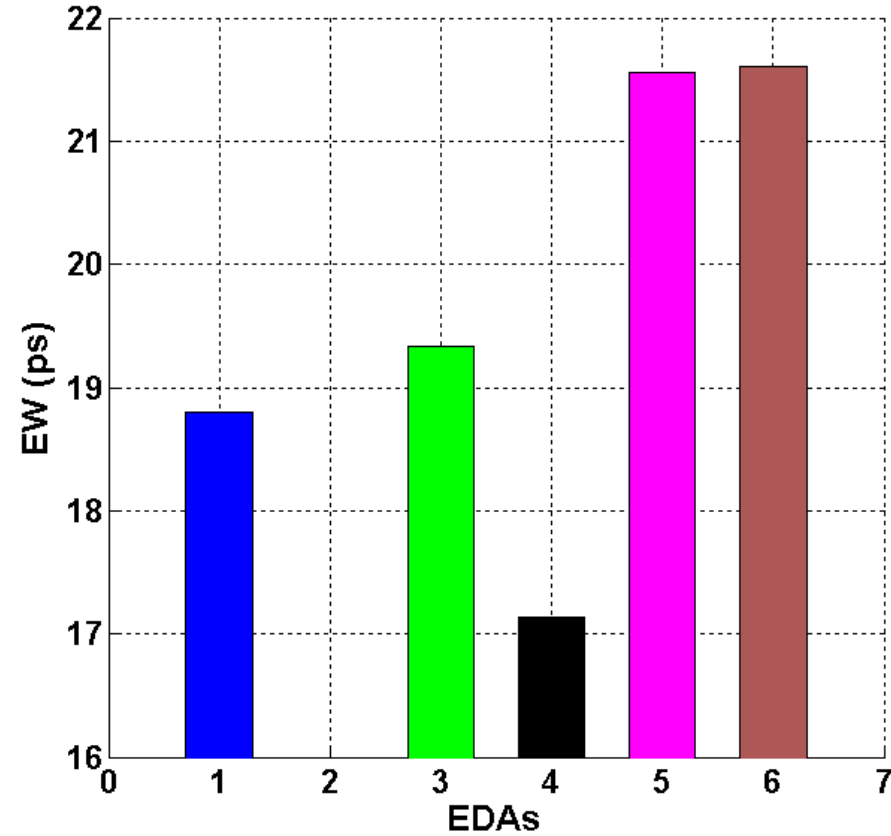
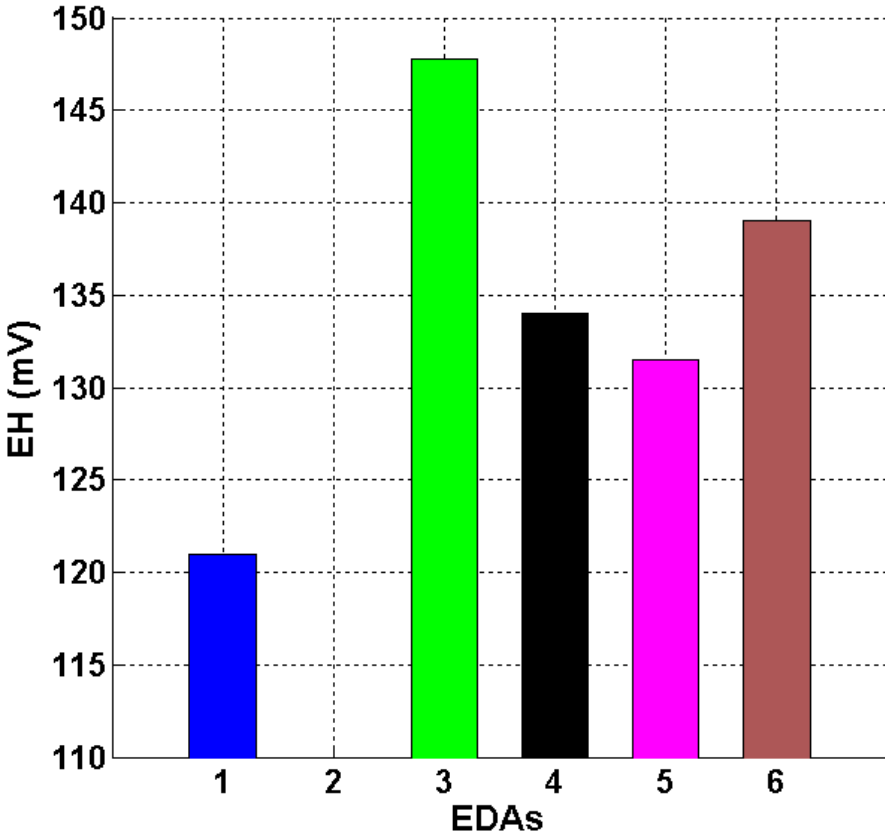


➤ Color mapping scheme could affect eye appearance

Eye Diagram Observations for Case 2

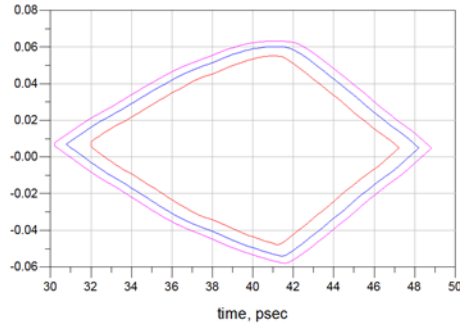
EDAs	EDA-1	EDA-2	EDA-3	EDA-4	EDA-5	EDA-6
Outer Eye	-	-	Largest	-	-	Smallest
Inner Eye	-	-	-	Smallest	Largest	-
Eye Shape	All look similar					
	-	-	The outermost traces bifurcated	-	-	-

Eye Metrics at BER = 1e-12 for Case 2

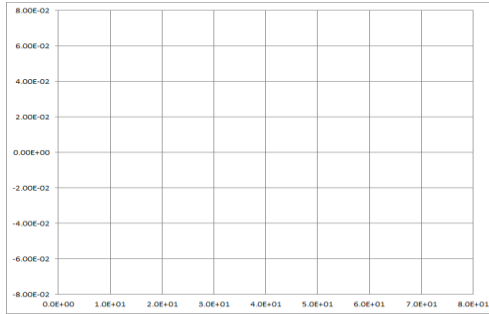


BER Contours for Case 2

EDA-1



EDA-2

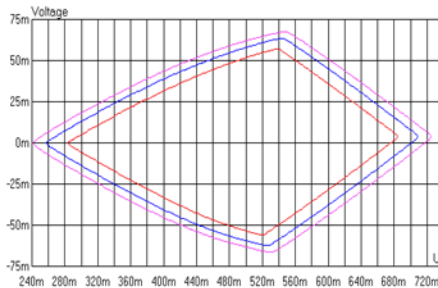


EDA-3 (BER 1e-9)

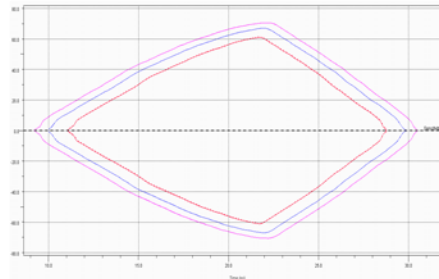


BER Contours (BER 1e-12, 1e-15, 1e-21)

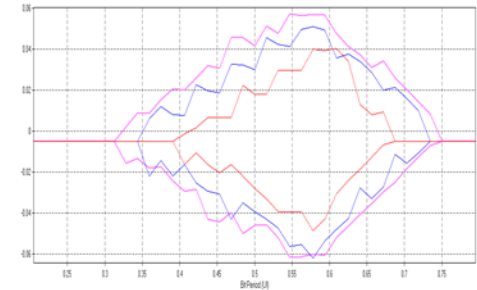
EDA-4



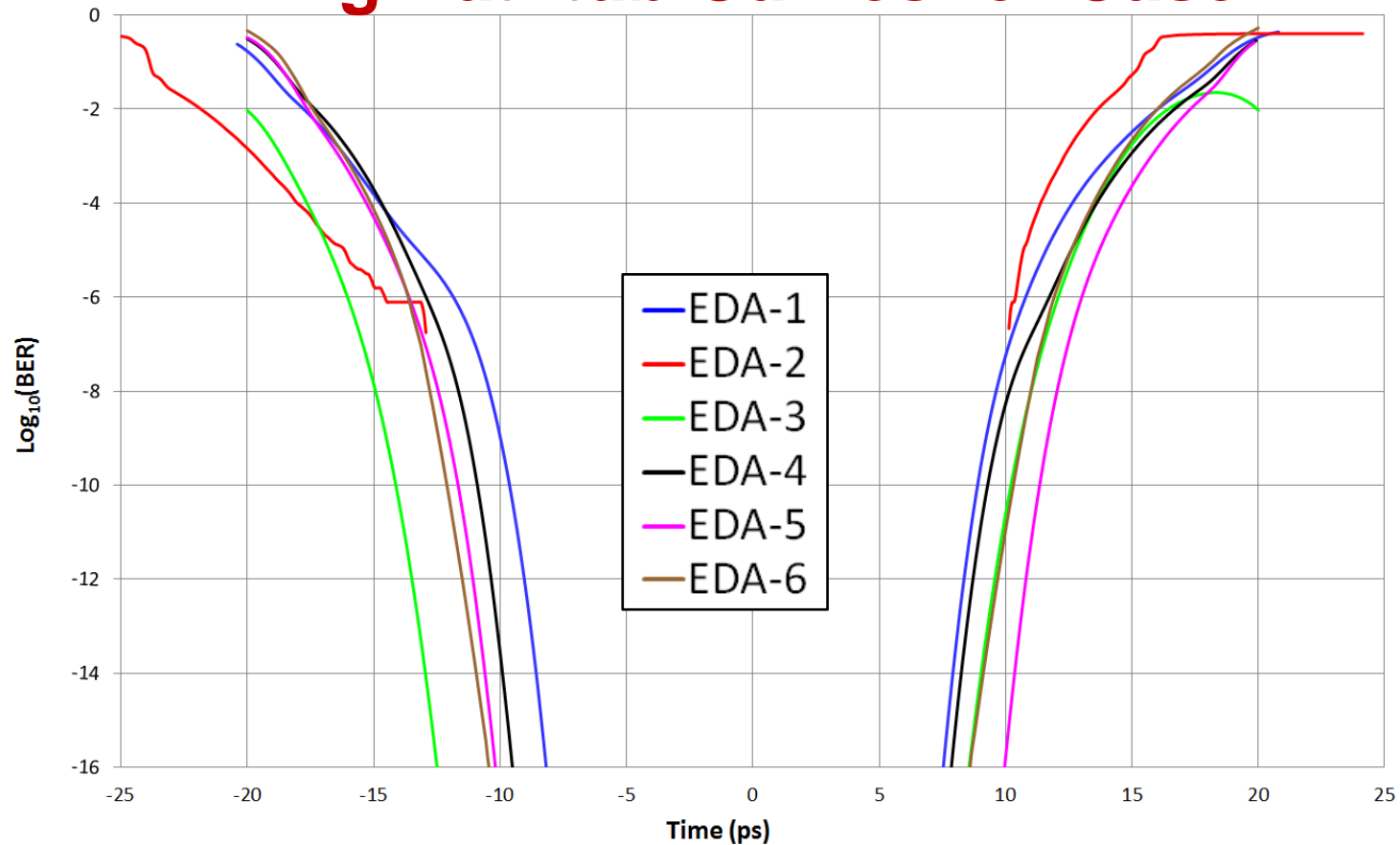
EDA-5



EDA-6



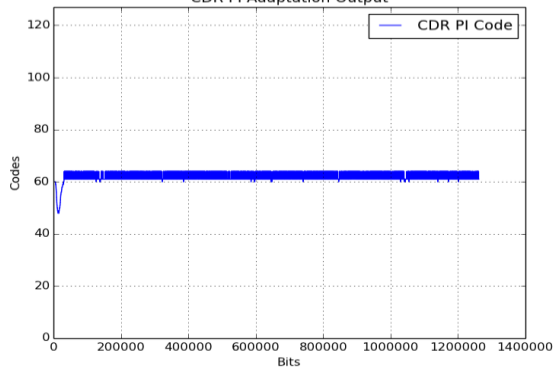
Timing Bathtub Curves for Case 2



CDR Adaptations for Case 2

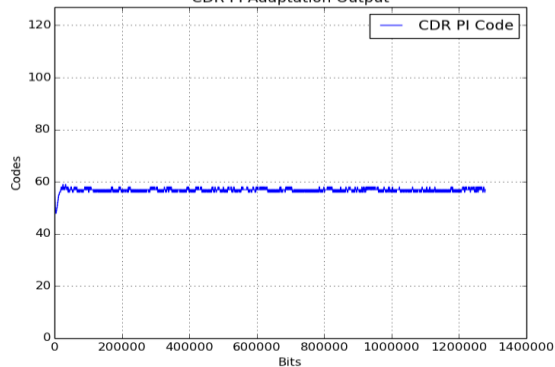
EDA-1

CDR PI Adaptation Output



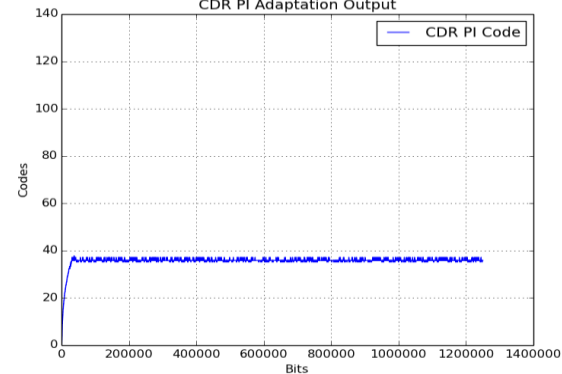
EDA-2

CDR PI Adaptation Output



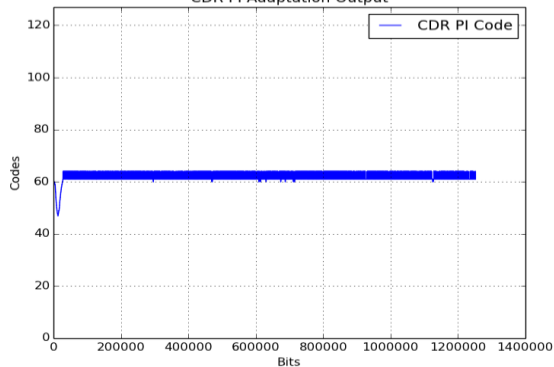
EDA-3

CDR PI Adaptation Output



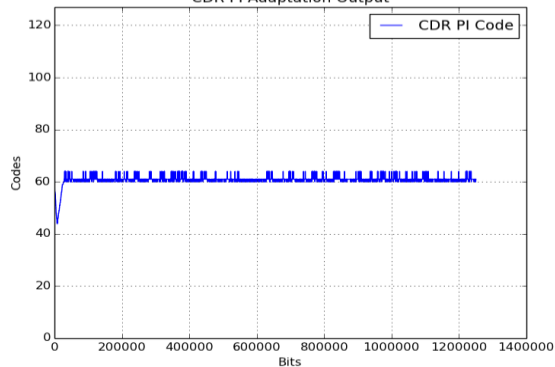
EDA-4

CDR PI Adaptation Output



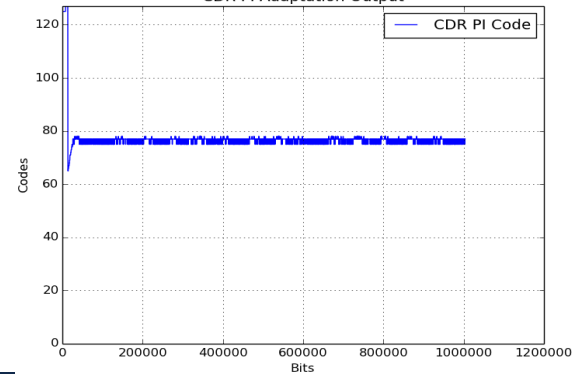
EDA-5

CDR PI Adaptation Output



EDA-6

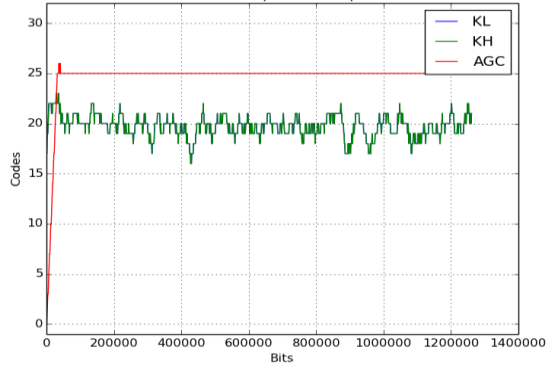
CDR PI Adaptation Output



CTLE & AGC Adaptation for Case 2

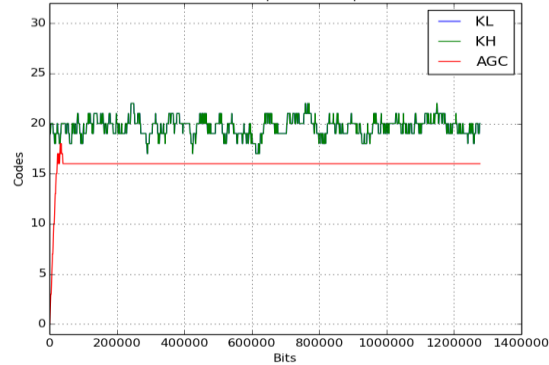
EDA-1

CTLE Adaptation Output



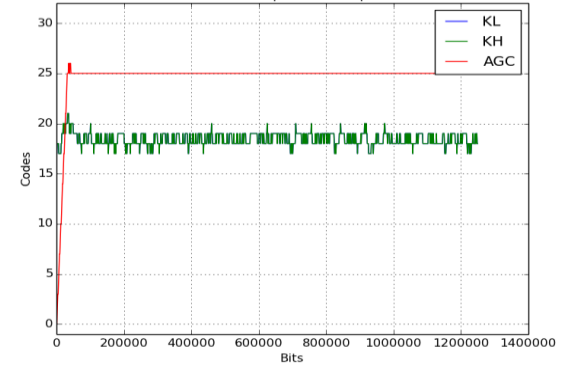
EDA-2

CTLE Adaptation Output



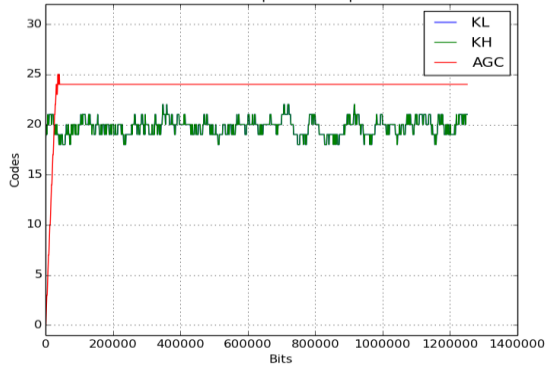
EDA-3

CTLE Adaptation Output



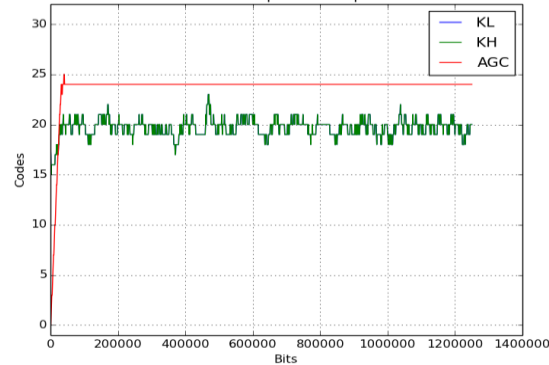
EDA-4

CTLE Adaptation Output



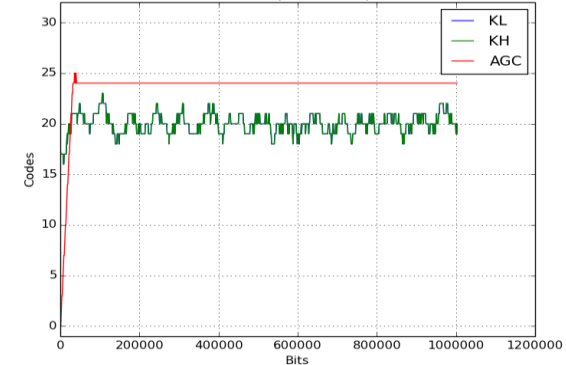
EDA-5

CTLE Adaptation Output



EDA-6

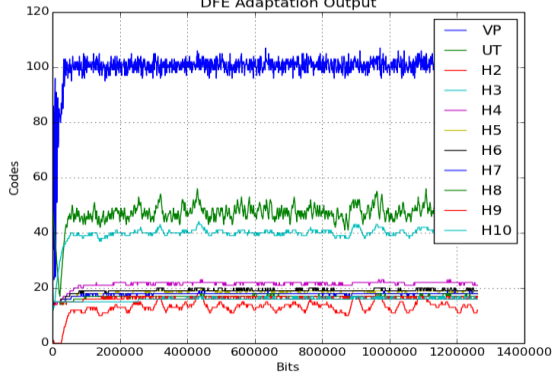
CTLE Adaptation Output



DFE Adaptations for Case 2

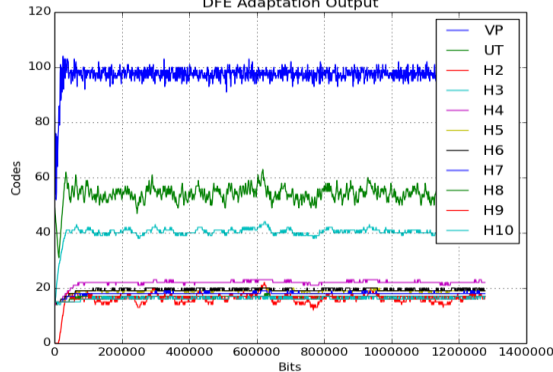
EDA-1

DFE Adaptation Output



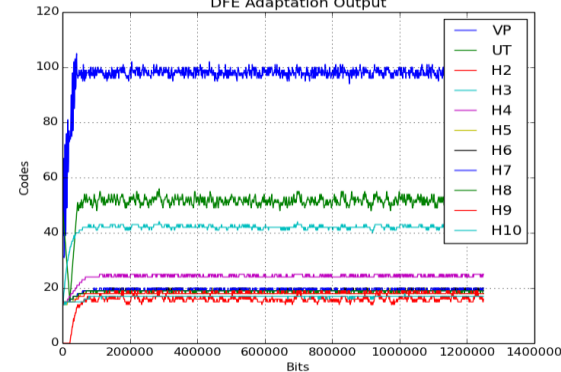
EDA-2

DFE Adaptation Output



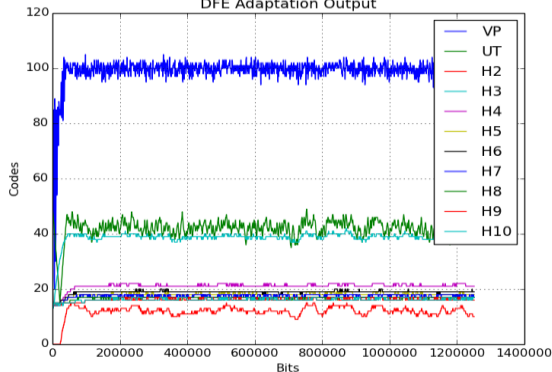
EDA-3

DFE Adaptation Output



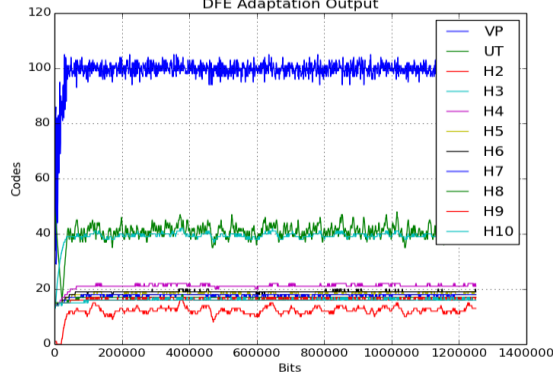
EDA-4

DFE Adaptation Output



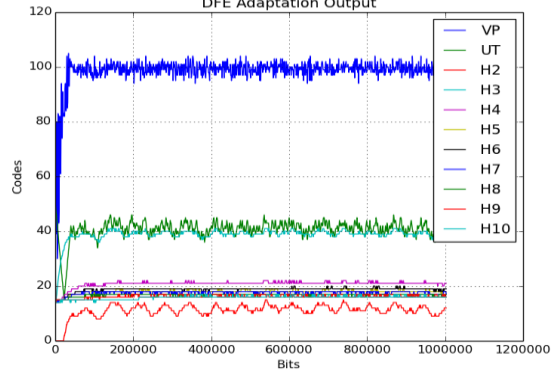
EDA-5

DFE Adaptation Output



EDA-6

DFE Adaptation Output



More Observations for Case 2

EDAs	EDA-1	EDA-2	EDA-3	EDA-4	EDA-5	EDA-6
AGC	25	16	25	24	24	24
CTLE	16 – 22	18 – 22	17 – 20	18 – 22	18 – 23	18 – 23
VP (h0)	~100	~99	~100	~100	~100	~100
UT (h1)	~48	~57	~56	~43	~41	~41
h2	~13	~16	~17	~13	~13	~13
h3	~40	~41	~42	~40	~40	~40
CDR	~61	~58	~38	~61	~61	~77
EH @ 1e-12	Smallest	NA	Largest	–	–	–
EW @ 1e-12	Smallest	NA	–	–	–	Largest

Discussion on Case 2 Simulation Results

➤ CDR adaptations

- EDA-2 CDR adaptation result is unexpectedly affected; it locked about 1/16 UI earlier than that in Case 1.

➤ CTLE adaptations

- All six EDAs generated approximately $CTLE=20$ (same as those in Case 1).

➤ AGC adaptations

- EDA-1 remains unchanged from Case 1, converged to 25.
- EDA-4, EDA-5 and EDA-6 remain unchanged from Case 1, at 24.
- EDA-3 convergence is slightly reduced from 26 to 25.
- EDA-2 is unexpectedly reduced from 24 to 16, which is an outlier.

Discussion on Case 2 Simulation Results (Con't)

➤ DFE tap adaptations

- EDA-2 has UT and DFE tap noticeably changed, which is an outlier.

➤ Eye metrics (EH and EW at BER=1e-12)

- We could not generate EH or EW from EDA-2, as of this date.
- EDA-1 has the most EH and EW reduction, compared with Case 1.
- EDA-3 has the least EH reduction, compared with Case 1.
- EDA-5 has the least EW reduction, compared with Case 1.

➤ Bathtub curves

- The six EDAs generated very different bathtub curves, including curve slopes.
- We could not extrapolate beyond 1e-6 in EDA-2, so the EH/EW data it is left blank.
- The conclusion for system margin could be different using different EDA tools.

Simulation Cases Description

➤ Case 1

- 25 Gbps serial link IBIS-AMI simulation with no jitter or noise impairments added to the analysis.

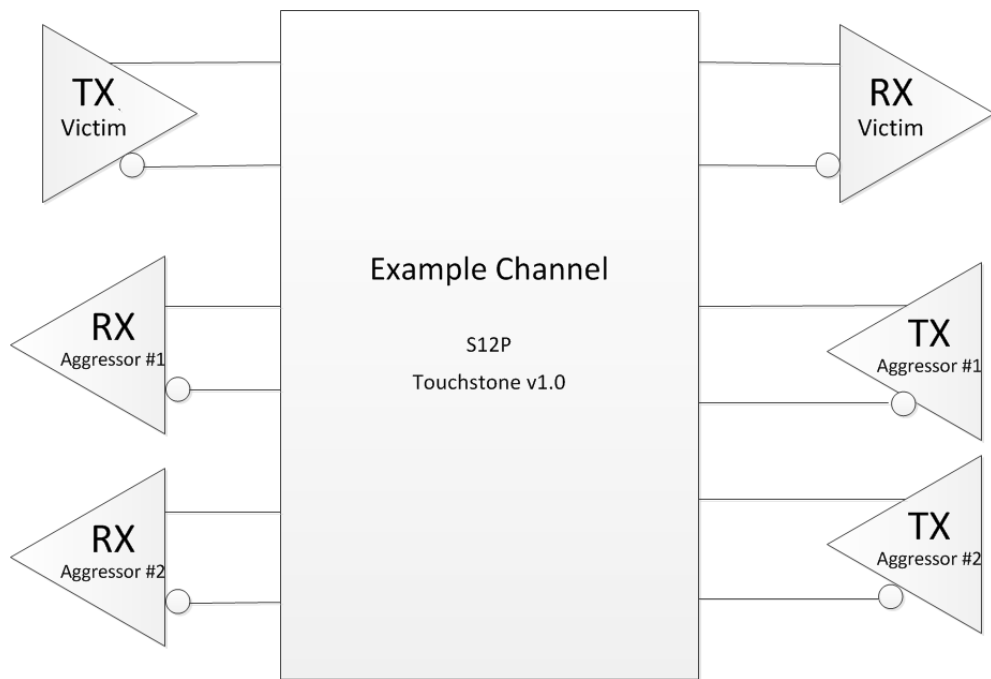
➤ Case 2

- 25 Gbps serial link IBIS-AMI simulation with jitter and noise impairments added to the analysis.

➤ Case 3

- 25 Gbps serial link IBIS-AMI simulation with crosstalk, jitter and noise impairments added to the analysis.

Simulation Case 3



25Gbps Crosstalk Channel Simulation With Jitter and Noise Impairments

Simulation Configuration for Case 3

Simulation Setup		EDA Configuration		AMI Model Specific	
Data Rate: 25Gbps		TX	RX	TX	RX
Data Pattern: PRBS-15		RJ 0.01 UI	RJ 0.01 UI	TXPVT 0	RXPVT 0
Samples Per Bit: 64		DJ 0.04 UI	DJ 0.025 UI	TXDIFFCTRL 31	DFE Auto-Adapt Enabled
AMI Processing Block size: 4,096		DCD 0.02 UI	DCD 0.01 UI	TXPRECURSOR 6	CTLE Auto-Adapt Enabled
Ignore Bits: 250E3			RN 2.5mV	TXPOSTCURSOR 14	AGC Auto-Adapt Enabled
Recording Bits: 1E6		-			

Crosstalk Aggressors

Data Rate:
25Gbps

Pattern:
PRBS-13

TX Phase:
0

TX model specific parameters are the same as those for the victim

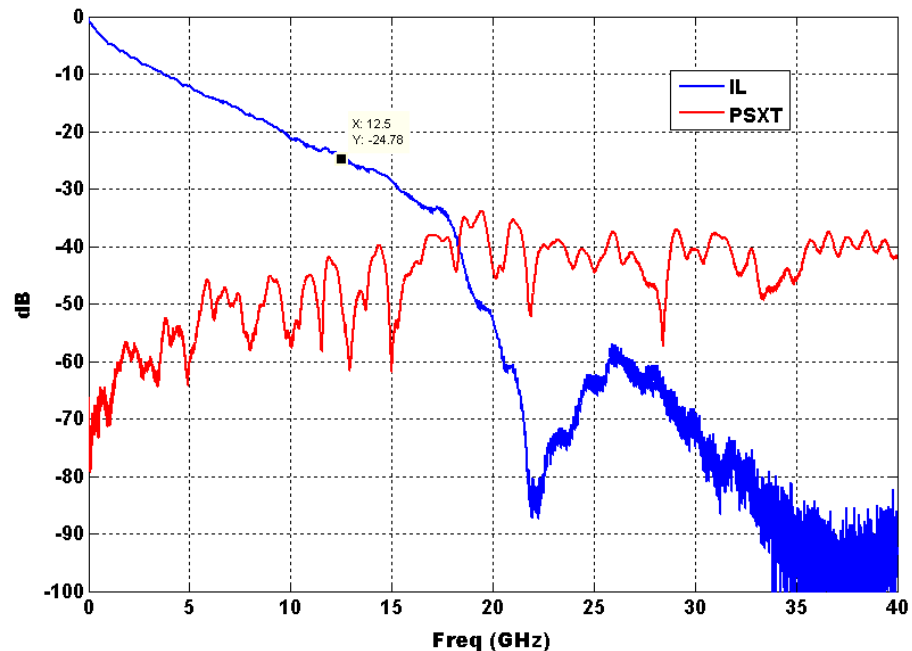
Link Channel Description

➤ Thru Channel

- Data measured with Keysight N5245A.
- S12P Touchstone File v1.0.
- Frequency range: 10MHz to 40GHz.
- Frequency step: ~3.124MHz.

➤ Crosstalk Channels

- Format is same as that for the THRU.
- The ICN from the aggressors is about 1.97mV rms. (The simulation is carried out in time domain.)



Output Eye Diagrams at BER 1e-6

EDA-1

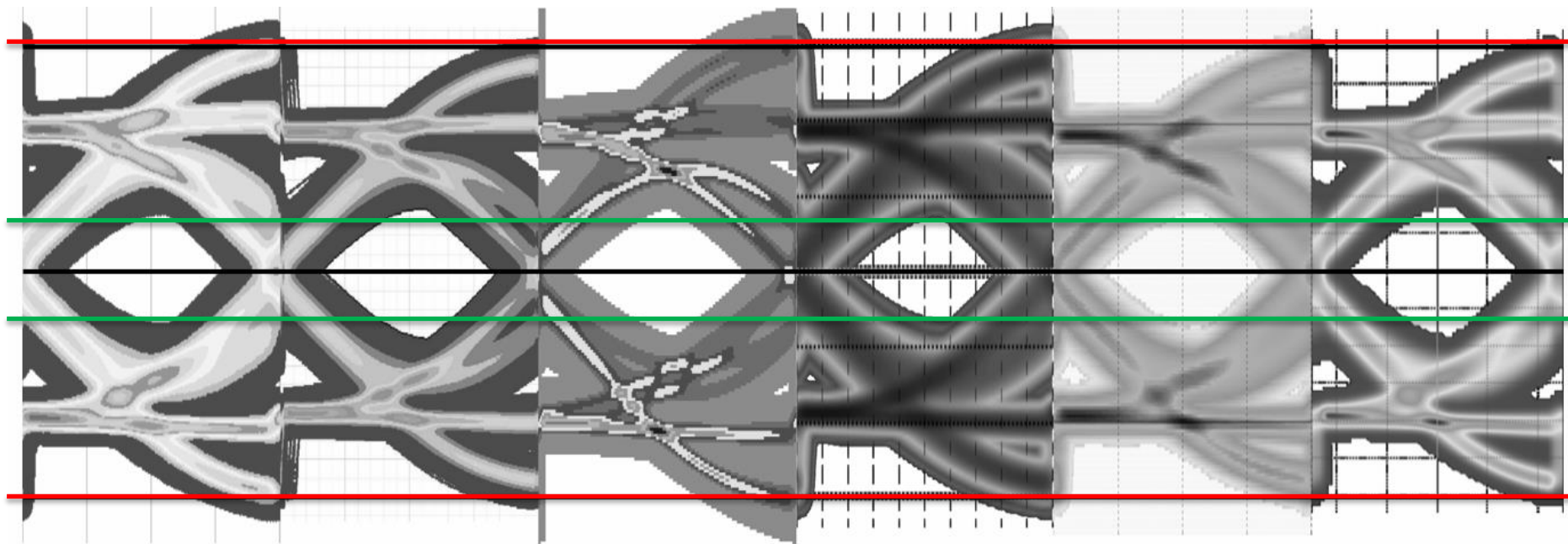
EDA-2

EDA-3

EDA-4

EDA-5

EDA-6

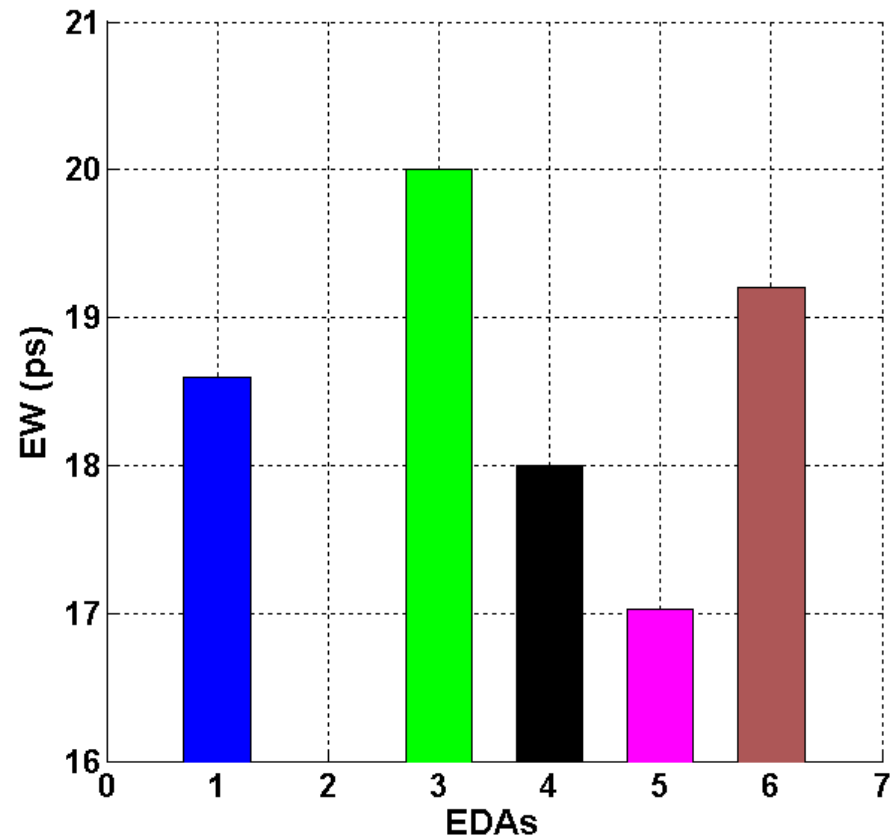
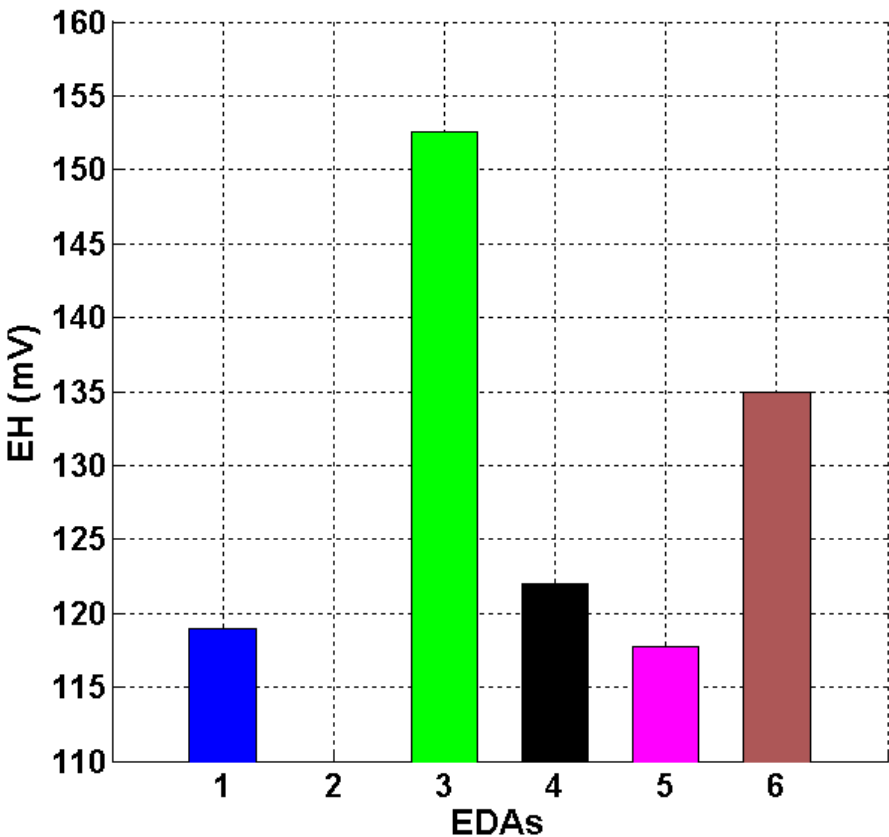


➤ Color mapping scheme could affect eye appearance

Eye Diagram Observations for Case 3

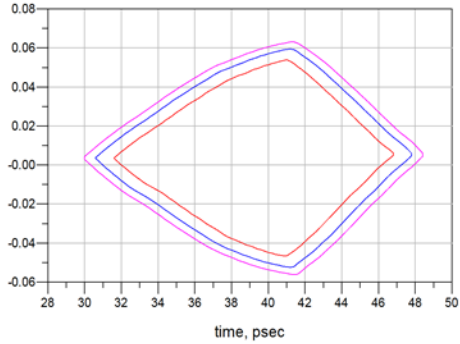
EDAs	EDA-1	EDA-2	EDA-3	EDA-4	EDA-5	EDA-6
Outer Eye	-	Smallest	Largest	-	-	-
Inner Eye	-	-	-	Smallest	-	Largest
Eye Shape	All look similar					
	-	-	The outermost traces bifurcated	-	-	-

Eye Metrics at BER = 1e-12 for Case 3

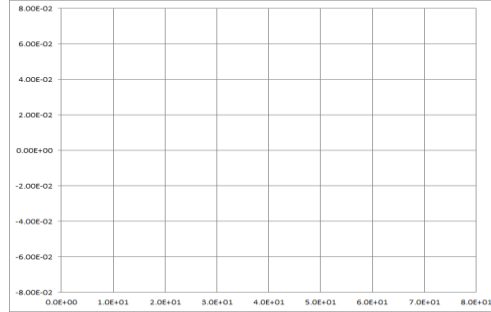


BER Contours for Case 3

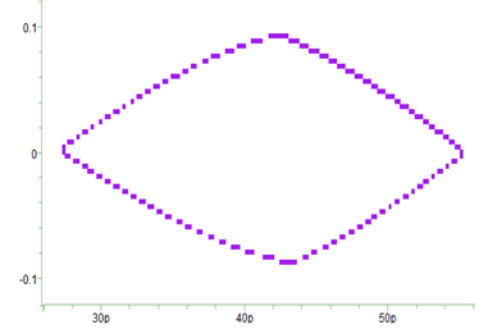
EDA-1



EDA-2

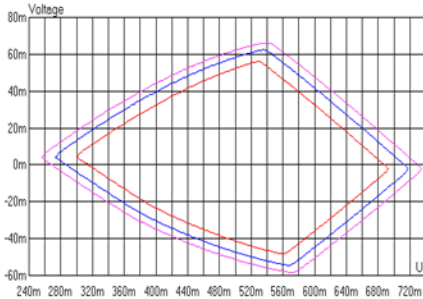


EDA-3 (BER 1e-9)

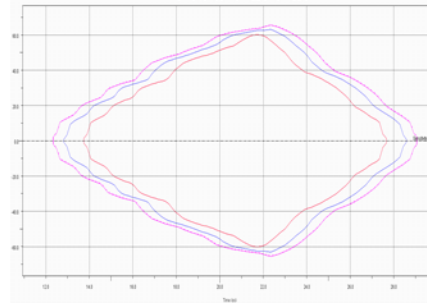


BER Contours (BER 1e-12, 1e-15, 1e-21)

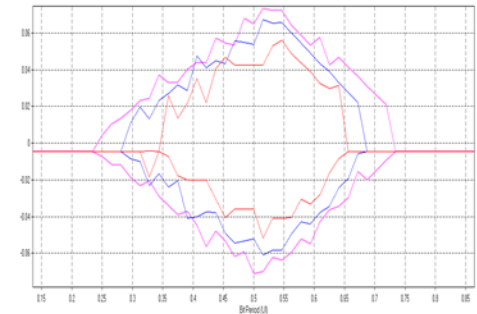
EDA-4



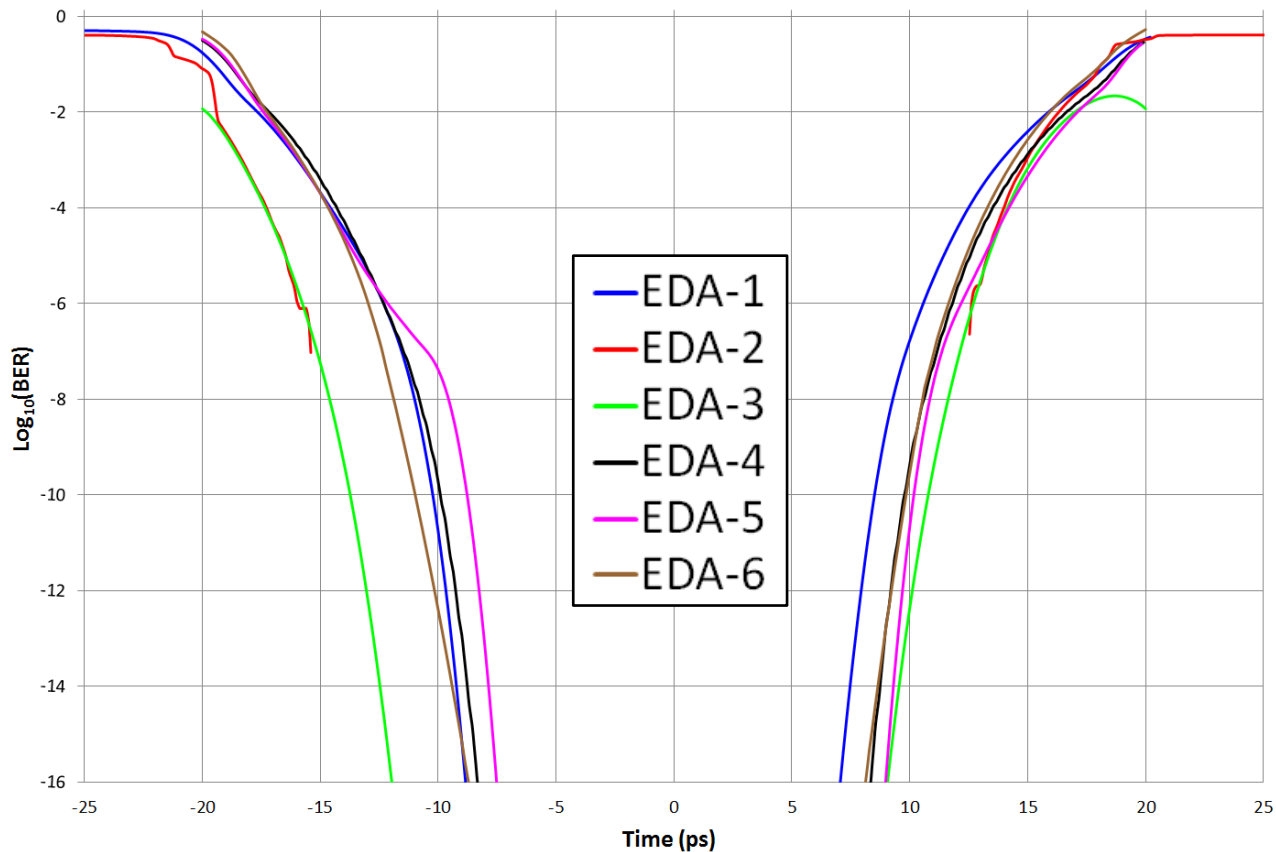
EDA-5



EDA-6



Timing Bathtub Curves for Case 3



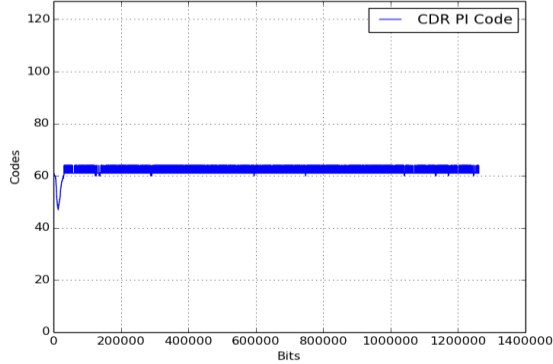
More Observations for Case 3

EDAs	EDA-1	EDA-2	EDA-3	EDA-4	EDA-5	EDA-6
AGC	25	24	25	24	24	24
CTLE	17 – 23	18 – 22	17 – 20	17 – 22	18 – 22	17 – 22
VP (h0)	~100	~100	~99	~100	~100	~100
UT (h1)	~48	~42	~54	~43	~41	~41
h2	~15	~13	~16	~15	~14	~15
h3	~40	~40	~42	~40	~40	~40
CDR	~62	~62	~38	~62	~61	~77
EH @ 1e-12	–	–	Largest	–	Smallest	–
EW @ 1e-12	–	–	Largest	–	Smallest	–

CDR Adaptations for Case 3

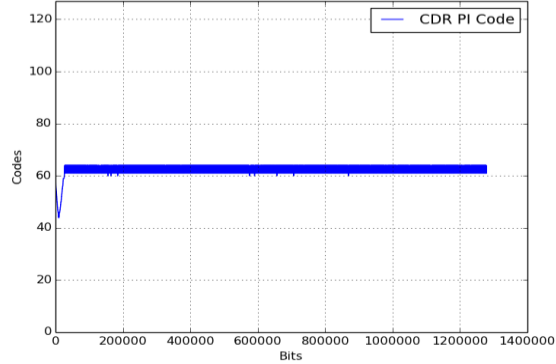
EDA-1

CDR PI Adaptation Output



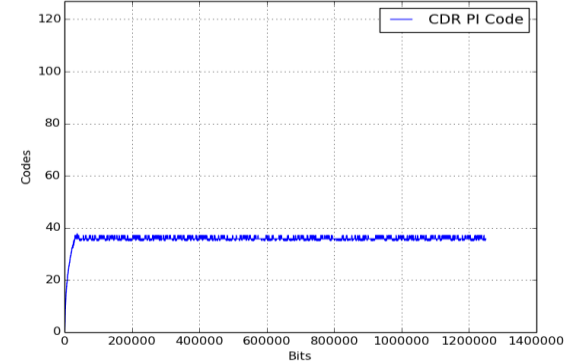
EDA-2

CDR PI Adaptation Output



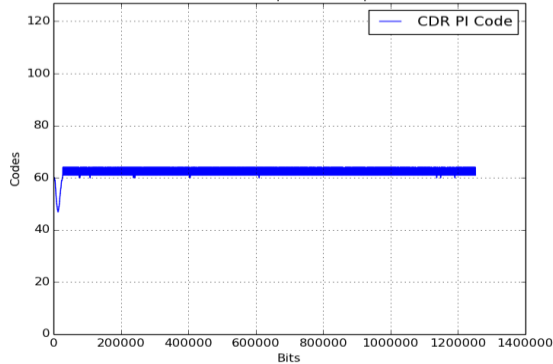
EDA-3

CDR PI Adaptation Output



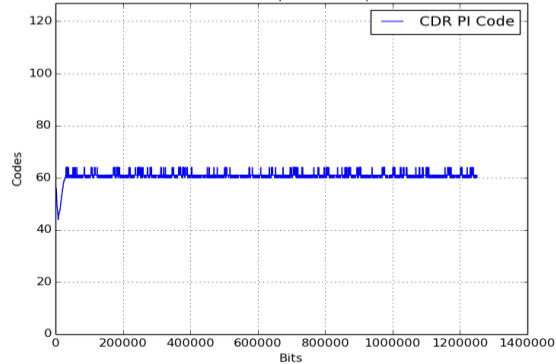
EDA-4

CDR PI Adaptation Output



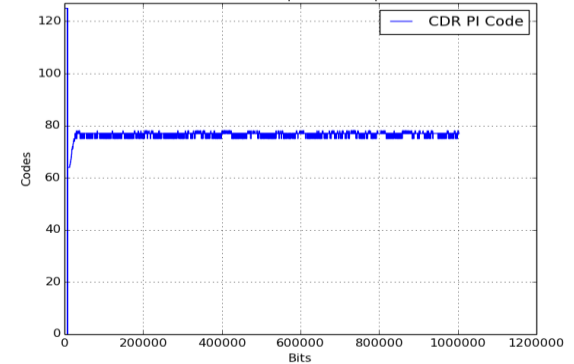
EDA-5

CDR PI Adaptation Output



EDA-6

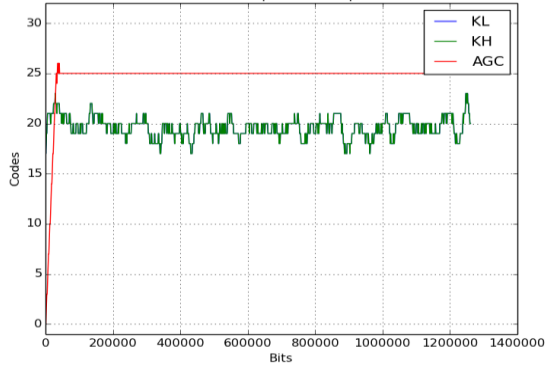
CDR PI Adaptation Output



CTLE & AGC Adaptation for Case 3

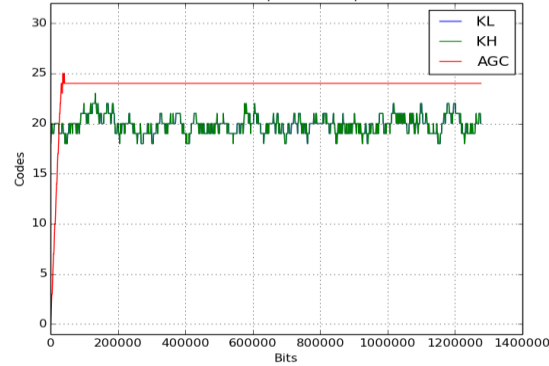
EDA-1

CTLE Adaptation Output



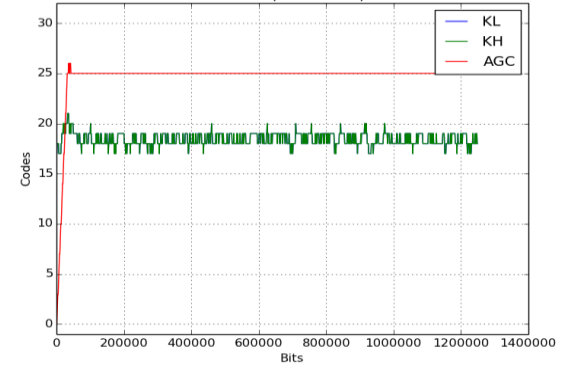
EDA-2

CTLE Adaptation Output



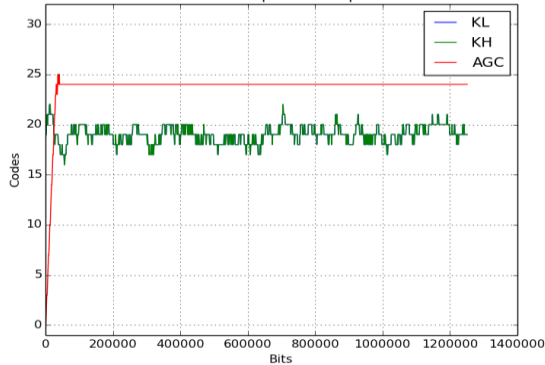
EDA-3

CTLE Adaptation Output



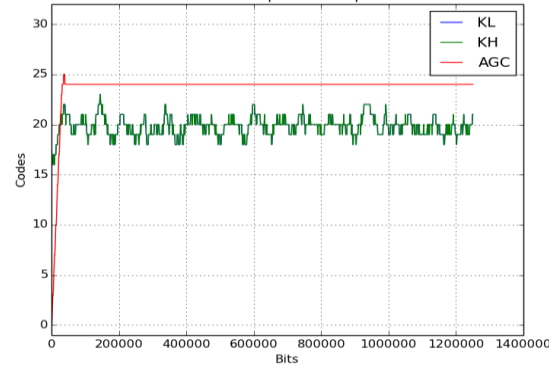
EDA-4

CTLE Adaptation Output



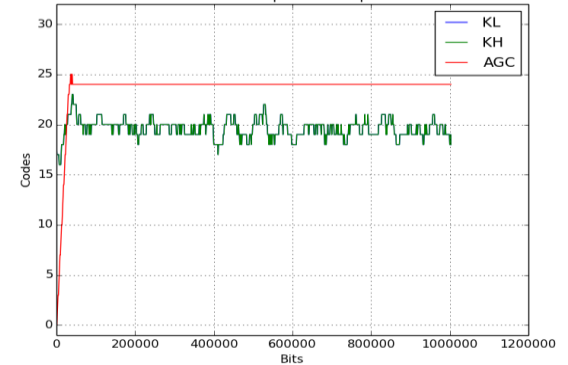
EDA-5

CTLE Adaptation Output



EDA-6

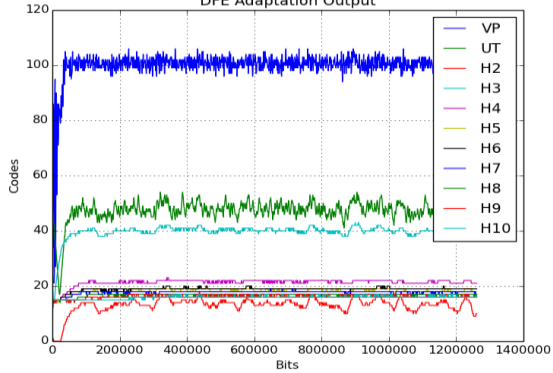
CTLE Adaptation Output



DFE Adaptations for Case 3

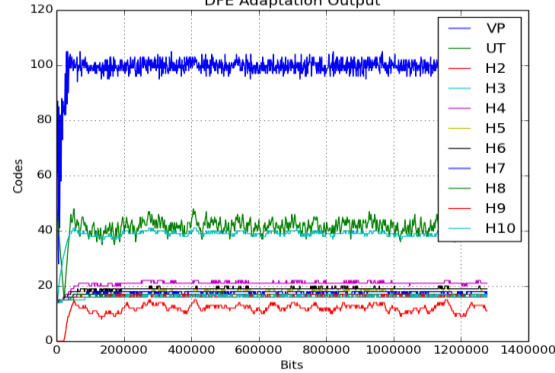
EDA-1

DFE Adaptation Output



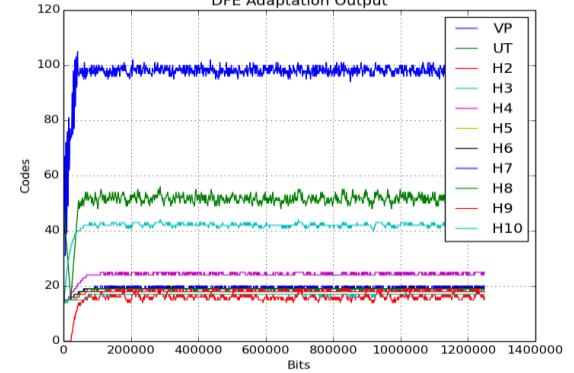
EDA-2

DFE Adaptation Output



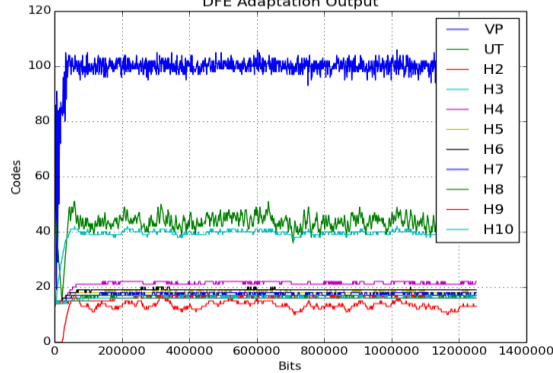
EDA-3

DFE Adaptation Output



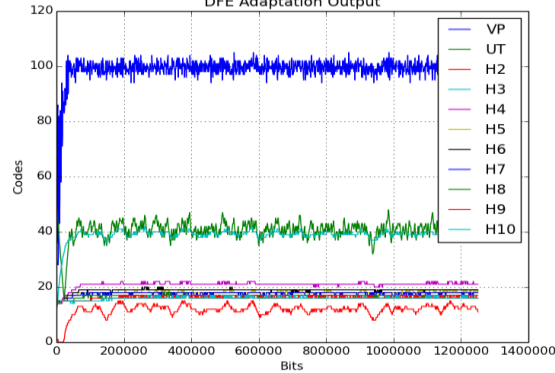
EDA-4

DFE Adaptation Output



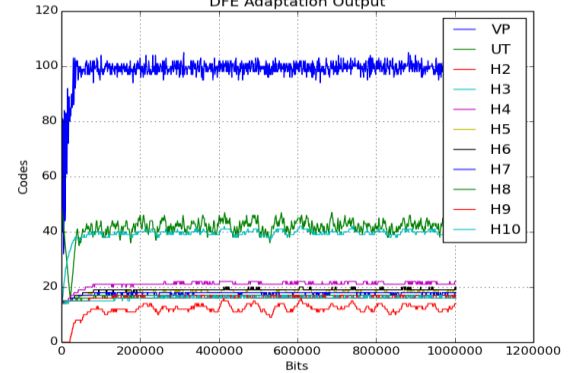
EDA-5

DFE Adaptation Output



EDA-6

DFE Adaptation Output



Discussion on Case 3 Simulation Results

➤ CDR adaptations

- CDR behaviors are matching Case 1, which is the expected behavior.

➤ CTLE adaptations

- All six EDAs generated approximately CTLE=20 (same as those in both Case 1 and Case 2).

➤ AGC adaptations

- Except for EDA-3, AGC adaptations match Case 1, the expected behavior.
- EDA-3 AGC slightly reduced from 26 to 25, compared with that in Case 1, and matching that in Case 2.
- EDA-2 AGC now matched that in Case 1, still making Case 2 an outlier.

Discussion on Case 3 Simulation Results (Con't)

➤ DFE tap adaptations

- Except for EDA-3, DFE adaptations match Case 1 only with increased variations, which is the expected behavior.
- EDA-3 results match Case 2.

➤ Eye metrics (EH and EW at BER=1e-12)

- We could not generate the data in EDA-2 for this measurement.
- EDA-3 stood out; it generated the largest EH, and the largest EW.
- EDA-3, somehow, showed increased EH and EW, compared with Case 2.

➤ Bathtub curves

- The six EDAs generated very different bathtub curves, including curve slopes.
- We could not extrapolate beyond 1e-6 in EDA-2, thus data it is left blank.
- The conclusion for system margin could be different using different EDA tools.

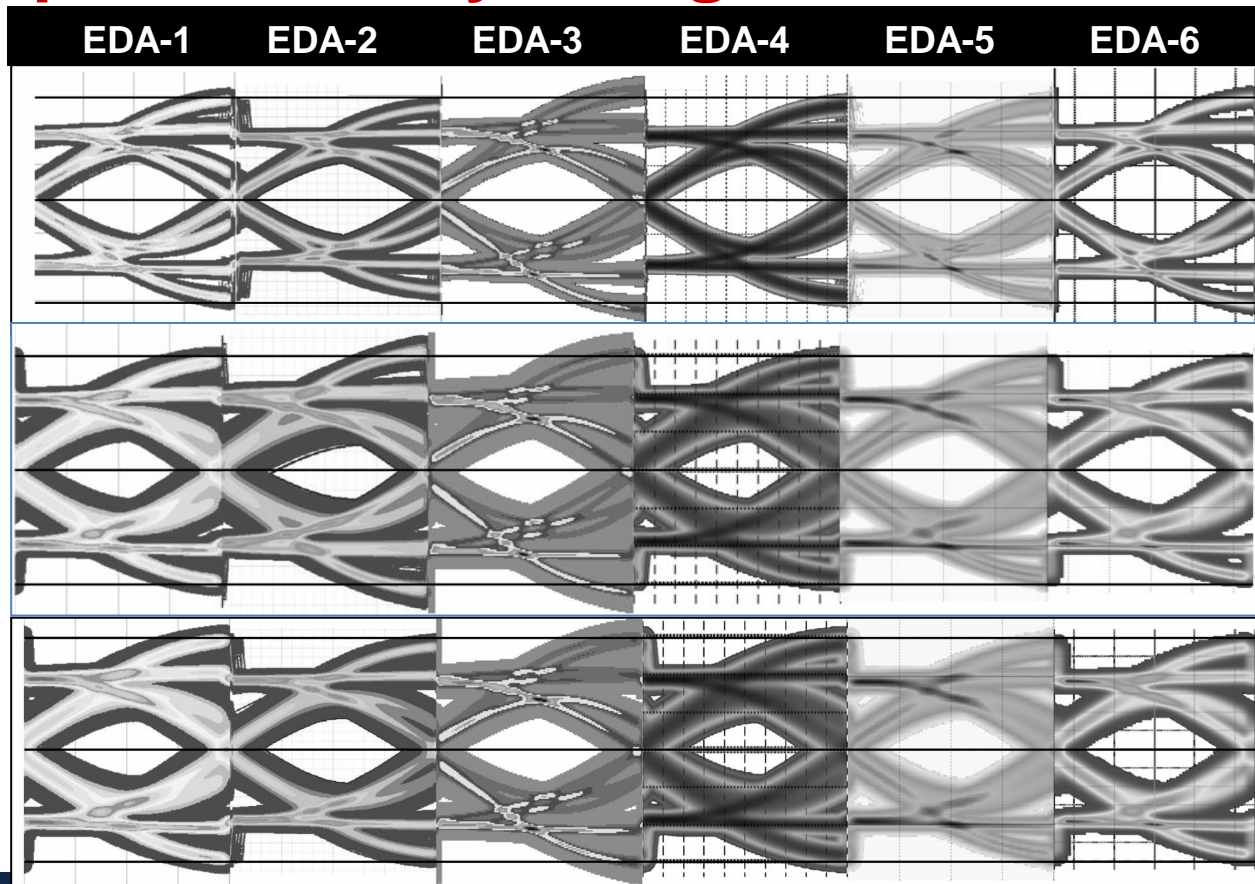
Selected Comparison of Simulation Results

Comparison of Eye Diagrams

➤ **Case 1: No added jitter or noise**

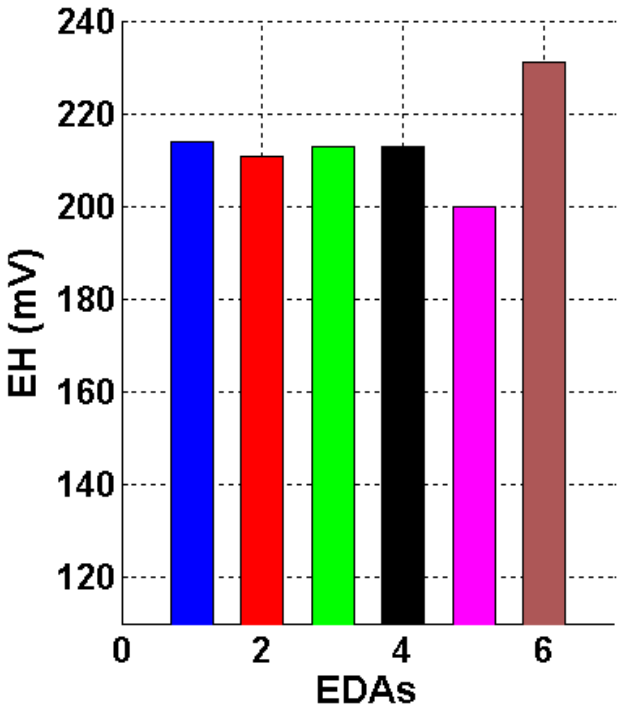
➤ **Case 2: With added jitter and noise**

➤ **Case 3: With added jitter and noise, plus crosstalk**

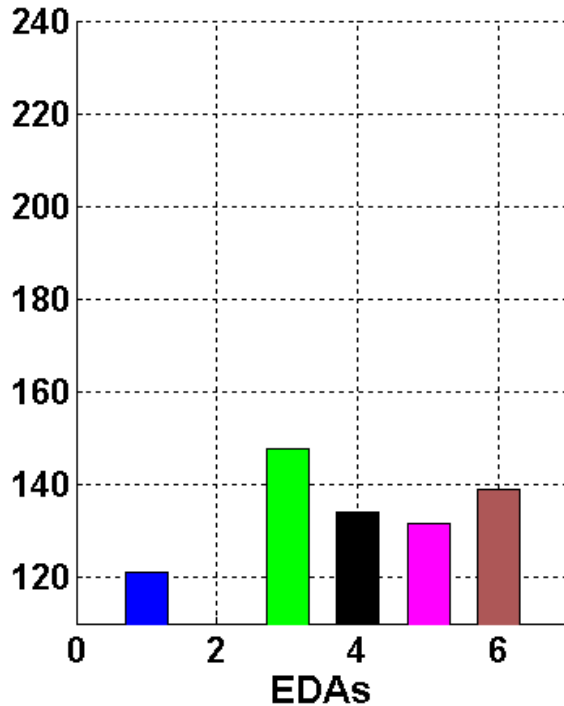


Comparison of Eye Height (mV) at 1e-12

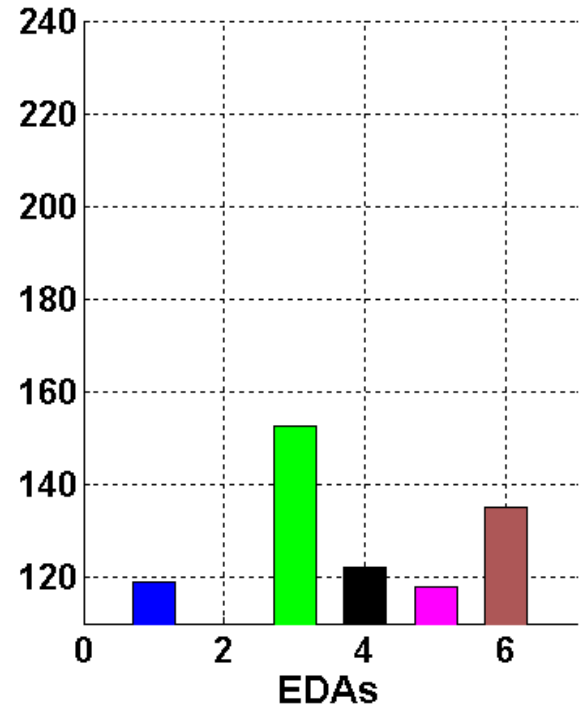
➤ With no added jitter or noise



➤ With added jitter and noise



➤ With added jitter, noise, and Xtalk

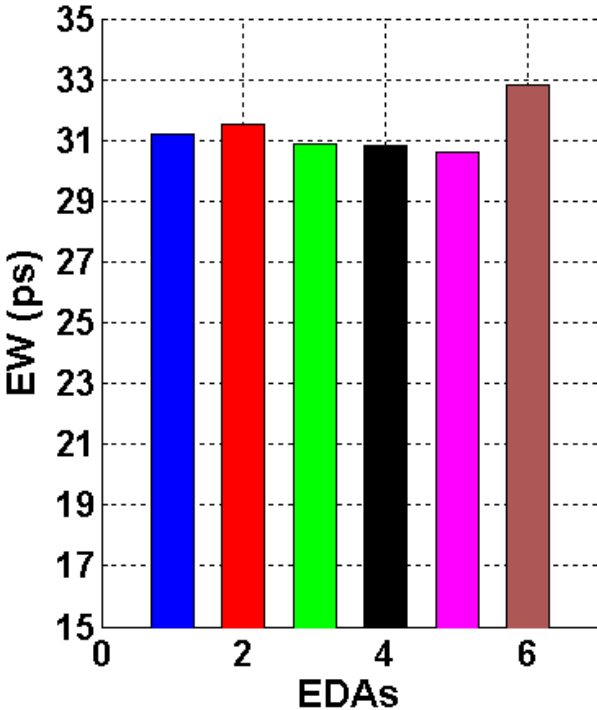


Eye Height Change Between Cases

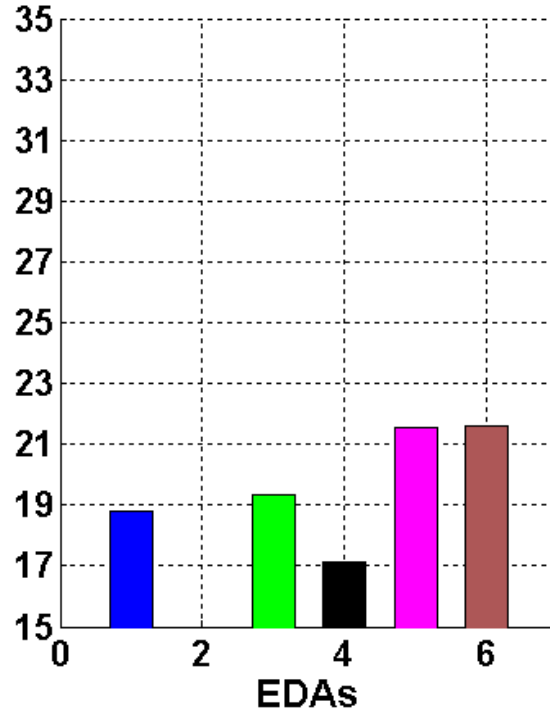
Eye Height Reduction (%)	From Case 1 to Case 2	From Case 2 to Case 3	From Case 1 to Case 3
EDA-1	43.5	1.7	44.4
EDA-2	-	-	-
EDA-3	30.6	-3.2	28.4
EDA-4	37.1	9.0	42.7
EDA-5	34.2	10.4	41.1
EDA-6	39.8	2.9	41.6

Comparison of Eye Width (ps) at 1e-12

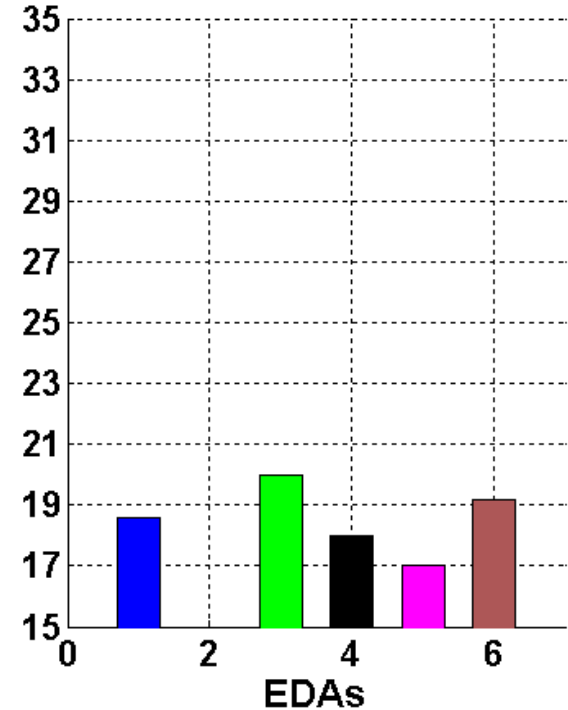
➤ With no added jitter or noise



➤ With added jitter and noise



➤ With added jitter, noise, and Xtalk

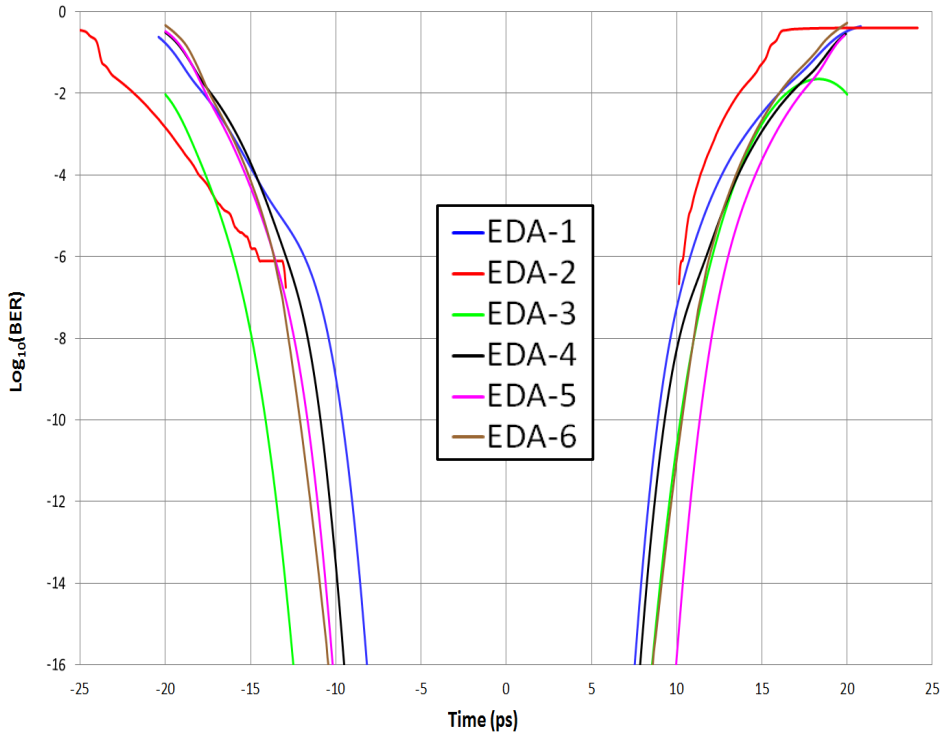


Eye Width Change Between Cases

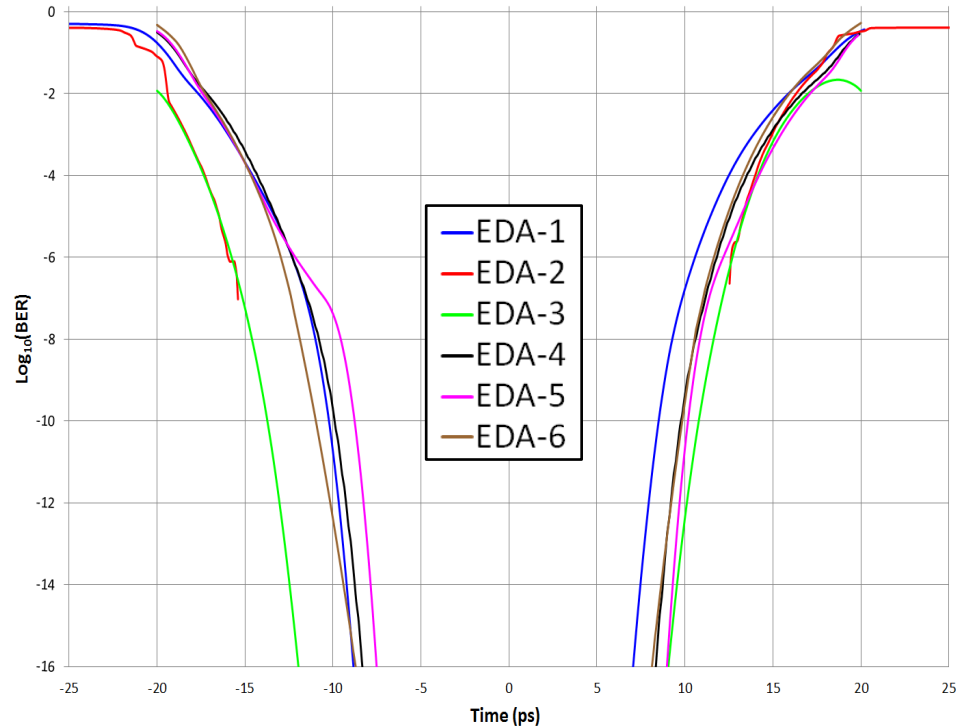
Eye Width Reduction (%)	From Case 1 to Case 2	From Case 2 to Case 3	From Case 1 to Case 3
EDA-1	39.7	1.1	40.4
EDA-2	-	-	-
EDA-3	37.4	-3.4	35.3
EDA-4	44.4	-5.0	41.6
EDA-5	29.5	21.0	44.3
EDA-6	34.1	11.1	41.5

Comparison of Timing Bathtub Curves

Without Crosstalk (Case 2)

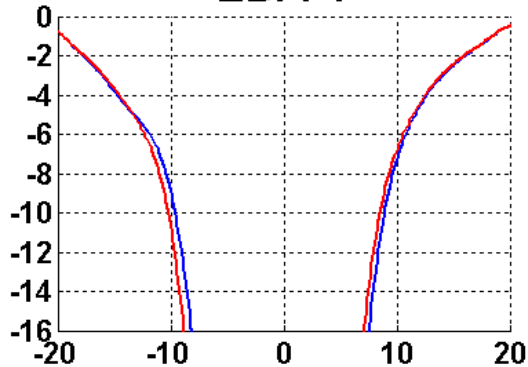


With Crosstalk (Case 3)

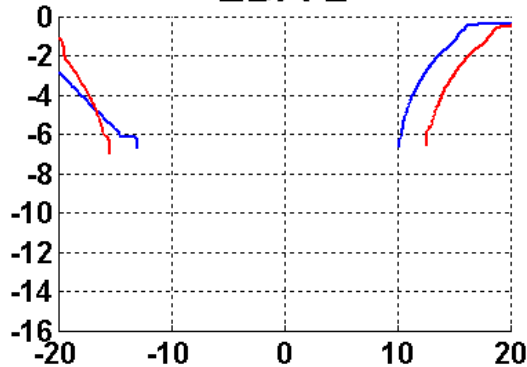


Bathtub Curves w/o (blue) & w/ (red) Crosstalk

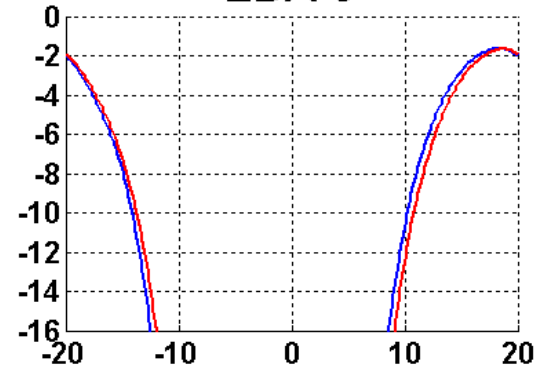
EDA-1



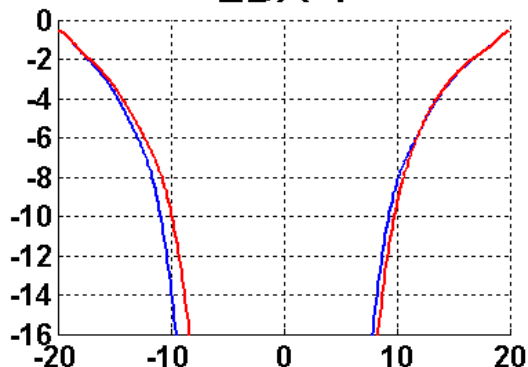
EDA-2



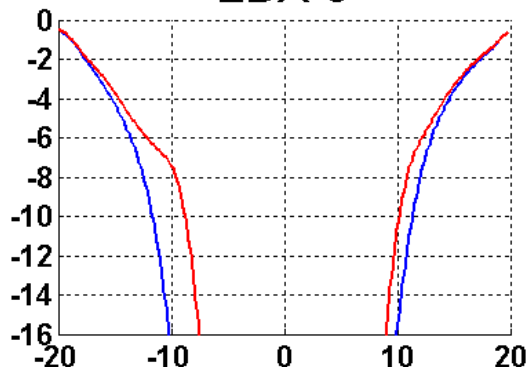
EDA-3



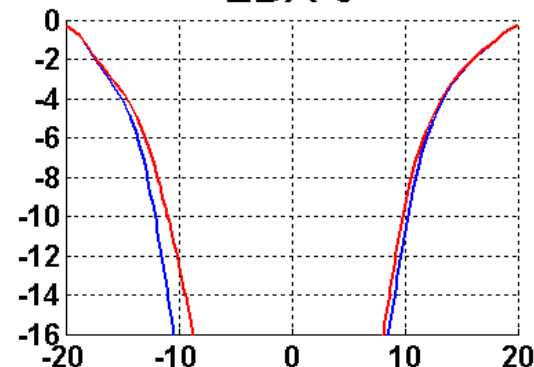
EDA-4



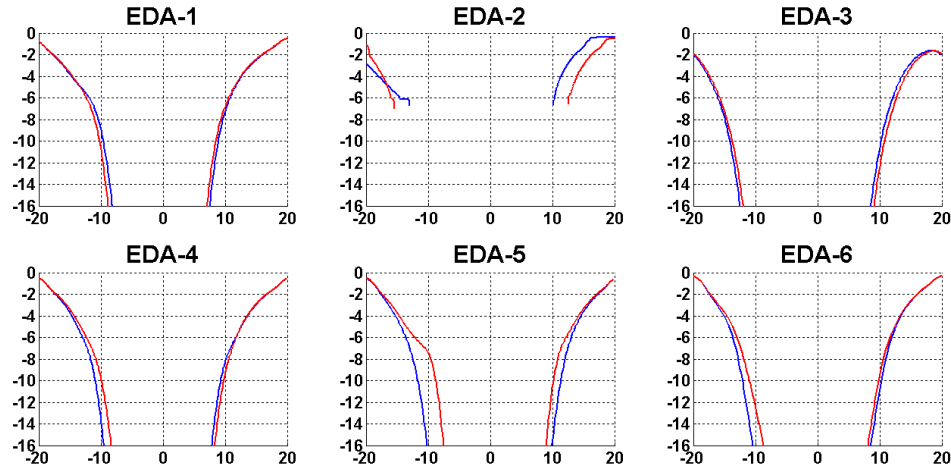
EDA-5



EDA-6

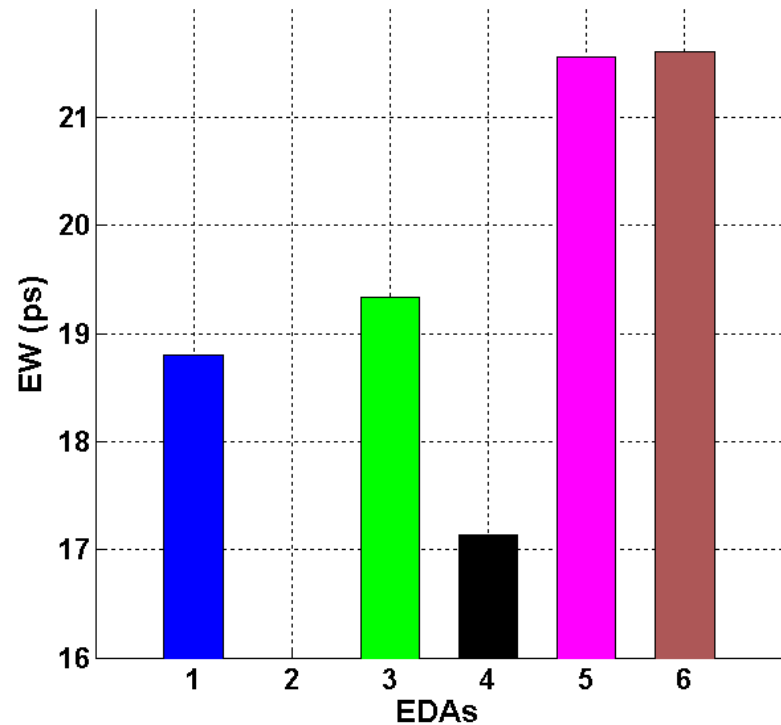
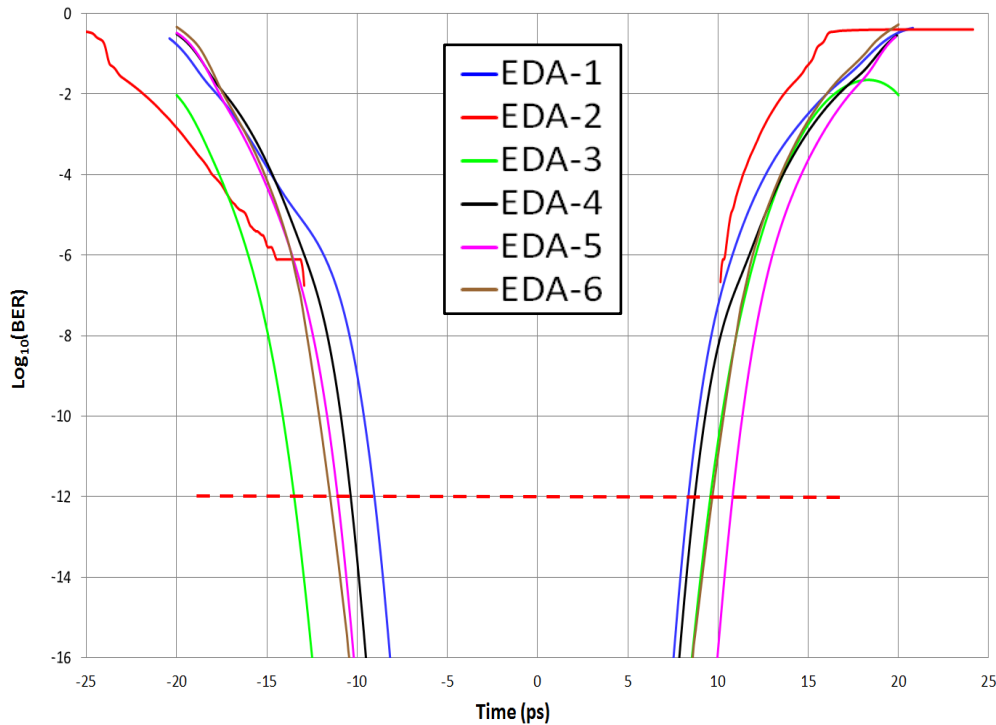


Bathtub Curves w/o (blue) & w/ (red) Crosstalk



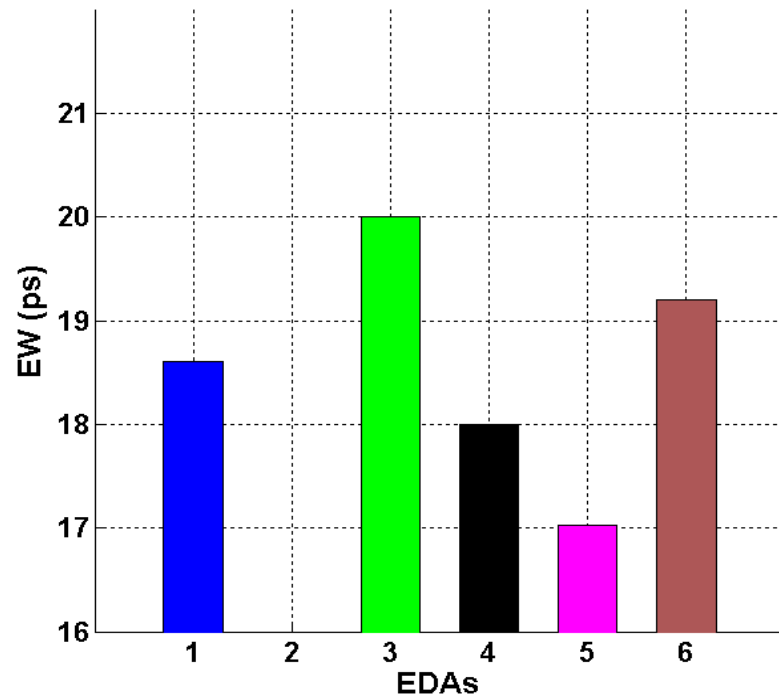
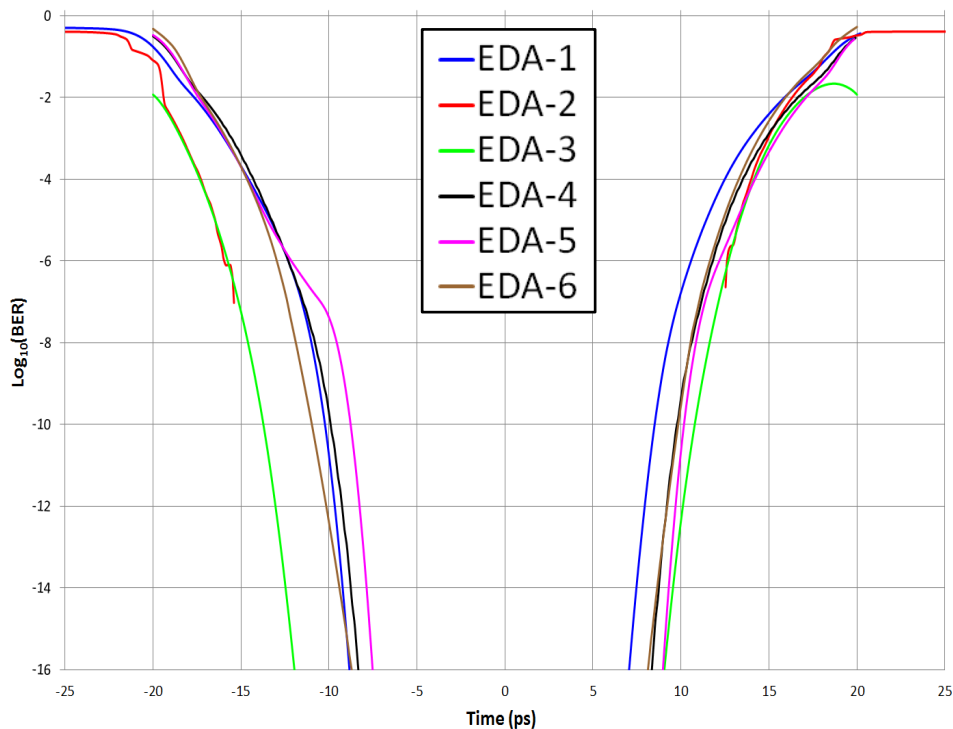
- Only EDA-5 and EDA-6 showed consistent degradation for both sides.
- EDA-2 showed larger EW, for both left and right side, even at BER = 1e-6.
- EDA-3 and EDA-4 showed a shift of the sides to the right.
- EDA-1 showed a shift of bathtub curve to the left side.

Eye Width Vs. Timing Bathtub for Case 2



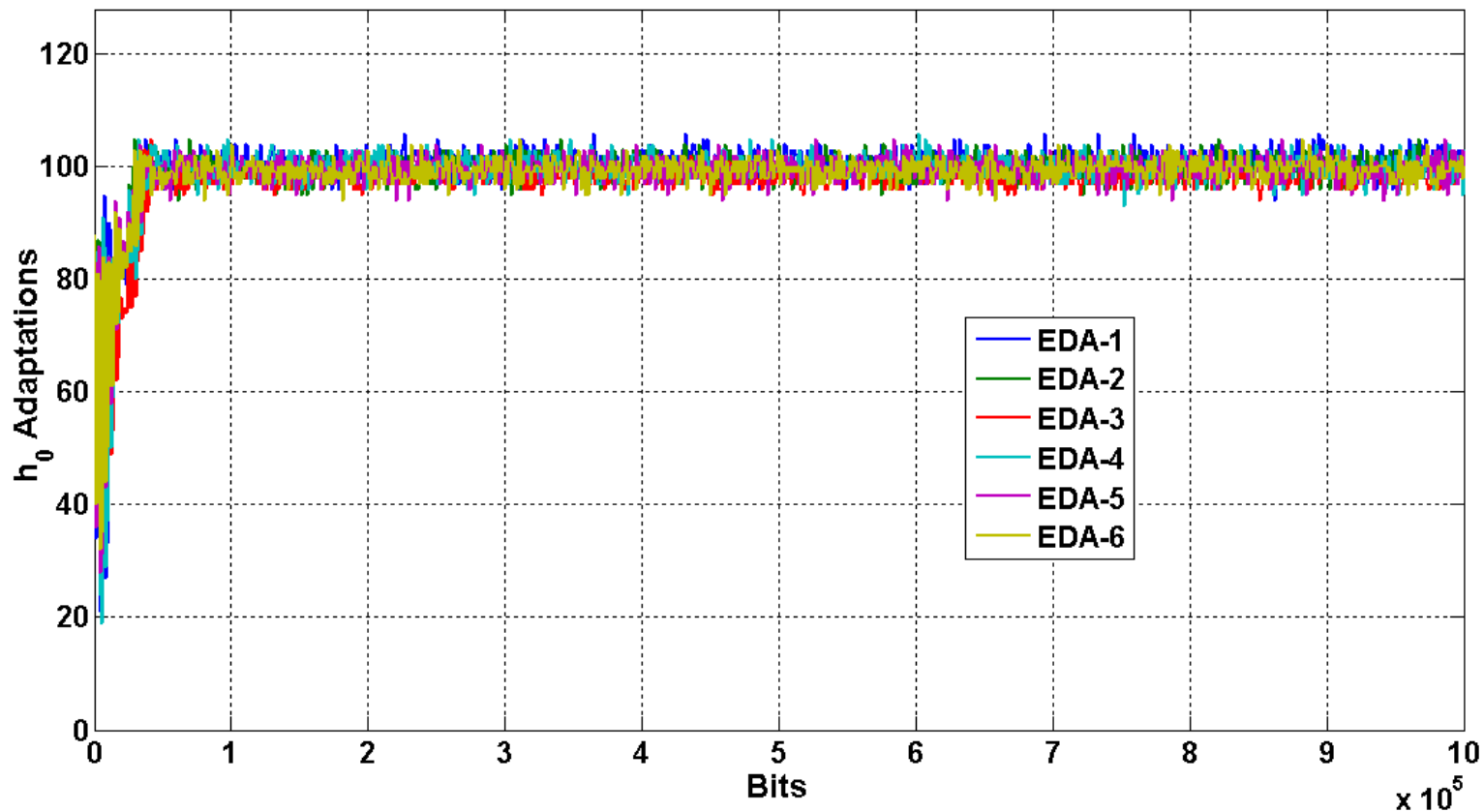
➤ The bar chart of eye width is derived from the timing bathtub curves.

Eye Width Vs. Timing Bathtub for Case 3

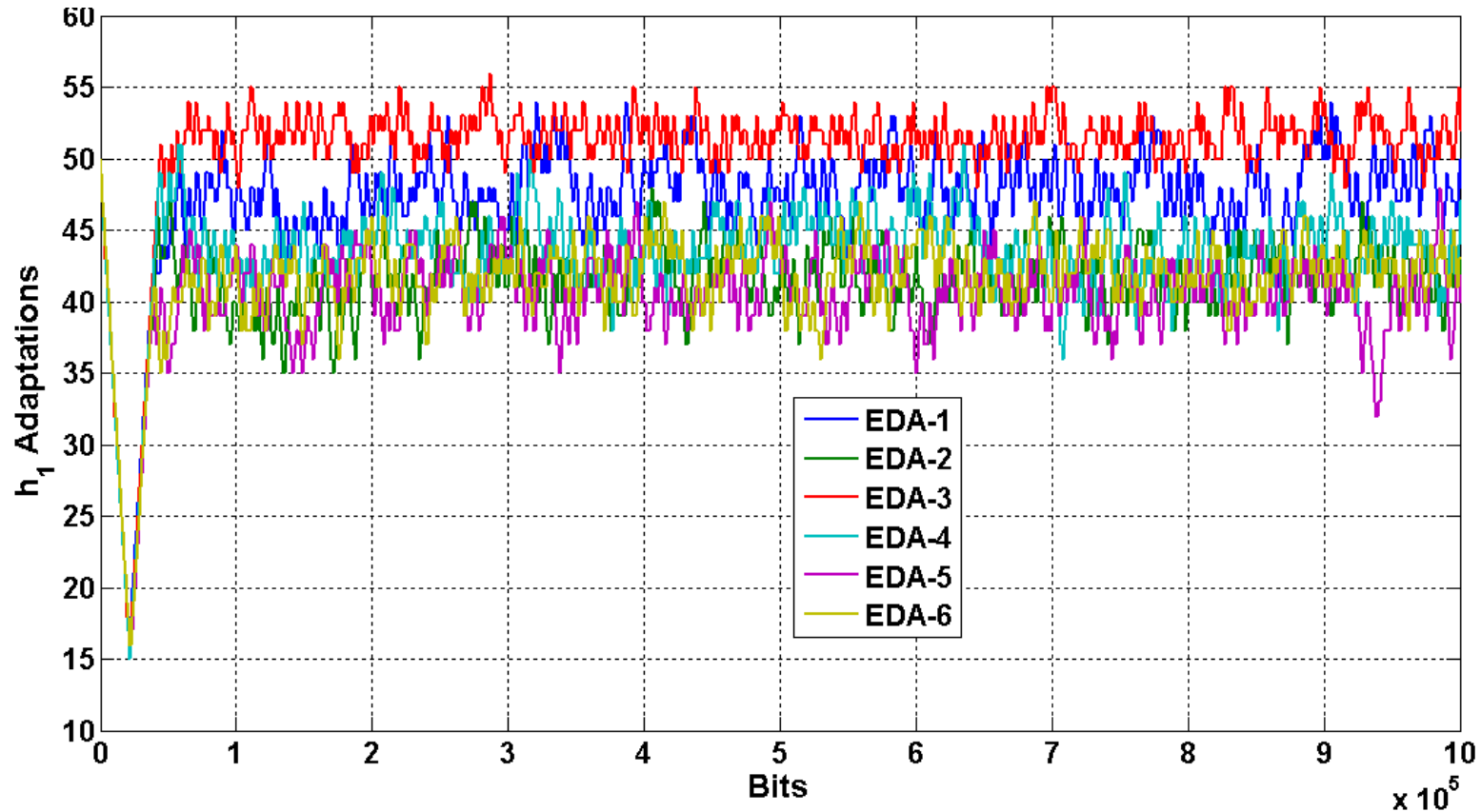


➤ The bar chart of eye width is derived from the timing bathtub curves.

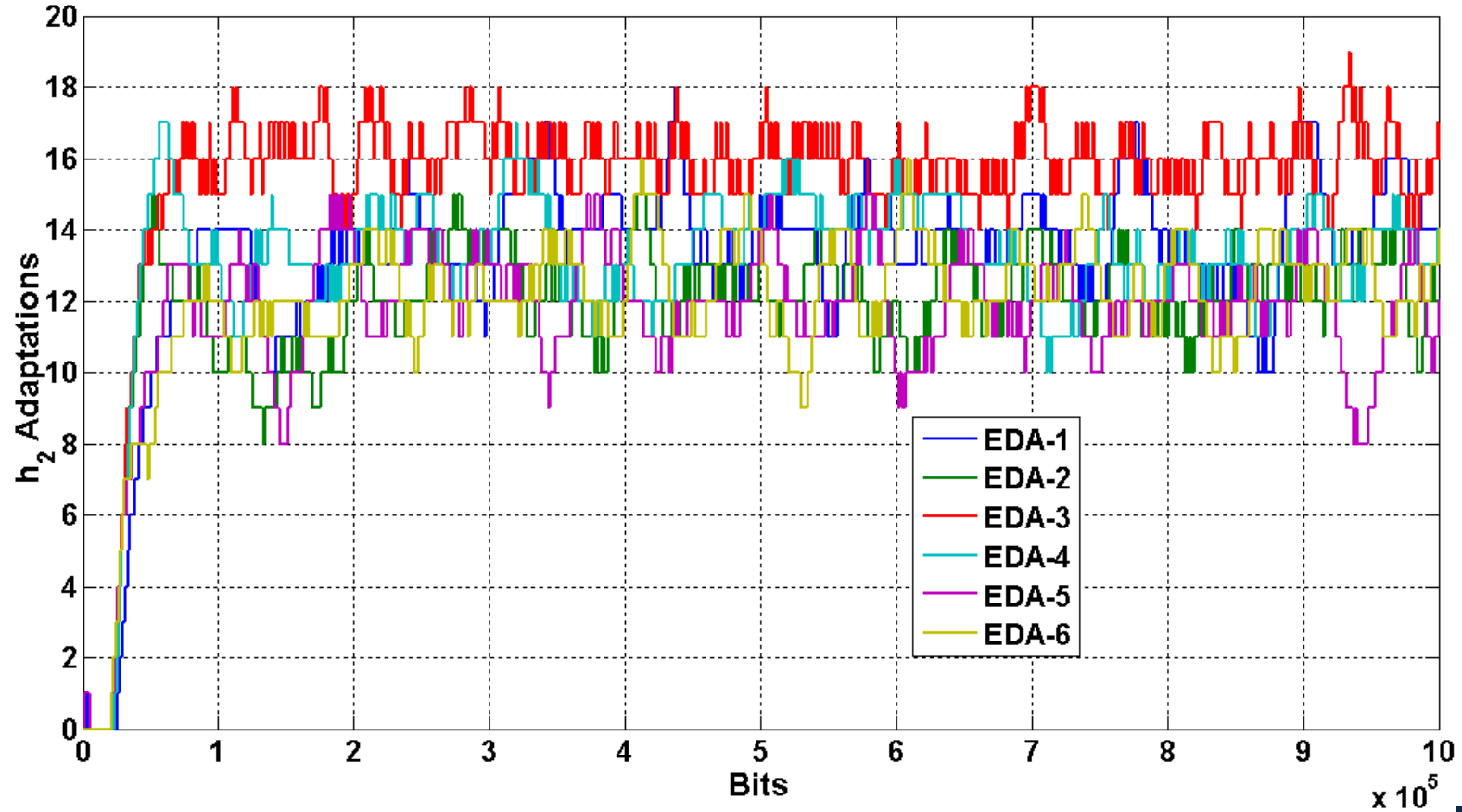
VP (h0) Adaptations for Case 3



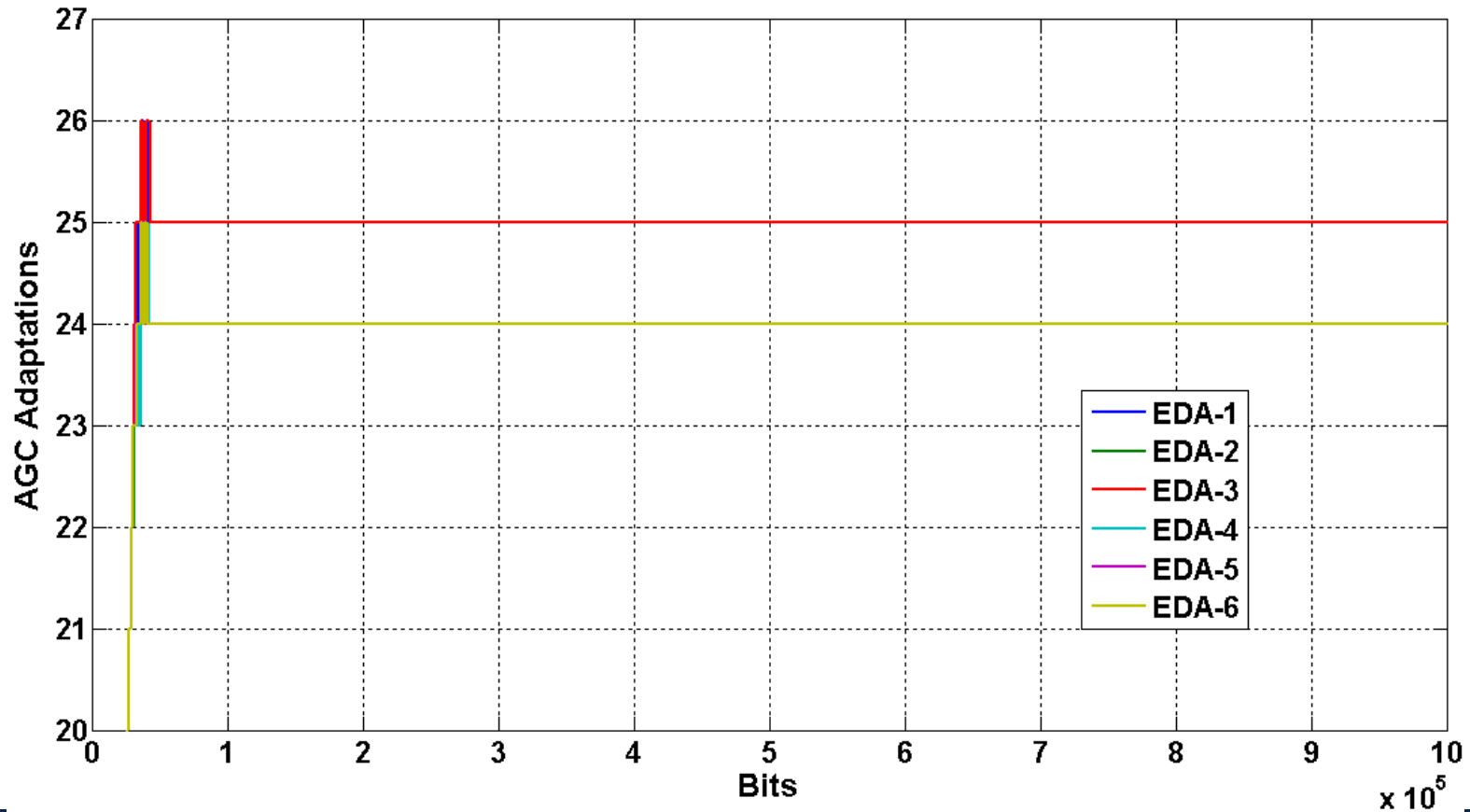
DFE UT (h1) Adaptations for Case 3



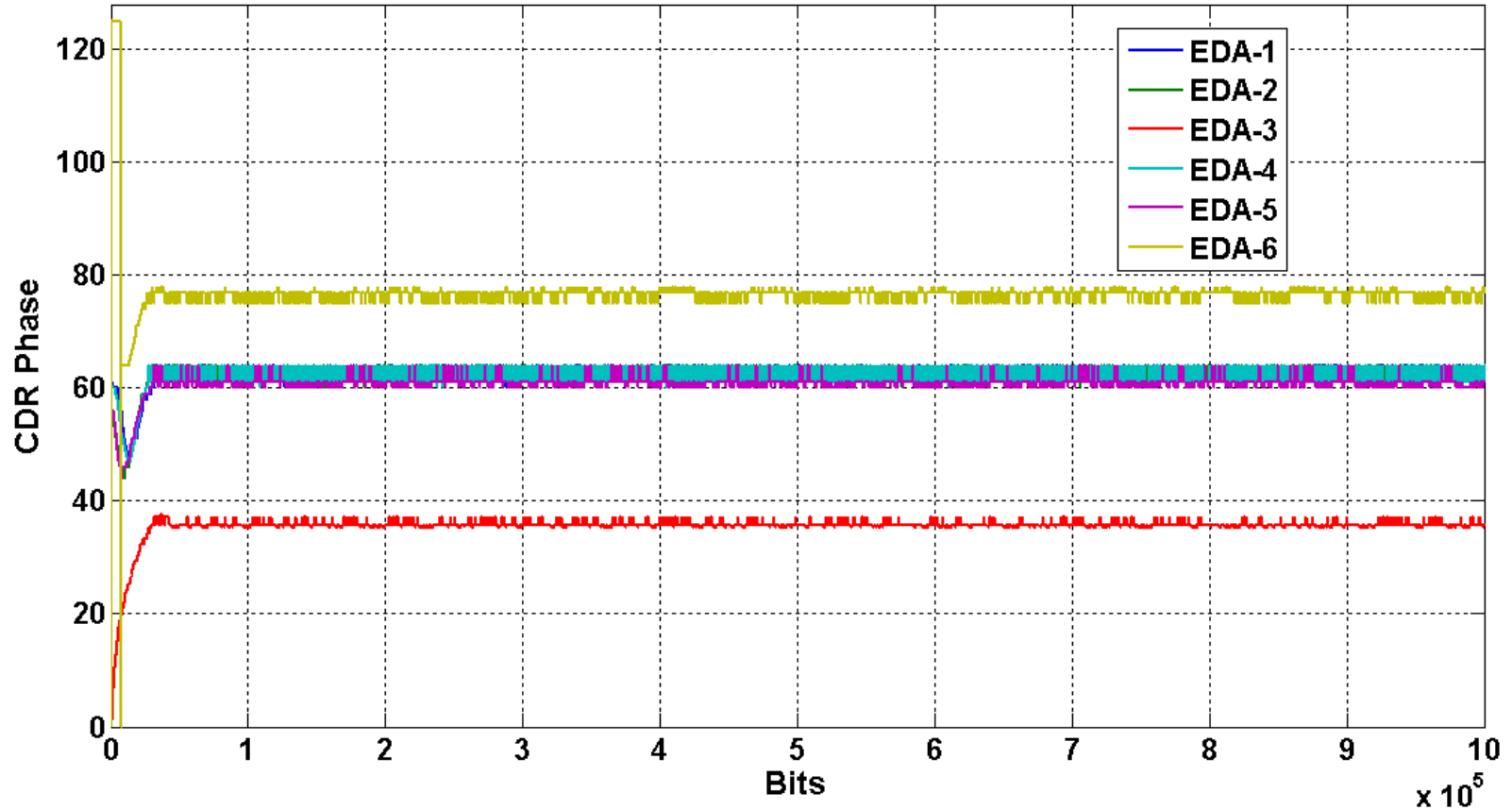
DFE h2 Adaptations for Case 3



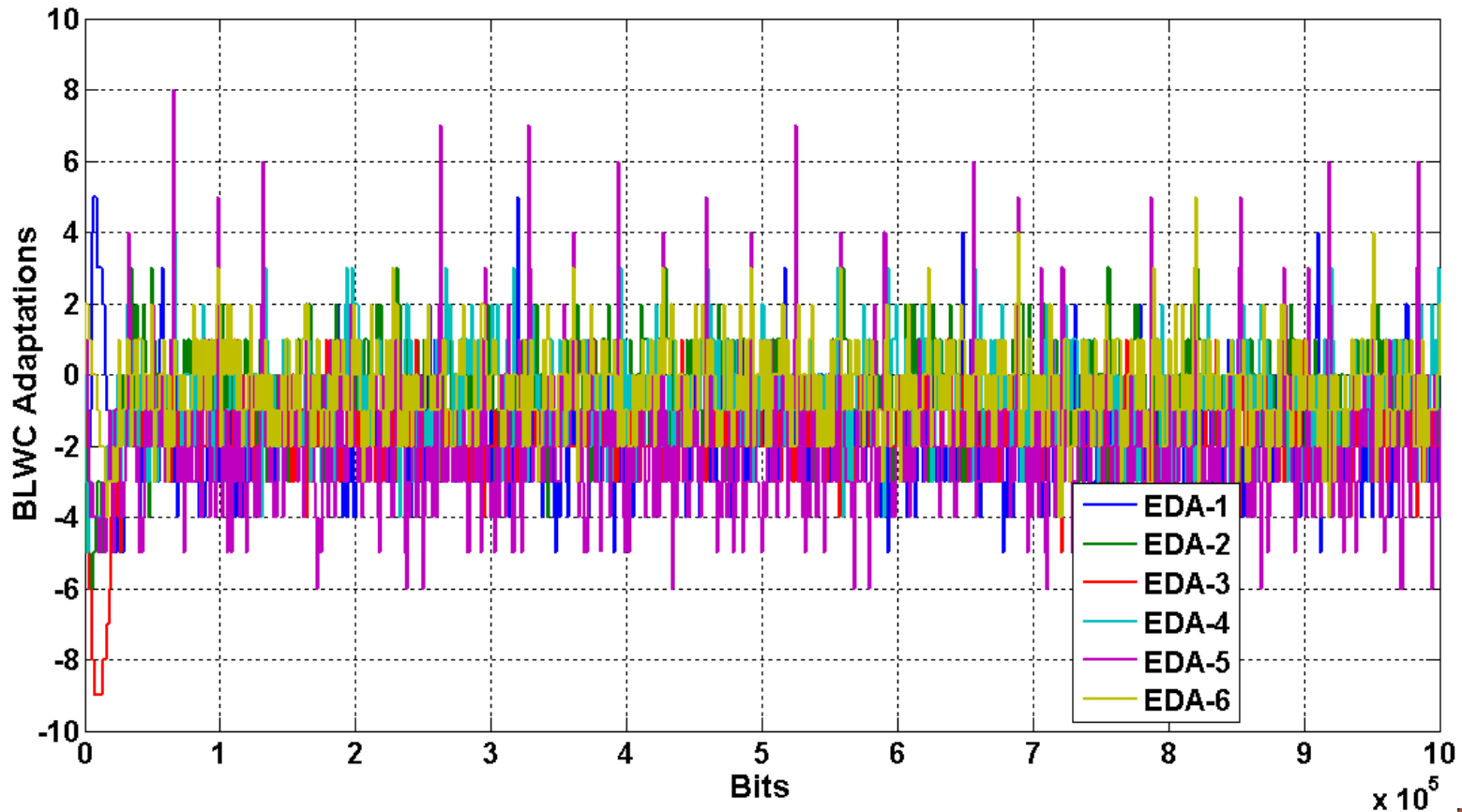
AGC Adaptations for Case 3



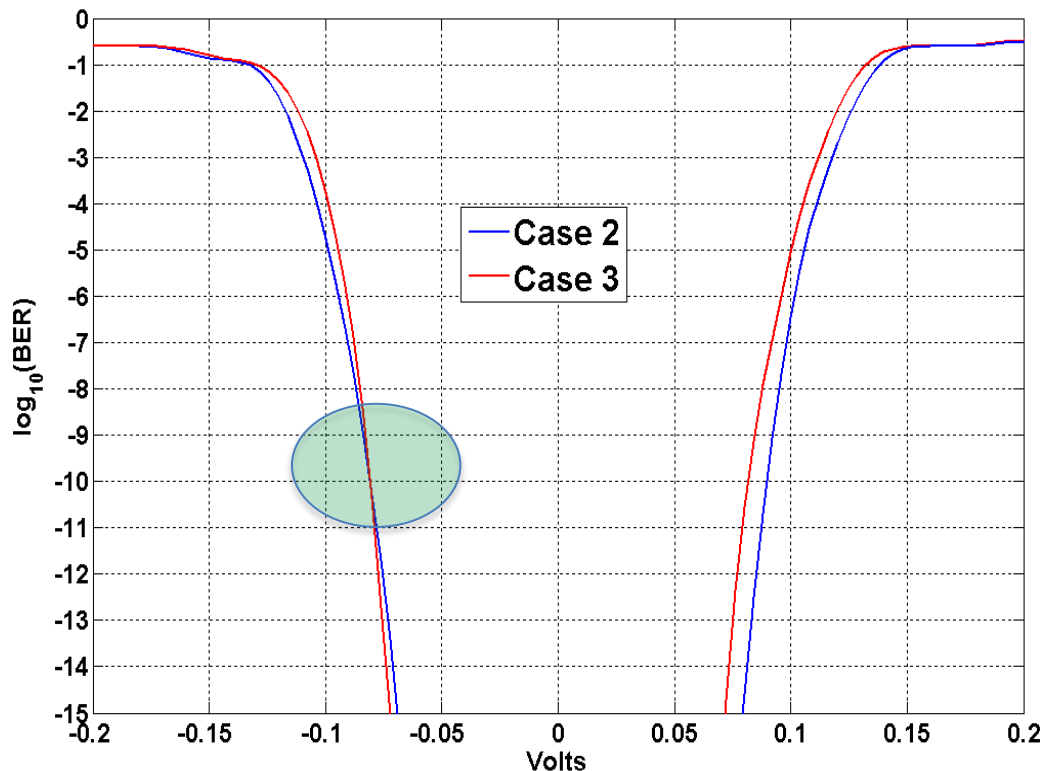
CDR Adaptations for Case 3



Baseline Wander Correction for Case 3



Comparing Eye Height from Bathtub Curve for EDA-3 between Case 2 and Case 3



- Case 2 and Case 3 crosses over at $\sim \text{BER} = 1\text{e-}10$.
- Since EH is determined by the smaller side of the branch, the left branch dominates in this example.
- The left branch showed less slope when crosstalk is added (Case 3) than in Case 2, which is not expected.

Summary of the Work

Summary

- Six EDAs are used to perform link simulations, based on Xilinx UltraScale GTY IBIS-AMI model (V2.1), of three setup conditions: (1) the THRU channel only without added noise or jitter, (2) with added noise and jitter, and (3) plus crosstalk interference, all at 25Gbps with a ~25dB loss backplane channel, whose model was provided by a Xilinx key customer.
- During the process of working on the above simulations, we have engaged proactively with all the six involved EDAs, trying to make sure our operations are intended and our setups are correct.
- However, we cannot guarantee that our presented results and our understanding of tool configurations always reflect the EDA intentions. In fact, a couple EDAs made quite a few changes during the work. The result in this presentation represent the latest information available to us.

Summary (Con't 1)

- In general, the differences in tools' capabilities and in certain results are quite large, larger than we initially anticipated. Xilinx is happy to work with any EDAs to investigate any unexpected results.
- Xilinx is also willing to assist any EDAs to find the cause of any discrepancies, be that the impulse response, the adaptation convergences, available EDA output parameters, or post-processing results.
- For the discrepancies that were observed, first, some EDAs have different IPR results, which surely affect link performance judgments:
 - Although the impact might not be visible from eye diagrams or bathtub curves, it can be revealed from converged parameter adaptation results.
 - EDA-6 delay in IPR translates into delay in CDR sampling phase.
 - EDA-3 has a different IPR profile but its impact on CDR adaptation is unexpected.

Summary (Con't 2)

- Although using identical SerDes TX and RX IBIS-AMI models, as well as the same channel s-parameter file(s), we have not seen any two EDAs generated the same data for any of the three simulated cases.
 - For example, for DFE h1 tap, the differences could be 16 codes among the six EDA results; for AGC, the difference could be 12 in settings, etc.
- EDAs have varying approaches in BER extrapolation, which could lead to drastically different conclusions regarding system margin.
 - Different extrapolation methods also yielded different bathtub curve slopes.
- When jitter/noise and crosstalk are added, converged adaptations are not expected to deviate by a lot. This is generally true for all EDAs.
 - The only exception is with EDA-2 in Case 2, which was unexpected.

Summary (Con't 3)

- When jitter/noise are added (Case 2), all EDAs show reduced EH and EW, i.e., less link performance margin, as expected.
 - However, when crosstalk is introduced (Case 3), four EDAs showed further reduced EH and EW (from Case 2), as expected, but
 - EDA-3 yielded both increased EH and EW.
 - EDA-4 showed increased EW as well.
 - Some EDAs showed very small amount of reduction (EDA-1), while others showed huge degradation (EDA-5).
- In conclusion, we have learned a lot from this work. We will keep working with EDAs to understand the unexpected and inconsistent results, such that we can better address our customers' inquiries and concerns.

Xilinx would like to thank all the six EDAs for their help with using the tools and discussions of the results!

