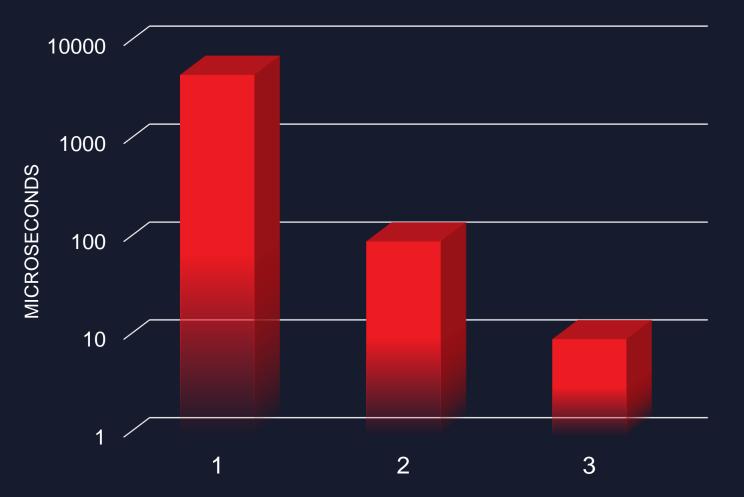
FPGAs: The Key to Accelerating High-Speed Storage Systems

Salil Raje Executive Vice President & GM Xilinx Data Center Business

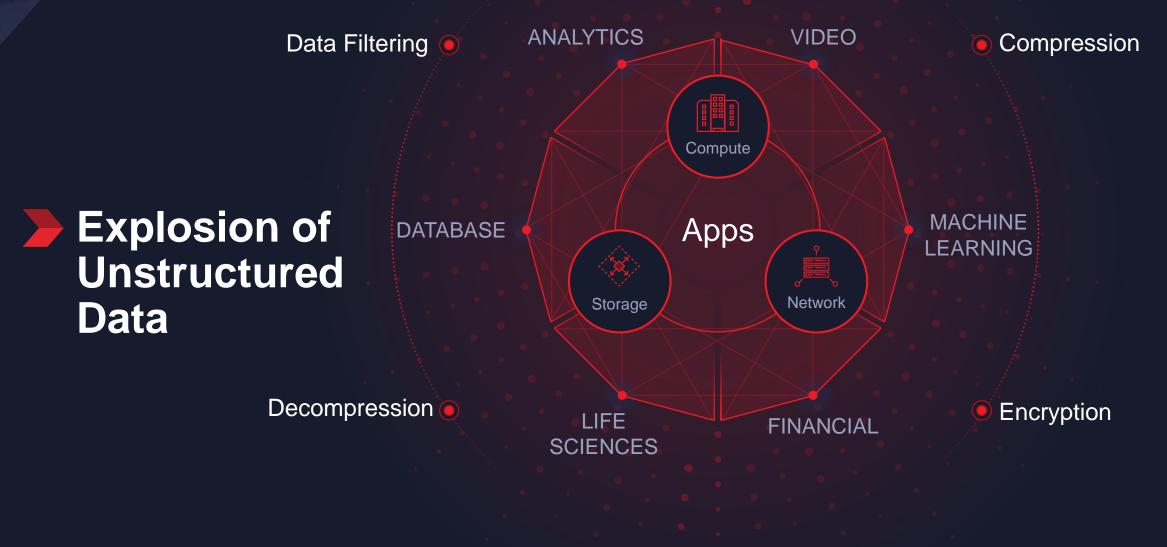


SSDs Have Been a Game Changer for Storage

LATENCY







Data Filtering

Continuously Evolving Standards

Decompression •

Hadoop Spark Aerospike RocksDB Cassandra Foundation DB

LZ Brotli Zipline GZip zSTD Huffman LZ Zipline Brotli

DES AES-XST SHA1-256 Block chain Compression

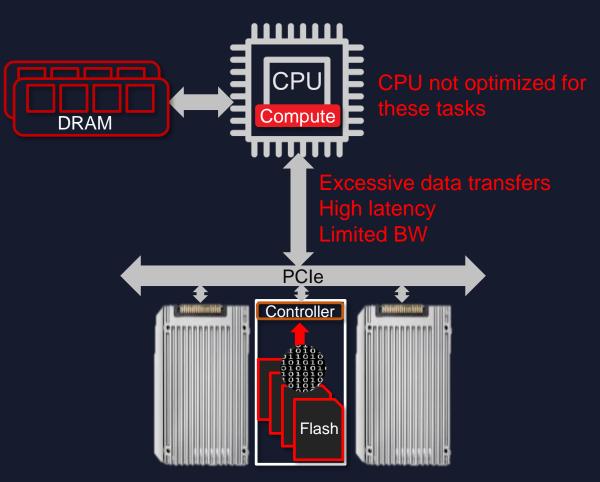
Encryption





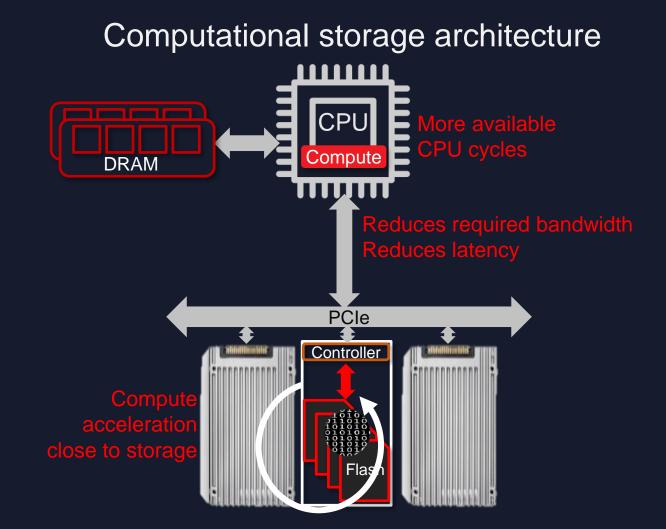
Bottlenecks Remain for Data Intensive Applications

Processor-centric architecture





Emergence of Computational Storage as the Solution





Growing Industry Momentum for Computational Storage





How FPGAs Address the Computational Storage Problem



FPGAs in Storage Today

> Flash controllers



> Storage Systems

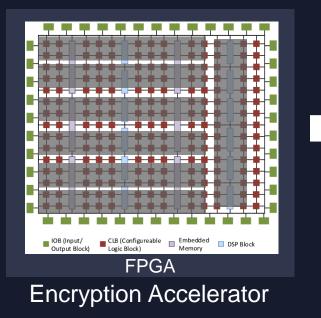
- Cache-offload
- Storage System & Switching connectivity
- » Data Reduction

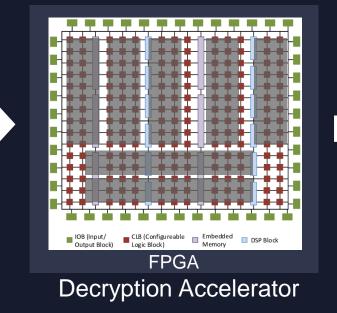


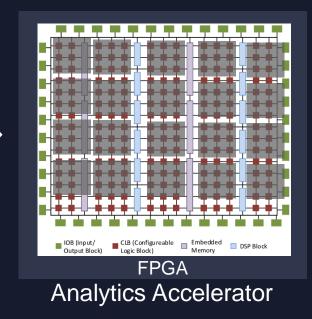


FPGA Advantages for Computational Storage

- > Flexible, fully customizable architecture adapts to specific applications
 - >> Massive parallelism, I/O and customizable data path
- > Performance, power and latency of dedicated HW + reconfigurability of SW
- > More economical than ASIC/ASSP for many applications





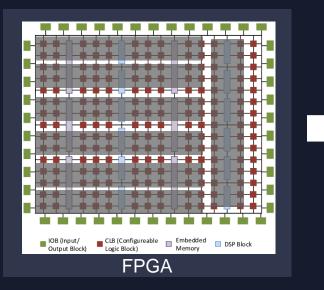




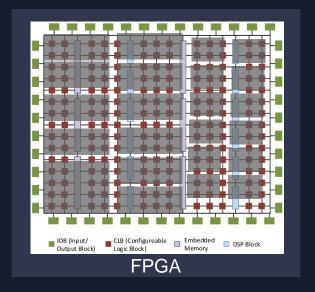
FPGA Advantages for Changing Standards

Architecture easily adapts to latest compression algorithms

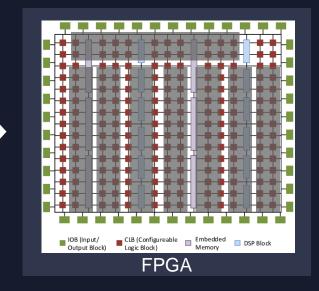
Gzip Accelerator



Brotli Accelerator



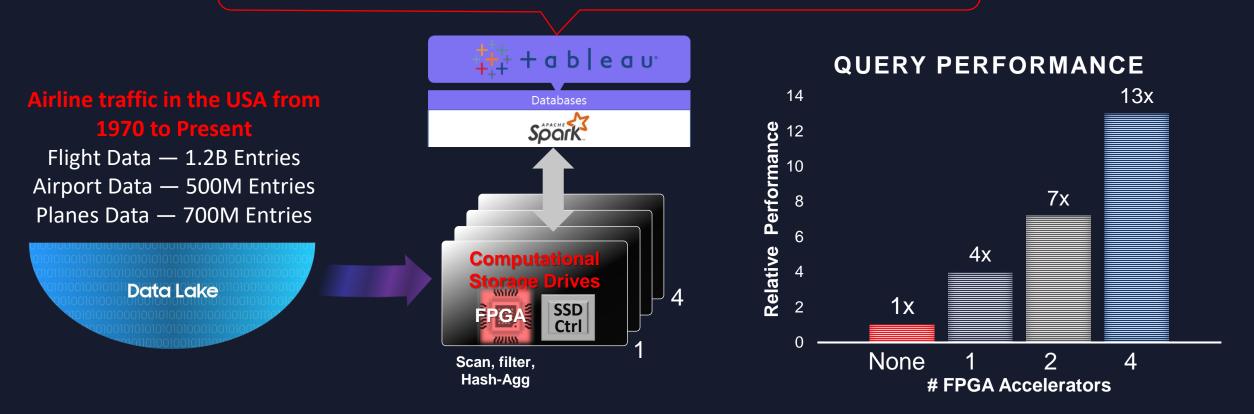
Zipline Accelerator





Example of Analytics Acceleration

Q1: "Which cities originate the most flights with >10min delays? Q2: "Which airport in the Bay Area has the worst record?





Example of Line Rate Hadoop Compression Acceleration

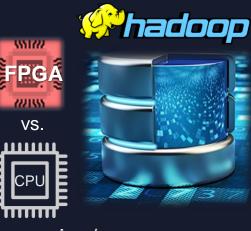
The challenge: Ingest real-time retail sales data during peak shopping season

A Larger object to show of advect and advect of the solution o

mint("please select exactly

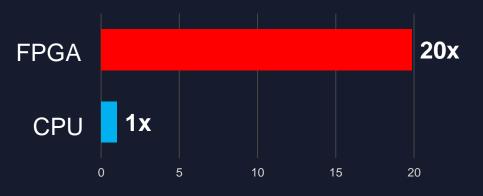
OPERATOR CLASSES -----

X sirror to the selected sect.sirror_sirror_x



Compression / Decompression Acceleration

CPU can't keep up with line-rate data ingestion making compression impractical



Intel Skylake-SP 6152 @2.10GHz CPU (Ubuntu 16.04), GB/s compression per CPU core = .0229. Alveo U50 = 10GB/s



FPGA-based Data Compression Enables Server Consolidation

Without Compression Acceleration



2x Dual CPU Servers With 192TB (uncompressed) With FPGA Compression Acceleration



Single Socket Server 2x Accelerators, 96 TB (compressed)

50% Reduction in Nodes 40% Lower Cost

Intel Skylake-SP 6152 @2.10GHz CPU (Ubuntu 16.04), GB/s compression per CPU core = .0229. Alveo U50 = 10GB/s, Assume 2:1 compression



Computational Storage Deployment Options



Computational Storage Drive (CSD)

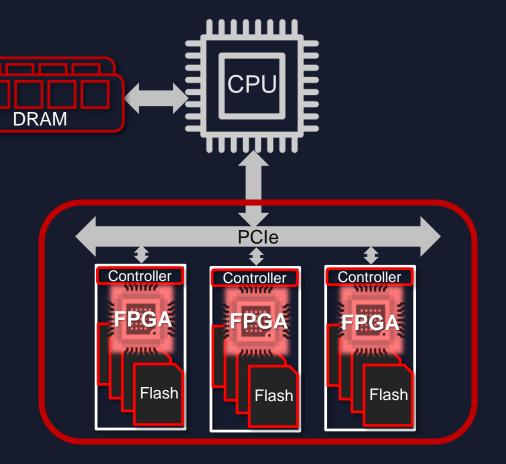
Integrated Accelerator and Flash

> Benefits:

- Easy to implement- plug & play
- Adding capacity adds accelerators + performance
- >> Ability to optimize BW between accelerator and flash
- Ability to customize FTL for specific workloads

> Vendors at FMS:

- Samsung
- Scaleflux





Computational Storage Processor (CSP)

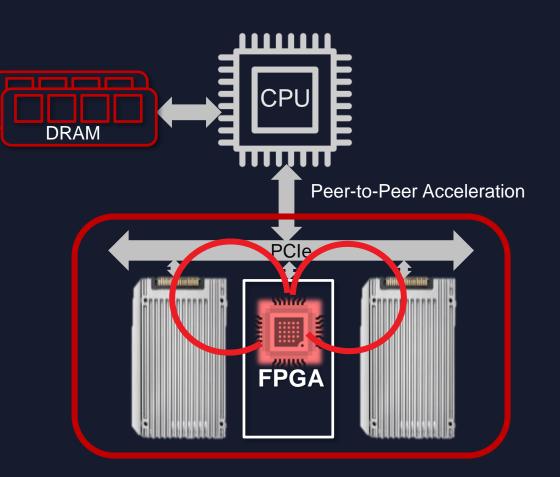
> Accelerator and Storage on same PCIe subsystem

> Benefits:

- >> SSD vendor independence
- Plugs into standard slot
- PCIe Peer-to-peer transfers for high bandwidth and low latency

> Vendors at FMS:

- >> Bittware
- > Eideticom
- Xilinx



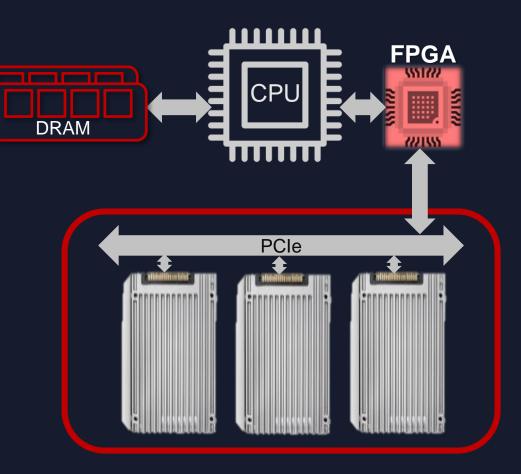


Computational Storage Array (CSA)

> Accelerator in-line with storage

> Benefits:

- SSD vendor independence
- Independently scale accelerators and SSDs
- Ability to optimize BW between accelerator and SSDs
- > Vendors at FMS:
 - Bittware



Future Directions



Current Data Center Architecture: Fixed Resources, Sub-optimal Utilization

	Ethernet													
	SSD	CPU	Accel			SSD	CPU	Accel			SSD	CPU	Accel	
	SSD	CPU	Accel			SSD	CPU	Accel			SSD	CPU	Accel	
	SSD	CPU	Accel			SSD	CPU	Accel			SSD	CPU	Accel	
•	SSD	CPU	Accel			SSD	CPU	Accel			SSD	CPU	Accel	
•	SSD	CPU	Accel			SSD	CPU	Accel			SSD	CPU	Accel	
•	SSD	CPU	Accel			SSD	CPU	Accel			SSD	CPU	Accel	
·	SSD	CPU	Accel			SSD	CPU	Accel			SSD	CPU	Accel	
•	SSD	CPU	Accel			SSD	CPU	Accel			SSD	CPU	Accel	
	SSD	CPU	Accel			SSD	CPU	Accel			SSD	CPU	Accel	



Future Data Center : Disaggregated and Composable

Challenge: Reduced Bandwidth and Increased Latency



Introducing Composable Storage Acceleration

Enables composability without significant performance penalty

> Benefits

- Performance and latency benefits of computational storage
- Scale compute / storage independently
- >> Higher density per rack
- > Lowest TCO

> Vendors at FMS:

>> Xilinx





Future DC: Composable + Adaptable Computational Storage

Reduced network traffic

Ethernet									
	FPGA		SSD		SSD				
•	Accel		SSD		SSD				
•	Storage Accel		SSD		SSD				
•	Storage Accel		SSD		SSD				
•	Storage Accel		SSD		SSD				
•	SSD		SSD		SSD				
•	SSD		SSD		SSD				
•	SSD		SSD		SSD				
•	SSD		SSD		SSD				

- Moves some compute next to the data
- > Network traffic reduced
- > Latency improved
- > Higher utilization with composable infrastructure

Future DC: Composable + Adaptable Network Acceleration

Ethernet

•	CPU	FPGA
	CPU	NIC
•	CPU	Smart NIC

Enables low latency high bandwidths acceleration of network interface workloads.

- > Enables significantly higher packets per second
- > Offloads network functions from the CPU



Future DC: Composable + Adaptive Compute Acceleration

Ethernet

Customizable acceleration up to

100x faster than CPUs for:

- >> Video transcoding
- >> ML inferencing
- Financial modeling

>> ...

	S21111		
•	FPGA	Compute Accel	Compute Accel
•	Accel	Compute Accel	Compute Accel
•	Compute	Compute	Compute
	Accel	Accel	Accel
•	Compute	Compute	Compute
	Accel	Accel	Accel
•	Compute	Compute	Compute
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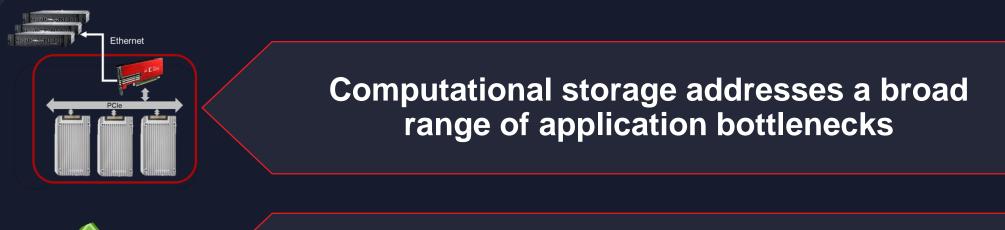


Future DC: Composable + Distributed Adaptive Acceleration

	Ethernet												
_													
•	CPU	Smart NIC		•	Storage Accel	SSD	SSD		•	Compute Accel	Compute Accel	Compute Accel	
•	CPU	Smart NIC		•	Storage Accel	SSD	SSD		•	Compute Accel	Compute Accel	Compute Accel	
•	CPU	Smart NIC		•	Storage Accel	SSD	SSD		•	Compute Accel	Compute Accel	Compute Accel	
•	CPU	Smart NIC		•	Storage Accel	SSD	SSD		•	Compute Accel	Compute Accel	Compute Accel	
•	CPU	Smart NIC		•	Storage Accel	SSD	SSD		•	Compute Accel	Compute Accel	Compute Accel	
•	CPU	Smart NIC		•	SSD	SSD	SSD		•	Compute Accel	Compute Accel	Compute Accel	
•	CPU	Smart NIC		•	SSD	SSD	SSD		•	Compute Accel	Compute Accel	Compute Accel	
•	CPU	Smart NIC		•	SSD	SSD	SSD		•	Compute Accel	Compute Accel	Compute Accel	
•	CPU	Smart NIC		•	SSD	SSD	SSD		•	Compute Accel	Compute Accel	Compute Accel	

- Composable accelerated storage, networking and compute
- Optimized for each workload
- Optimal infrastructure utilization

FPGAs are Key to Accelerating High-Speed Storage Systems





Offers data center operators >5x performance boost and up to 2x reduction of TCO



Xilinx is leading the way in distributed adaptive acceleration



Computational Storage in Action

>Visit Xilinx in booth 313

> Visit our partners

Alpha Data, Bittware, Burlywood, Codelucida, GigalO, Echo Streams, Eideticom, Everspin Technologies, IP-Maker, Mobiveil, Pliops, PLDA, Scaleflux, Smart IOPS, Samsung, SMART Modular, Toshiba Memory America, Western Digital

> Visit our Computational Storage microsite

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> Join SNIA working group for Computational Storage

Adaptable. Intelligent.



