QUALITY REPORT

Shaping the Future
Absolute Quality




XILINX
ALL PROGRAMMABLE™

This report showcases the accomplishments of several of the global Xilinx engineering teams who are responsible for the many milestones successfully reached at 28nm, 20nm and 16nm FinFET.

FOR XILINX, THIS YEAR WAS ALL ABOUT BREAKTHROUGHS. BY SHATTERING RESTRICTIONS INHERENT WITH ASICs AND ASSPs, XILINX LEFT THE COMPETITION BEHIND AND DELIVERED ON THE PROMISE OF OUR ALL PROGRAMMABLE VISION. THE ABSOLUTE QUALITY OF THE NEW PORTFOLIO UNLEASHES THE POSSIBLE, AND ENABLES OUR CUSTOMERS TO MOVE THEIR PRODUCTS A GENERATION AHEAD.

Xilinx's commitment to excellence is exhibited by our continued execution with **ABSOLUTE QUALITY**. We have delivered on this commitment across every family and every device in our product portfolio spanning 28nm, 20nm, and 16nm. Our commitment is further demonstrated by the expansion of our portfolio from FPGAs to the highest capacity 3D ICs, All Programmable dual core SoCs, and heterogeneous multi-processing SoCs offering the highest levels of security and safety. Finally, from a design perspective, our industry-leading ASIC-strength Vivado® Design Suite, expanded IP portfolio, 'software defined' SDx™ Development Environments, and UltraFast™ Design Methodology, incorporate design best practices for both productivity and quality of results. We are proud to say that we have successfully transformed Xilinx from an FPGA company with implementation tools for hardware engineers, to an All Programmable company with programming models required for hardware, software and systems engineers. As a result, Xilinx is enabling customers to rapidly create quality products that are smarter, connected and differentiated, and a generation ahead of the competition.

These investments, engineering innovation, and unwavering commitment led to these successes, and we are extremely pleased with the results. This Quality Report explains our results in terms of:

Execution
Demonstrated with errata free products through our 28nm new product introduction and now extended with 20nm and 16nm results. We will continue to drive leading quality, new product introduction (NPI), & advanced reliability success.

3D Packaging Innovation
Redefining the FPGA landscape with stacked-silicon interconnect technology which exceeds the capacity confines of Moore's Law, and advances test and manufacturing methodologies for known-good die selection.

SoC Integration
Creating simplicity through SoC solutions and elevating the ability to achieve higher quality at the system level.

Design Tools Productivity
Pushing ease of use to new levels through proven design methodologies, predictable QoR, and significantly improved user experiences.

Quality that Builds Trust
With knowledge sharing that drives quality for our suppliers, partners, and customers, driving success throughout the All Programmable ecosystem.

16nm Leadership
Extending Xilinx momentum with a new generation of solutions defined through intimacy with our customers and brought to market through close engineering partnerships with industry leaders.

These are exciting times. As systems and networks evolve to be become more software defined and virtualized, video is everywhere, more machines are connected and augmented with 'vision', wireless moves to 5G, and ever more processing is performed in the cloud, Xilinx continues to deliver new generations of All Programmable devices and design environments with Absolute Quality.

With confidence and pride,

MOSHE GAVRIELOV
President & CEO

VINCENT TONG
SVP, Global Operations & Quality

First to go "all in" at 28nm and 20nm

First to production on 28nm with zero production errata

"Zero-defect" mindset extended beyond silicon to design tools and IP

First to deliver a re-architected, SoC-strength development environment and tool suite

Quality

Building Trust

Quality Proof Points

- RMAs reduced by >68% since 2008
- 46% of customer RMA issues resolved in the field
- Customer scorecard has remained above 9.0 since Q1 2009
- No major excursions or recall for the past eight years
- All Xilinx products meeting <10PPM

Huawei - Gold Core Partner Award
Olympus - Supplier of the Year Award
Agilent - Best Supplier Award
Cisco - Security Award
Fujitsu - Distinguished Partner Award
Anritsu - Supplier Excellence Award
ZTE - Excellent Partner Award
National Instruments - Quality Award

Full-Circle Support and Feedback

Regardless of the amount of in-house testing, analysis, and issue resolution, the most credible and meaningful measures of quality are those that come back from customers. From top to bottom, Xilinx executives, managers, and engineers diligently focus on customers and continually refine Xilinx products, programs, training, and support to deliver optimal results. Key customer-centric feedback includes:

- Validated customer returns (RMAs), which are tracked against products shipped and which show an overall rate of <10PPM (see Figure 1).
- Since 2008, closed-loop customer root cause shows that less than 19% of RMA cases stem from Xilinx issues (see Figure 2).
- Customer feedback (NPS) based on RMA case data shows exceptionally high customer satisfaction.

Frequent and extensive knowledge sharing also helps optimize Xilinx customer successes. Discussions and information sharing, which often include partners and suppliers, provide a high level of transparency through:

- Unique device DNA for more timely device analysis.
- Design checklists and development methodology.
- Design margins, with validated results from design evaluation samples.
- Design issue mitigations, offered at early stages and prior to production release for early adopters.

Spartan FPGA

Product	Technology Node	PPM
Spartan-II/IIE	0.22µm/0.18µm/0.15µm	0.0
Spartan-3	90nm	0.0
Spartan-3E	90nm	0.0
Spartan-3A/3AN	90nm	0.0
Spartan-6	45nm	0.1

Virtex FPGA

Product	Technology Node	PPM
Virtex /-E	0.25µm/0.18µm	0.0
Virtex-II/IIP	0.15µm/0.13µm	0.0
Virtex-4	90nm	0.0
Virtex-5	65nm	0.59
Virtex-6	40nm	9.31
7 series	28nm	2.35

Figure 1: Based on customer return data, CY2014 product PPM demonstrated the Xilinx zero-defect mindset.

TRUST IS EARNED over time, by performing consistently and delivering results that exceed expectations. Xilinx enjoys strong working relationships with customers because of an unwavering commitment to quality. The evidence of this commitment— the true testimonial to Xilinx quality—is the real-world data that focuses on end-user experiences and design results.

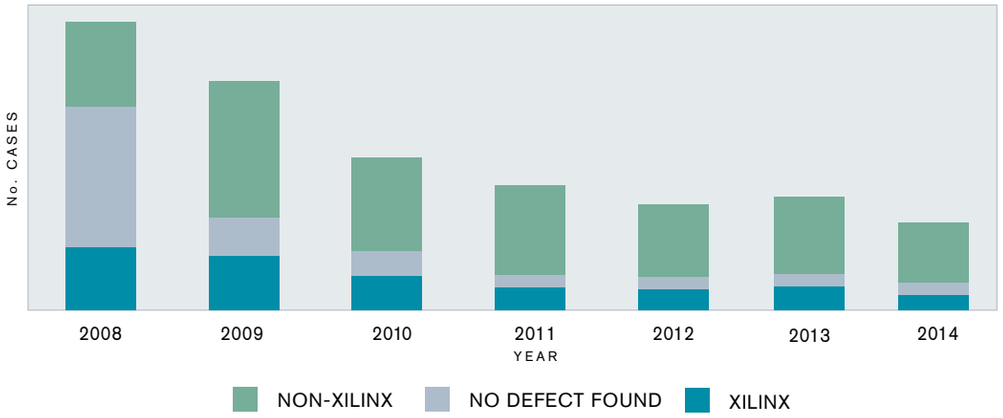


Figure 2: Over the last four years, RMAs have been reduced by >60% versus 2008 levels as a result of product quality, customer support, and direct engagements for issue resolution.

Unleashing Customer Confidence

"With 7 series, UltraScale and Vivado Design Suite, our quality was achieved on the basis of work that began with a clear strategy and a chain of decisions made years ago. The development teams all embrace complete ownership of their results and this ensures that quality emanates from the very source of the innovation. With UltraScale, we maintain our position of being a generation ahead and soon shipping UltraScale+ MPSoC with 16nm node."

WAI KOOI WONG
Vice President, Corporate Quality
XILINX, INC.

The Bottom Line

Xilinx's commitment to excellence is exhibited through our ongoing execution with quality, long term reliability, functional safety, and security always at the forefront. Xilinx and customers—with support from technology suppliers and partners—make up a tightly linked community. The entire ecosystem must succeed to drive up the quality of the end solutions enabled by Xilinx innovations. Periodic quality scorecards provided by customers are therefore the true measure of Xilinx quality (see Figure 3).

Additional Xilinx customer-facing quality hallmarks include:

- Closed-loop focus on root cause.
- On-line RMA portal for real-time customer support.
- Transparent change management and data reporting including horizon reports, reliability, SEU, RMA, and automatic notifications.
- Device DNA (eFuse) and 2D bar coding to track device/die history.
- Executive commitment to improving customer satisfaction.
- Robust control processes and continuous improvements are part of Xilinx's philosophy.

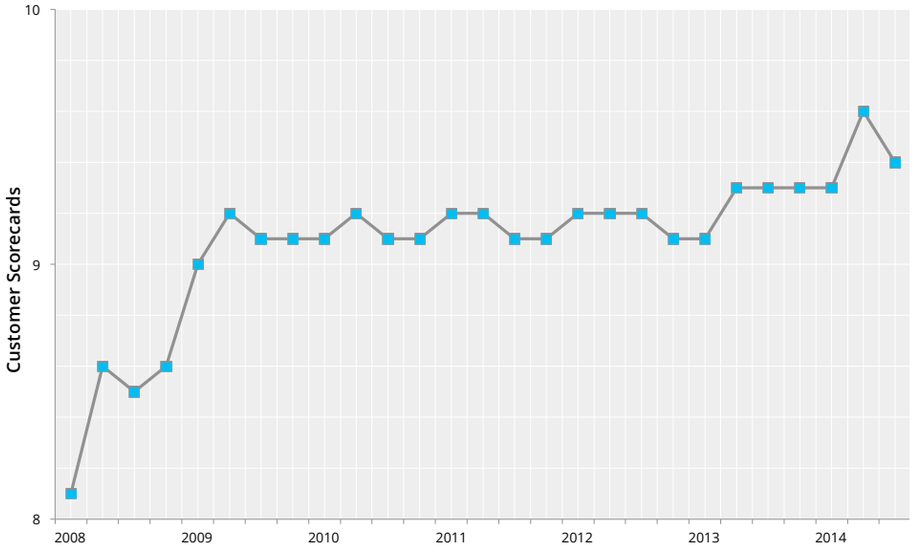
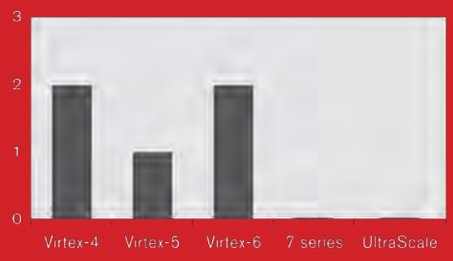


Figure 3: Top management focus on customer feedback and flawless results continue to drive positive customer results.

28/20nm
Execution

Execution Proof Points: Zero Production Errata



- 100% of goals met at each release milestone, with very aggressive specifications
- Stable process, with excellent yield, quality and reliability, and zero production errata
- First silicon ahead of schedule, compared with prior generation
- Scalable optimized architecture for rapid rollouts
- 50X more samples for verification and characterization compared with previous generation
- System level characterization for more customer based evaluations
- Lifetime goals met: 10 years @ 100°C Tj, or 20 years @ 85°C Tj
- Defect densities leading those of prior nodes

Leading Nodes and SoC Wins

Success starts with strong foundational disciplines. At each node, this meant starting by matching the available processes with the technologies Xilinx needed to deliver. At 28nm, Xilinx chose the High-Performance Low-power (HPL) and SoC process at TSMC, and thereby avoided many of the pitfalls other companies experienced at this node. More significantly, this continues to allow Xilinx to deliver industry-leading performance per watt (see Figure 1). The tightly controlled processes, earlier customer engagements, and real-world design rules yield:

- A proven supplier engagement model, including technical engineering and executive-level involvement.
- Process and Performance Learning Vehicles (PPLVs), which resolved many complex issues to accelerate NPI and increase design confidence (see Figure 2).
- Functional margin, moving from 40nm tri-Tox to 20nm dual-Tox.
- A high-k/metal gate process with much lower gate current, resulting in fewer issues and faster time to market.

Actual Hardware Benchmark Results

UltraScale Kintex-7 FPGA Estimator Results

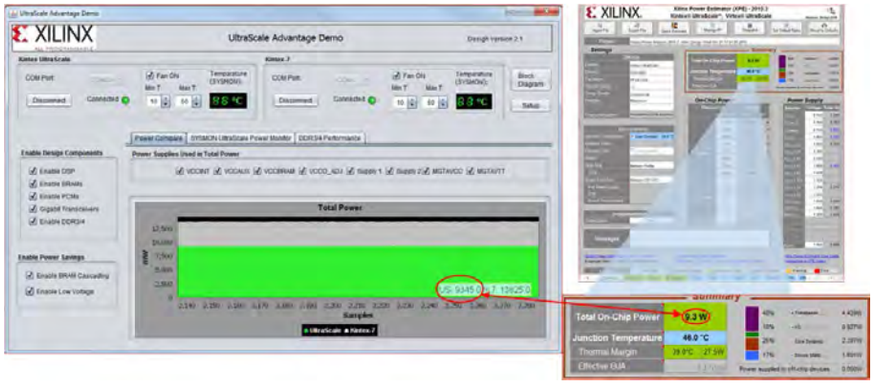


Figure 1: The Xilinx Power Estimator tool was tuned continuously using targeted simulation based on test vehicle results and early architectural learning, giving designers highly accurate results.

NUMBERS TELL THE STORY. The results are in and have ended all debate: Xilinx is a generation ahead at 28nm/20nm. The company embraced a hallmark zero-defect mentality, going "all in" on the HPL/SoC process and one foundry partner. The Xilinx focus on quality and reliability—which spans design, process development, assembly, and test—was guided by fifth-generation new product introduction (NPI) processes and the most stringent release criteria to date.

Driving Success Generation After Generation

Xilinx engineers have proven that they verify, characterize, test, and qualify devices better and faster than anyone else in the industry. All while achieving absolute quality. For five generations, Xilinx's advanced NPI methodology and milestone criteria (see Figure 2) have been tightened to keep ahead of increasing device complexity. At 20nm, the advancements improved data collection, verification, and characterization with:

- Highly automated design flows and timing analysis.
- Verification and characterization processes for earlier identification of issues and earlier corner material (12 weeks sooner than previous generations).
- Test coverage exceeding 99.7%, with earlier data collection.
- "Big data" analysis driving deeper insights into testing and sharing across teams.

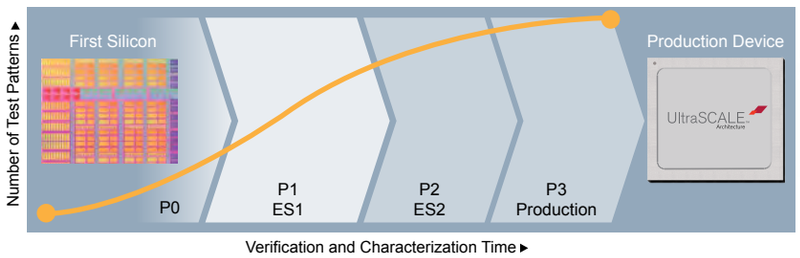


Figure 2: From first silicon to production material ship, Xilinx has redefined its verification and characterization process to drive early discovery to release with zero errata.

Unleashing Silicon Development

"Our 7 series, UltraScale and Vivado Design Suite deliver the leadership value our customers have come to expect from us. Our strategy of designing our All Programmable products with TSMC's leading technology, together with our scalable optimized architecture, and leveraging our industry-leading SOC & stacked silicon interconnect technologies have continued to put Xilinx a full generation ahead of the competition. We have continued to co-optimize 7 series & UltraScale product with the Vivado Design Suite to deliver a high-quality, compelling user experience. Delivering these multiple breakthroughs is a testament to our talented employees and their commitment to creating high-value, high-quality innovative products for our customers."

VICTOR PENG
EVP and GM, Products
XILINX, INC.

Robust Technology Reliability

Xilinx reliability methodologies continued to overcome the shrinking reliability margins at the 16nm process node. By leveraging early learning and in-depth tools expertise, Xilinx engineers shortened development processes from months to days, and accommodated the extra iterations required at 28nm and 20nm. As a result, Xilinx devices are meeting the stringent requirements of the most reliability-sensitive applications in industrial, automotive, aerospace, and defense industries (see Figure 3):

- Enhanced Design-for-Reliability (DFR) guidelines have proven a FIT rate less than 12 at production.
- Improved outlier elimination and new DFR methodology are combating the "shrinking bathtub" curve at 20nm.
- Xilinx engineering and quality assurance programs have yielded proven, predictable, and very-low failure rates over extended device lifetimes. The 20nm devices were released to production with power and defect density (DD) beating previous estimations.

		16nm FF+		20nm SoC		28nm HPL	
Item	Device	LT [yr] @125C	Vmax [V]	LT [yr] @125C	Vmax [V]	LT [yr] @125C	Vmax [V]
TDDB	COREN	32	1.08	15.5	1.06	150	1.17
	COREP	48	1.09	1450	1.18	4.02E+03	1.25
	1.8V ION	1500	2.39	32	2.04	2	
	1.8V IOP	9.00E+06					
Hot Carrier Injection	COREN	375					
	COREP	84					
	1.8V ION	41					
	1.8V IOP	96					
BTI	COREN	1.20E+07					
	COREP	2050					
	1.8V IOP	6270					

Item	Test structure	16nm FF+ Result / LT [yrs]@125C	20nm SoC Result / LT [yrs]@125C	28nm HPL Result / LT [yrs]@125C
SM	Kelvin_Via Via_Chain	Zero Failures from 3 lots	Zero Failures from 3 lots	Zero Failures from 3 lots
Gate Oxide TDDB	MG-M0	300yr	N/A	N/A
	PO-MD1/2	>100	131	N/A
	MxMx	300~600yr	3550	3400
	VxMx		905	1000
Electromigration	High-R Resistor	Jmax > 2x	2x	2x
	M0	Jmax > 4x	4x	N/A
	M1 & 1xM	Jmax >> 2x	2x	2.5x

Figure 3: From 28nm to 16nm, wafer-level reliability exceeds transistor and interconnect market requirements to deliver industry-leading device FIT.

3D PACKAGING Innovation

Innovation Proof Points

- The microbumps (~200,000) and C4 bumps (~20,000) passed all criteria for reliability, older inelastic strain, and fatigue
- Virtex® UltraScale™ FPGA VU440 has ~600,000 microbumps and C4 bumps (>20,000) with 19 billion working transistors
- UltraScale FPGA VU440 has passed all qualification requirements including power cycling at 20nm
- Proven known good die program to drive manufacturing capabilities
- Proven 2nd generation 3D packaging solution

Stress	Conditions	Criteria
HTOL	T=125°C, Vccmax, Dynamic	Pass
PC	3x Reflow	
	Ramp up 30°C to 130°C in 3 minutes	
	Hot Dwell 6 minutes at 127°C - 130°C	
	Ramp down: 130°C to 30°C in 3 minutes	
	Cold Dwell: 6 minutes at 27°C - 30°C	
THB	MSL4; Ta= 85°C, RH= 85%, Alternative Bias	
TH	MSL4; Ta= 85°C, RH= 85%	
HTS	3x Reflow, Ta= 150°C	
TC-B	MSL4, -55°C / +125°C	

More and More...than Moore

More on a chip and more die integrated on a single device—for more advanced systems. The world's first monolithic 3D FPGA (see Figure 1), the Xilinx Virtex-7 FPGA V2000T and now the Virtex UltraScale FPGA VU440, represent a breakthrough in all of these dimensions that required very stringent qualification and test. The industry's second generation 3D IC required further advancements, including:

- Low loss organic packaging for robust board level reliability & optimal signal integrity.
- Optimization of package substrate material and interposer resistivity to achieve 33Gb/s system channel characteristics.
- Design and timing verification of high-performance inter-die interconnects.
- 3D thermal-mechanical modeling and analysis for package reliability, addressing package co-planarity issues and stresses introduced by the interposer.

To learn more about these Xilinx advancements, please visit www.xilinx.com/quality.

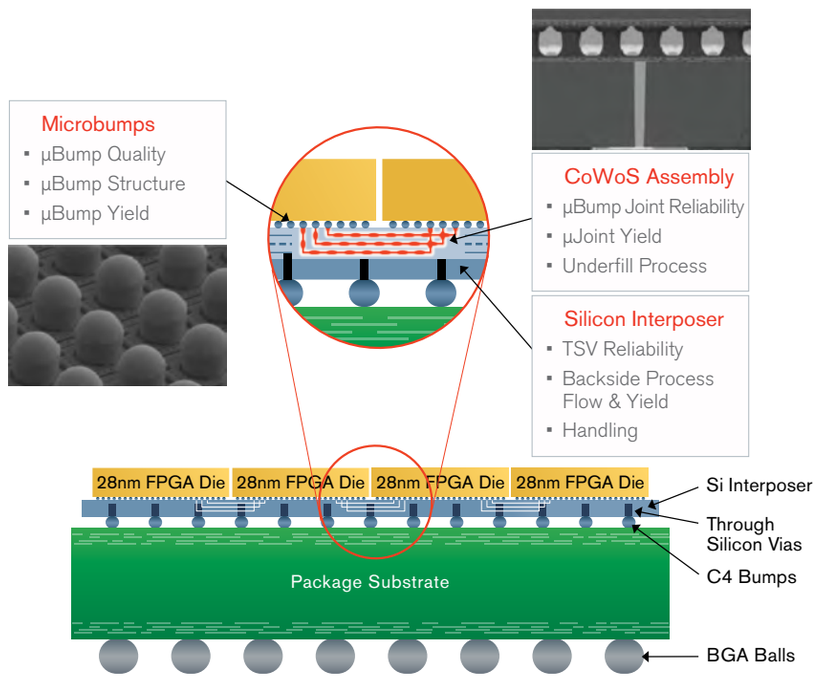


Figure 1: SSIT cross-section showing key quality considerations on a typical qualified SSI device using TSMC's CoWoS process.

STACKING SILICON PUSHES THE LIMITS, and allows Xilinx to set new standards for capacity and performance. Xilinx-innovated Stacked Silicon Interconnect technology has driven devices beyond the confines of Moore's Law, both for monolithic and heterogeneous devices. To mitigate the risks associated with stacked silicon and meet quality goals for breakthrough 33Gb/s devices, Xilinx used early learning from lead-free flip-chip test vehicles (ranging from 90nm to 20nm) and leading-edge modeling and manufacturing methodologies that address the increased complexity.

More Integration

Stacked silicon offers the inherent advantage of selecting "like" products in terms of power consumption and speed, which means more predictable results than monolithic silicon. A comparison of simulated and actual eye diagrams demonstrates this exceptional quality (see Figures 2 and 3). The methodologies behind the industry's first 28nm (28Gb/s) 3D IC heterogeneous devices and now extended at 20nm (33Gb/s) are fully integrated to meet performance and specifications. Selection starts with solid test and manufacturing methodologies at the assembly site, and includes:

- Ensuring multiple-die performance by adding system timing checks to characterization process.
- DFM rules that provide performance advantages.
- Enabling power die optimization during selection, through fully integrated die testing at wafer sort, now standard across the 7 series, UltraScale, and UltraScale+™.
- FPGA self-diagnostic capabilities for higher test coverage confidence.
- Reliability prediction, using a custom hierarchical, end-to-end tool that draws on a Xilinx design database.
- Expanded wafer qualification using three additional elements for assembly testing: electrical, thermal, and mechanical.

Unleashing Stacked Silicon

"To push beyond conventional thinking and break through Moore's Law in delivering our 3D IC solution, we continue to deliver a superb level of engineering excellence. In doing so, we opened up a new frontier for combining technology building blocks, from cost-effective component die. This could not have been accomplished without a laser focus on prevention and flawless engineering execution from Xilinx and our supply partners."

LIAM MADDEN
CVP, FPGA Development and Silicon Technology
XILINX, INC.

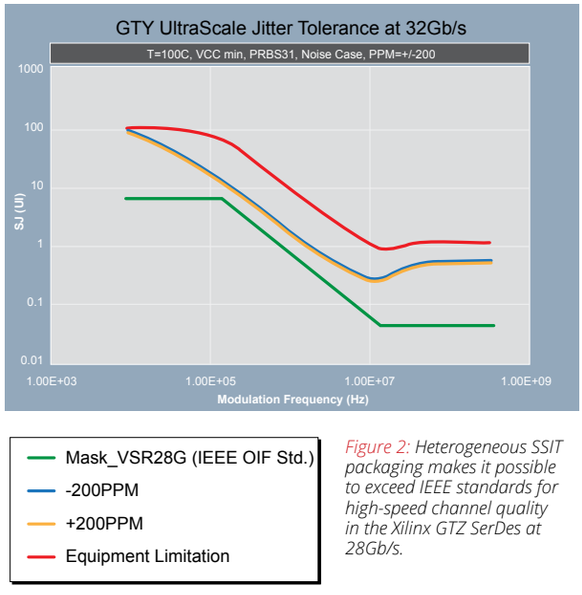


Figure 2: Heterogeneous SSIT packaging makes it possible to exceed IEEE standards for high-speed channel quality in the Xilinx GTZ SerDes at 28Gb/s.

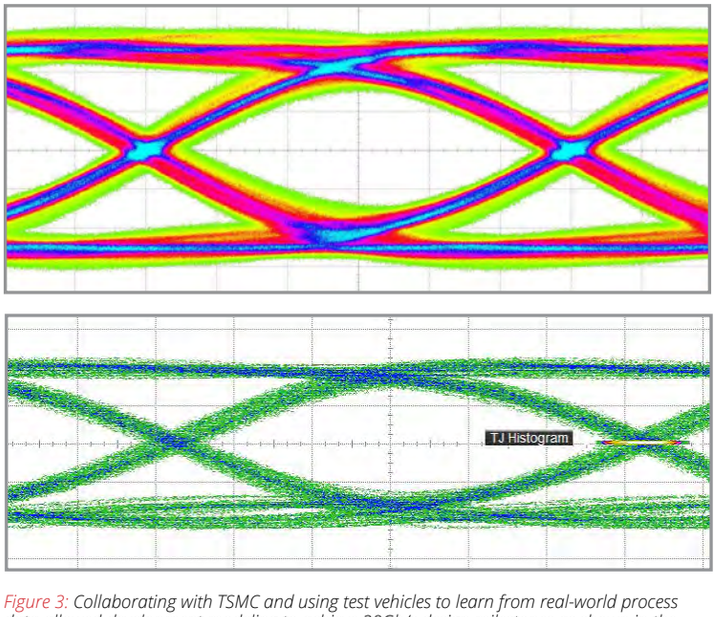


Figure 3: Collaborating with TSMC and using test vehicles to learn from real-world process data allowed development modeling to achieve 28Gb/s design milestones as shown in the simulated (upper) and actual (lower) eye diagrams.

SoC Integration

SoC Characterization and Verification

- Carried out under conditions that align with the most stringent customer requirements
- Block characterization improvements for GTX and for BRAM:
  - New Verilog flow
  - Customization of build-in self-test (BIST) march sequence
- Tests run using memory test boards, varying attributes, and test conditions that exceed specifications by 10%
- Additional corner-case and volume system testing with critical IPs
- 3X increase in the number of targeted reference designs* (TRDs) compared with previous generation
- 3X increase for exercising non-processing areas (connectivity, DSP, AMS, etc.)

** The Vivado tools are used for design testing, which makes this testing part of the critical release criteria for the tools themselves.*

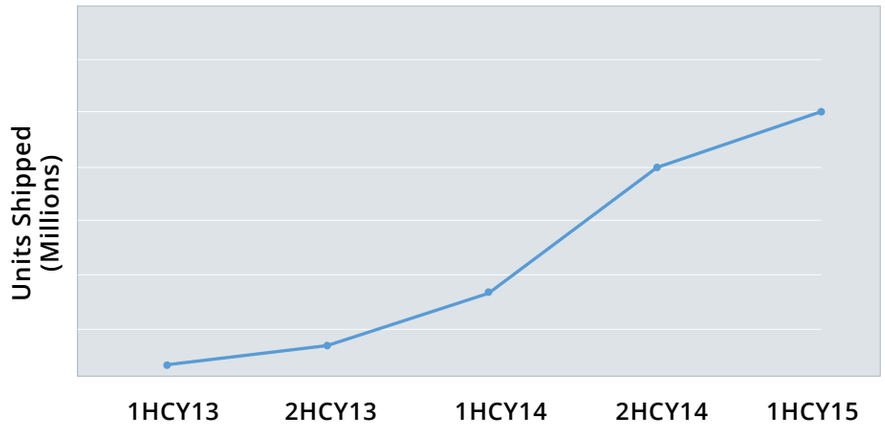


Figure 1: Leveraging the FPGA learning from our scalable optimized architecture, Xilinx was able to de-risk the Zynq SoC evaluation and to launch in record time.

Simplified Solutions

The Zynq® SoC and MPSoC devices replace chip-to-chip latencies with high-speed FPGA-processor connections, giving designers the latest Xilinx advancements such as 7 series and UltraScale+ SerDes to support maximum throughput and capacity for SoC designs. Engineers and system architects can leverage SoC capabilities, implement accelerators in the device's processing system or its programmable logic, and bring more complex designs to market with confidence in the quality of the total solution. Besides leveraging learning and enhancing design tools, Xilinx has introduced new mechanisms for integrating system-level verification of target specifications for the processor subsystem, logic, and IP (see Figure 1). The scalable optimized architecture and common blocks across the 7 series FPGAs and SoCs contributed to absolute quality and accelerated the rollout of devices. After verification of the first Kintex®-7 325T based device, many 28nm devices went straight from first tape out to production.

IT TAKES MORE THAN LOGIC. Xilinx has redefined integration by wrapping industry-leading logic and I/O fabric around an ARM® processor subsystem. This industry-first leveraged learning that began more than 10 years ago with the Virtex-II Pro and continued through Virtex-4 and Virtex-5 PowerPC designs. Xilinx proprietary approaches for testing and characterizing FPGA and processor interactions now yield an advanced, robust SoC that simplifies design and unleashes future generations of All Programmable systems.

System-Level Quality

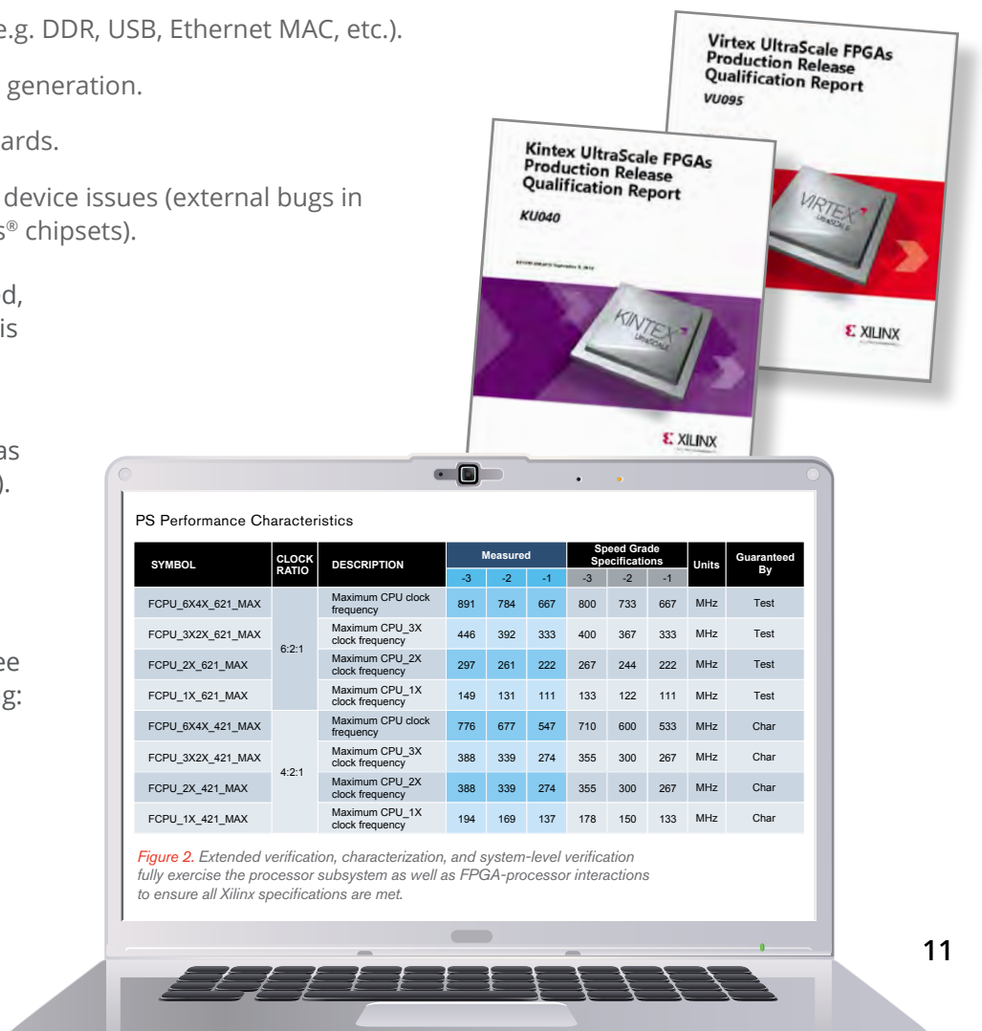
The role of FPGAs has evolved from "glue logic" and rapid prototyping to today serving as the heart of advanced systems. Device testing has similarly evolved to track more advanced applications, with system-level testing being a significant component in the Xilinx quality equation. Zynq SoC quality, while benefiting from many proven practices, called for further refinements at every stage of development and was driven by a balanced focus on silicon verification, system-level performance, and extensive, holistic testing:

- Prior to silicon, extensive emulation leveraged the EDK platform and booted operating systems such as Linux.
- Rearchitected verification and characterization approaches solidified the on-chip FPGA fabric.
- Randomized continuous testing of the processor subsystem exercised the SoC-unique feature set:
  - Guidelines stem from the Xilinx embedded software initiative, aimed at processor-IP testing.
  - Verification IP for all Xilinx interfaces (e.g. DDR, USB, Ethernet MAC, etc.).
  - Constrained-random and random test generation.
  - Compliance testing for interface standards.
  - Results: catching more than just Xilinx device issues (external bugs in other components such as PCI Express® chipsets).
- Processor-FPGA interactions were tested, during which the processor subsystem is the master.
- Additional SoC-specific characterization and verification were performed, such as Open Verification Methodologies (OVM).
- Stringent coverage and metric-driven verification performed on the SoC (see Figure 2).
- Expanded wafer qualification using three additional elements for assembly testing: electrical, thermal, and mechanical.

Unleashing Customer Acceleration

"As design complexity and integration increase, our customers demand top quality system solutions to accelerate their design capabilities. The Zynq platform provides a fully verified prebuilt processing system completely validated along with its associated software and tools. With this platform, Xilinx delivers the highest level of performance and quality, which our customers expect."

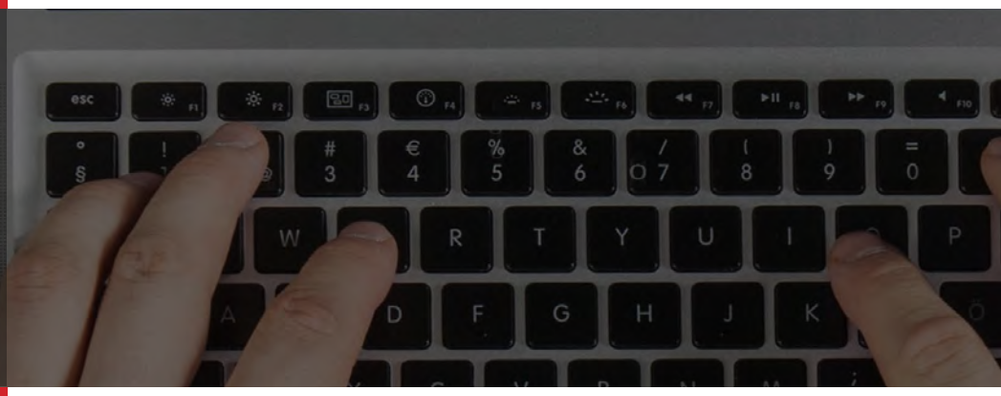
VAMSI BOPPANA
Vice President, Processor Development
XILINX, INC.



SYMBOL	CLOCK RATIO	DESCRIPTION	Measured			Speed Grade Specifications			Units	Guaranteed By
			-3	-2	-1	-3	-2	-1		
FCPU_6X4X_621_MAX	6:2:1	Maximum CPU clock frequency	891	784	667	800	733	667	MHz	Test
FCPU_3X2X_621_MAX		Maximum CPU_3X clock frequency	446	392	333	400	367	333	MHz	Test
FCPU_2X_621_MAX		Maximum CPU_2X clock frequency	297	261	222	267	244	222	MHz	Test
FCPU_1X_621_MAX		Maximum CPU_1X clock frequency	149	131	111	133	122	111	MHz	Test
FCPU_6X4X_421_MAX	4:2:1	Maximum CPU clock frequency	776	677	547	710	600	533	MHz	Char
FCPU_3X2X_421_MAX		Maximum CPU_3X clock frequency	388	339	274	355	300	267	MHz	Char
FCPU_2X_421_MAX		Maximum CPU_2X clock frequency	388	339	274	355	300	267	MHz	Char
FCPU_1X_421_MAX		Maximum CPU_1X clock frequency	194	169	137	178	150	133	MHz	Char

Figure 2. Extended verification, characterization, and system-level verification fully exercise the processor subsystem as well as FPGA-processor interactions to ensure all Xilinx specifications are met.

Design Tools
Productivity



Ever Expanding Testing Base

Vivado Quality Initiatives

- TL9000 audited standardized processes
- High quality and continuous nightly builds
- Extensive daily regression suites with over 220,000 nightly tests
- Weekly regression testing of over 50K interactive, batch, formal checking, directive random and hardware testing
- Robust release checklist and criteria
- Functional safety certified in 2016

Vivado IP Quality Initiatives

- XVI - Xilinx Verification Initiative (Functional Verification) – UVM based methodology
- Viper - Next generation verification across all Vivado IP - 80,000+ IP test jobs per day
- System Level Validation (SLV) - Over 120 different IP tested, over 1500+ systems tested daily

Ecosystem Participation in Release Testing

- Early partner/ecosystem participation in all releases
- Real-time debugging, using partner IP, for testing and improved quality
- Extended requirements and tier definitions for ecosystem partners to include Vivado training and proficiency
- Results: Hundreds of products already on 7 series and UltraScale; more than 50 partner IP cores supporting AXI, several vendors providing evaluation cores from inside the Vivado Design Suite

Bringing Design Vision to Life

The Vivado Design Suite represents a major advancement in ease of use for All Programmable developers. Vivado accelerates integration, implementation, verification and debug for 28nm, 20nm and 16nm (see Figure 1). Vivado has been designed to handle exponential growth in device densities reaching 10s of millions of logic cells.

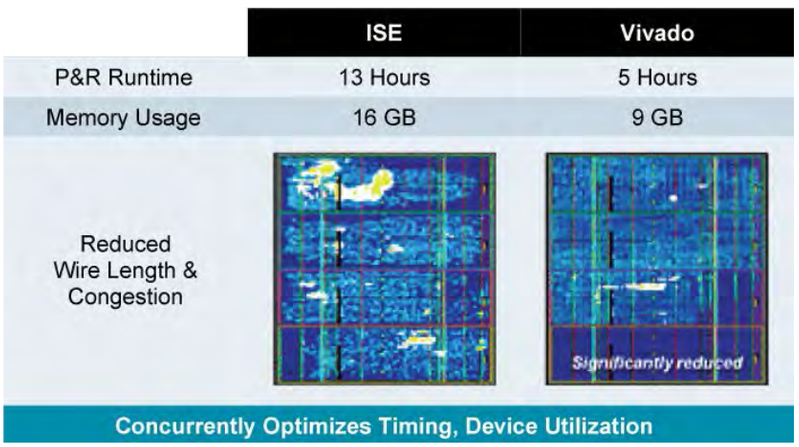


Figure 1: The Xilinx design suite was rearchitected to enhance the customer experience and provide superior quality of results. Customer summary data reflects success based on these goals, and will drive further advancement of Vivado.

- The UltraFast Design Methodology: Delivers the first comprehensive set of design methodologies in the programmable industry. Xilinx collected the best practices of expert users and distilled them into an authoritative set of methodology guidelines.
- Production proven: Used on 90% of all 7 series designs and 100% of UltraScale/UltraScale+.
- The Tcl API: Designers have the flexibility of working in a scripted Tcl environment, an interactive Tcl shell, or a graphical project tool. Tcl also allows much more in-depth testing (better coverage) of Vivado.
- TcL App Store: Xilinx, Alliance partner and customer Tcl Apps to streamline development.

TIME IS MONEY. Even breakthrough innovations such as Xilinx All Programmable devices require the right tools to achieve maximum value and deliver the highest level of quality. The Vivado Design Suite delivers a SoC-strength, IP-centric and system-centric, next generation development environment that has been built from the ground up to address the productivity bottlenecks in system-level integration and implementation. The Vivado Design Suite is a generation ahead in overall productivity, ease-of-use, and system level integration capabilities. Vivado tools provide 4X faster implementation, 20% better design density and up to 3-speed grade performance advantage all while improving designer productivity with key features such as IP Integrator to rapidly assemble Xilinx, customer and 3rd party plug-and-play IP and High Level Synthesis for C/C++ based IP generation.

Predictable User Experiences and Design Methodology

The Xilinx zero-defect mindset was applied to the Vivado Design Suite from the beginning and feedback from customer scoring indicates that the quality of the Vivado tools has consequently exceeded expectations (see Figure 2). Stringent testing and release criteria has provided continuous improvement to the tools and IP. In addition, the UltraFast Design Methodology for the Vivado Design Suite enables project managers and engineers to accelerate productivity and quickly tune their sources, constraints and settings to accurately predict schedules. Now in its second edition, the guide covers all the aspects of:

- Board and Device Planning
- Design Creation and IP Integration
- Implementation and Design Closure
- Configuration and Hardware Debug

The Vivado Design Suite automates part of the UltraFast Design Methodology by providing linting rules and templates for optimal HDL coding style, and XDC timing and physical constraints.

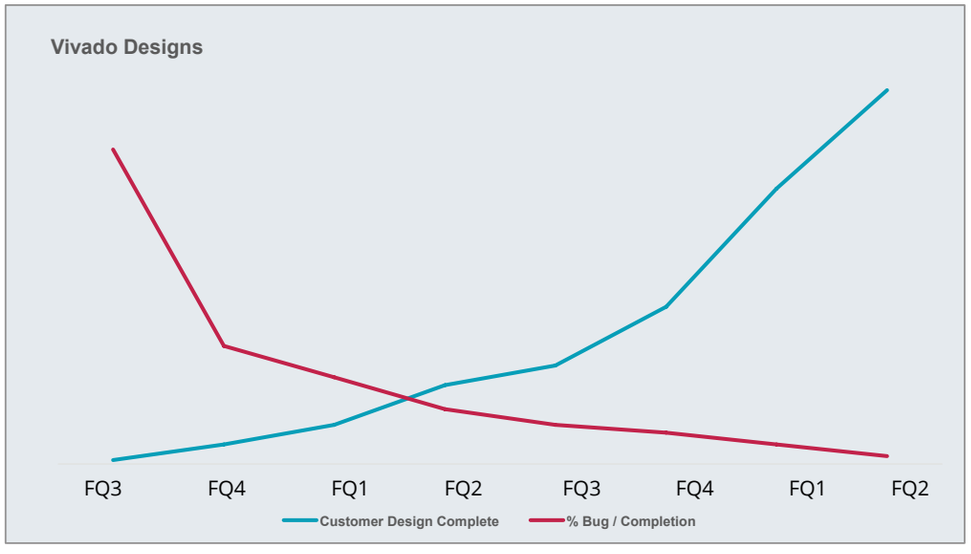


Figure 2: Earlier and more stringent testing and verification mitigate the risks that stem from increasing complexity. Testing with higher-level customer designs increased the prerelease discovery and resolution of issues. With more issues identified during development, the impact on customers is minimized and design cycles are accelerated for higher-quality products and an improved user experience.

Unleashing FPGA Possibilities

"As design complexity increases, in step with quantum increases in capacity and performance of integrated solutions, the need for a revolutionary design environment has become compelling. Our strategy in building a completely new platform of design tools architected around a shared, scalable data model have showed successful results. Vivado has continued to provide the highest-quality results and productivity for all customers."

SALIL RAJE
VP, Software and IP Products Development
XILINX, INC.

16nm
Leadership

Building on 20nm Innovations Proof Points

- Leveraging 28nm learnings and a scalable, optimized architecture
- Second-generation 3D IC/PS architecture leveraging proven technology
- Second-generation high-k/MG reduced process variation (i.e., gate-last, high-k-last)
- NMOS elevated source/drain, PMOS eSiGe to boost performance
- Intact design, verification, and integration teams to carry forward HPL expertise
- UltraScale architecture for simple migration between planar and FinFET nodes

Staying a Generation Ahead at 16nm

Xilinx began developing the 16nm UltraScale+ family in 2012. Before shipping the first 20nm UltraScale device, our proven approach for 16nm was well under way. Since then, the lessons learned at 20nm have helped Xilinx refine 16nm process and product qualification methodologies, including extended temperature testing and a renewed focus on wear-out data and reliability estimations. In addition, Xilinx is introducing major testing changes stemming from early DFT specifications. The new opportunities for Xilinx leadership and innovation at 16nm will include FinFET transistors, double-patterning lithography, gate dielectric scaling, increasing I/O and packaging complexity, scaling power, and overall changes to testability and reliability.

A World-Class Team

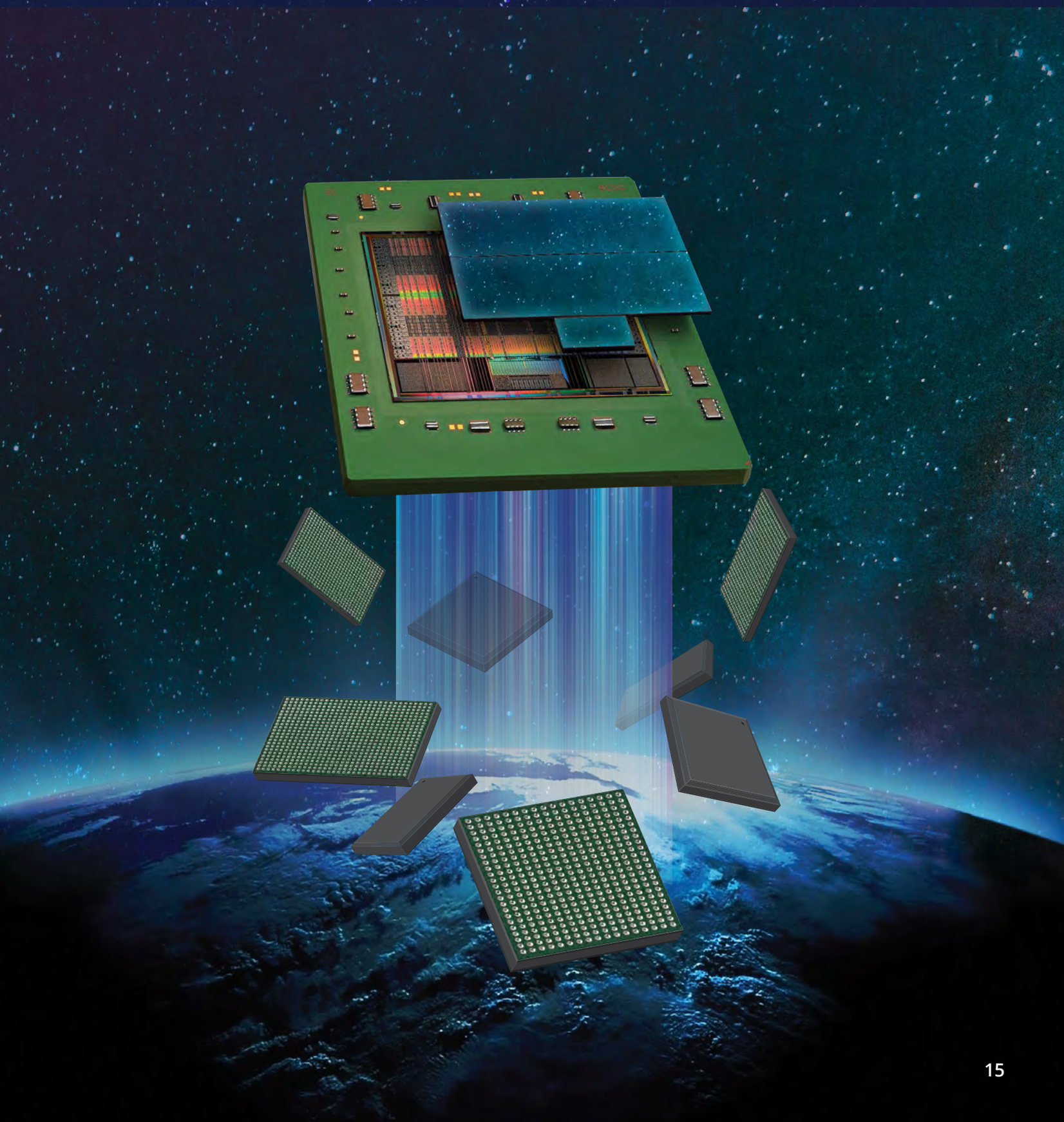
In collaboration with TSMC and our supply chain partners, Xilinx is driving solutions to all of the 16nm challenges. This extended ecosystem will continue to play an expanding role in the introduction of the next-generation devices. In addition, our “Voice of the Customer” initiative continues to grow as IP, design tools, and silicon become more integrated solutions. Supporting the world-class Xilinx extended team is a solid foundation of engineering achievements based on learning from previous generations.

On Track

Xilinx, together with TSMC, is on track to deliver 16nm technology products. Built on a proven foundation, including third-generation SSIT and embedded ARM processor architecture, Xilinx is delivering a significant boost in performance/watt from TSMC’s 16FF+ FinFET 3D transistors. Optimized at the system level, UltraScale+ delivers value far beyond a traditional process node migration – providing 2–5X greater system level performance/watt over 28nm devices, far more systems integration and intelligence, and the highest level of security and safety.

In collaboration with TSMC, the journey continues with the development of the 7nm process and 3D IC technology for its next generation of All Programmable FPGAs, MPSoCs, and 3D ICs. The technology represents the fourth consecutive generation where the two companies have worked together on advanced process and CoWoS 3D stacking technology, and will become TSMC’s fourth generation of FinFET technology. The collaboration will provide Xilinx a multi-node scaling advantage and build on its outstanding product, execution, and market success at 28nm, 20nm, and 16nm nodes.

CHALLENGES GIVE RISE TO INNOVATION. With the release of each generation of devices, Xilinx introduces technology advances that overcome existing limitations, allowing engineers to build more value into electronic systems. First to market with UltraScale and 16nm FinFET UltraScale+ All Programmable FPGAs, 3D ICs and SoCs, Xilinx has built on the momentum and market leadership established at 28nm and has delivered for three consecutive generations All Programmable device innovation ahead of the competition — a 3-Peat.



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