

A GENERATION AHEAD FOR SMARTER SYSTEMS: 9 REASONS WHY THE XILINX ZYNQ-7000 ALL PROGRAMMABLE SOC PLATFORM IS THE SMARTEST SOLUTION

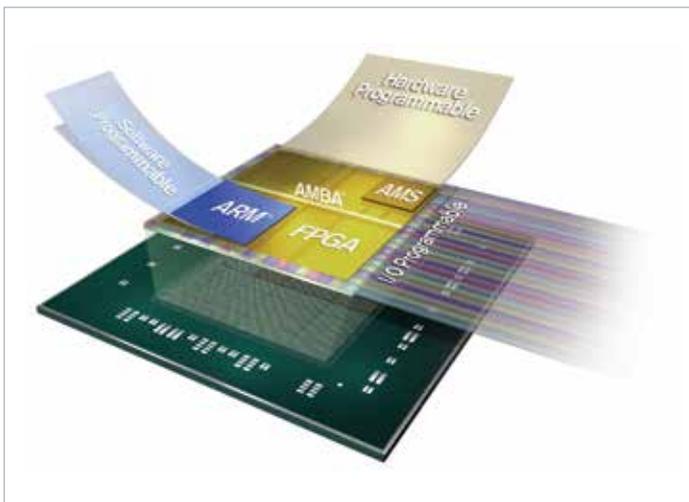
Introduction to Smarter Systems

The global electronics industry is undergoing a transition to smarter systems. The drivers behind this change are all connected to requirements involving efficiency, productivity, security, quality, and of course cost. The enemy is waste. Systems reduce waste when they use only the required resources to deliver only the desired goods and services when and where they are needed. The opportunity is intelligence. Systems that can make their own decisions can change the role of electronics in our businesses and everyday lives. To achieve these goals, systems must be able to obtain, process, interpret, and make choices based on a wide variety of information from remote and local databases, sensor data, and many other dispersed inputs.

What does this transition to smarter systems mean to system vendors? It means that there must be more decision-making technology and intellectual property. The networks that convey essential information are being transformed from dumb pipes to smart ones. Buildings are becoming smarter so that light and heat are delivered only where needed. Highly integrated networking has come to the factory floor to ensure that every system has access to critical data needed to make decisions. Robots within these factories combine information from databases with machine vision to become more efficient. Energy grids are becoming smarter so that electricity infrastructures can handle the changing loads of complex societies. Automobiles are becoming smarter through vision systems and wireless communications to increase drivers' safety and to help drivers handle the increasing traffic congestion in urban areas.

The Xilinx Zynq™-7000 All Programmable SoC is the ideal platform to infuse intelligence into today's embedded systems. It is All Programmable, meaning that not only can one add systems intelligence through software, but additional data processing and decisions can be executed in real time with programmable hardware and system interfaces can be optimized and evolved through programmable I/O. All this intelligence can be added with low design costs and tremendous flexibility to change the design or upgrade in the field. It also enables a significant level of programmable systems integration, including CPU, DSP, ASSP, FPGA, and mixed signal functionality. This leads to lower BOM cost, higher systems performance, and lower system power. Systems based on the Zynq platform can literally be shipped the same day if desired.

THREE PROGRAMMABLE ASPECTS OF THE ZYNQ-7000 ALL PROGRAMMABLE SOC PLATFORM DEVICES



Xilinx Zynq-7000 All Programmable SoCs are the fastest, smartest way to create smarter systems. These devices fuse a fast processor system based on two 1GHz ARM® Cortex™-A9 MPCore processors with the industry's fastest and most advanced 28nm FPGA fabric, multiple high-speed serial transceivers, and an on-chip analog-processing block that incorporates two 1Msamples/sec A/D converters. Xilinx recently introduced a fifth member of the Zynq-7000

All Programmable SoC family—the Zynq Z-7100—with enhanced DSP resources in the FPGA fabric. All five Zynq devices are optimized for specific combinations of system power, cost, and size.

Xilinx is leading the industry to usher in the trend to smarter systems with application-focused solutions for smarter networks, data centers, and vision-based systems. These solutions build on the Zynq-7000 All Programmable SoC with an ever expanding portfolio of building blocks for smarter systems called SmartCORE™ IP, a new generation of design tools called Vivado™ that includes the ability to design at higher abstraction levels, a variety of application design kits, and system-level expertise to help the rapid design and implementation of smarter systems.

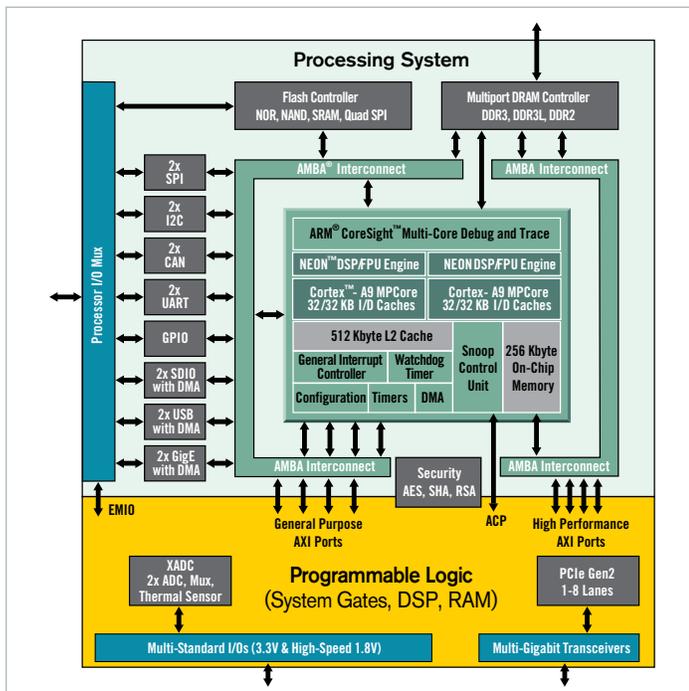
Zynq: A Generation Ahead

Xilinx Zynq-7000 All Programmable SoCs are a generation ahead of alternatives and the smartest solution to a wide range of system-design problems in all markets, across the entire application spectrum. Here are 9 reasons why this is true:

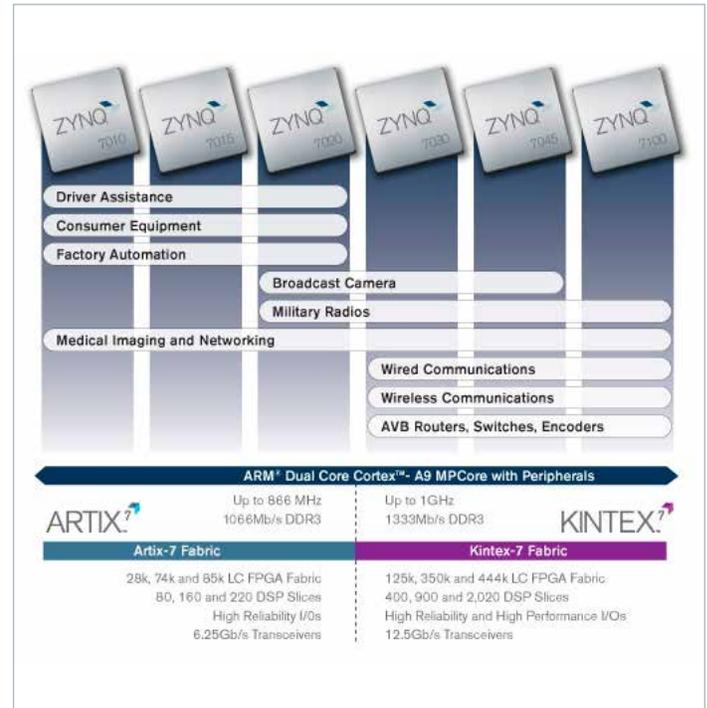
Reason 1: Most efficient ARM+FPGA for analytics and control

A 1GHz, dual-core, hardened implementation of the ARM Cortex-A9 microprocessor sits at the heart of each Zynq All Programmable SoC. The two ARM processors communicate with on-chip memory, SDRAM and Flash memory controllers, and peripheral blocks through the ARM AMBA AXI-based interconnect. Together, these hardened blocks constitute the Zynq-7000 All Programmable SoC's Processor System (PS).

THE ZYNQ-7000 ALL PROGRAMMABLE SOC



THE ZYNQ-7000 SOC FAMILY: FIVE MEMBERS SPANNING A RANGE OF APPLICATIONS



The on-chip PS is attached to the Zynq device's on-chip Programmable Logic (PL) through multiple ARM AMBA AXI ports, creating extremely efficient coupling between these two key components of the Zynq architecture. There are two 32-bit AXI master interfaces; two 32-bit AXI slave interfaces; four 64-bit configurable and buffered, high-performance AXI slave interfaces; and one 64-bit AXI ACP (Accelerator Coherency Port) interface. That's nine AXI interfaces in total linking the Zynq PS to the PL.

The number and size of these ARM AXI PS-PL connections is a critical architectural choice—a choice based on a careful consideration of the bandwidth requirements of the Zynq PS. The four 64/32-bit configurable, high-performance AXI ports provide the PL with direct, high-speed access to the Zynq-7000 All Programmable SoC's on-chip memory and SDRAM controller through four independent 1Kbyte FIFO buffers. In this way, several separate hardware accelerators implemented in the Zynq PL can have independent, high-speed access to a Zynq-based system's main memories. If that access needs to be coherent with the on-chip caches, then the accelerators implemented in the PL can employ the 64-bit ACP connection, which is directly attached to the ARM Cortex-A9 MPCore processor's snoop control unit.

There are four more 32-bit AXI ports connecting the Zynq PS and PL in addition to the 64/32-bit configurable AXI ports. These ports provide a connection between the Zynq PS and any peripheral-type IP blocks implemented in the Zynq PL.

Reason 2: Most extensive OS, middleware, and stack ecosystem

All of this hardware requires software to harness it and the Xilinx Zynq platform includes an extensive OS, middleware, and stack ecosystem. OS support includes many Linux variants (Xilinx's own PetaLinux, Wind River's Linux 5, and Timesys' LinuxLink), Android from iVeia and Adeneo, Microsoft's Windows Embedded Compact 7, and several real-time operating systems including Xilinx's FreeRTOS, Wind River's VxWorks, Green Hills Software's INTEGRITY, ENEA's OSE, Express Logic's ThreadX/NetX, ETAS' RTA-OS SC1-4, eSOC's eT-Kernel, Micrium's μ C/OS, Mentor Embedded's Nucleus, and Quadros from Quadros. These operating systems span the applications universe from communications, automotive, and industrial to consumer and medical.

The Zynq platform also has the largest software ecosystem, by far, with software-development tools available from Xilinx and from leading tool vendors including ARM, Microsoft, Mentor Embedded, Green Hills Software, Wind River, Kyoto Microcomputer, Yokogawa, Computex, Abatron, and Lauterbach and design help from more than 30 Design Service Ecosystem Alliance Members.

Xilinx also offers several specialized software- and hardware-design solutions for Smarter Networks, Smarter Video, Advanced FOC (Field-Oriented Control Loop) motor control, security, and other applications. In addition, the Zynq platform benefits from the huge ecosystem of middleware, and stack vendors offering products and services specifically for the ARM Cortex-A9 MPCore processor including:

- Audio codecs
- Video codecs
- Graphics
- Imaging
- Image processing and recognition
- Face recognition
- Cryptography
- Secure systems operation
- File systems
- Networking
- Databases
- Power management

Reason 3: Highest level of security and reliability

Smarter systems must meet stringent requirements for security and reliability and the Zynq platform has many features that aid a design team's efforts in designing safety features and secure operation. With respect to secure operation, the Zynq platform is unique in always booting the processor side first, FPGA side second. If desired, the boot sequence supports user authentication (RSA), encryption (AES-256) and data authentication (HMAC). The authenticated and decrypted code is then placed into on-chip memory where it executes only after it's safely stored away from prying eyes. This is the only secure way to boot a device like the Zynq-7000 All Programmable SoC and this technique has been reviewed by our toughest aerospace and defense clients who know a ton about security.

Xilinx put these features into the Zynq-7000 platform after conferring with interested clients. That's one of the reasons why Zynq-7000 SoCs support the AES and SHA algorithms in hardware. The competition has AES built into its on-chip FPGA configuration manager, but apparently uses it only for decrypting the FPGA configuration bit stream. It does not appear that the competition's hardware AES decryption applies to the processor boot code. In addition, it seems that the only way to securely boot the competition's device is to configure the PL first, and then boot the PS. It is unclear how, if any, thought was given to how to keep Trojan software from being inserted into the device prior to securely booting the PL. There are clearly many unanswered questions regarding Altera's solution.

In addition, Zynq devices include unique Anti-Tamper (AT) technology. These features are critical not only for defense programs, but also for commercial customers who are looking to protect their IP. A detailed list of these features is found in the Xilinx XAPP1084 document and provided in a ready-to-integrate IP solution called the Security Monitor (SecMon). On-chip A/D converters and a temperature sensor allow a Zynq device to monitor its environment so that it can "zeroize" itself including its AES key if it senses any indication of tampering. No competing device offers these generation-ahead secure features based on four device generations worth of development in this arena.

Many system parameters go into operational reliability but one frequently discussed issue involves single-event upsets (SEUs). There are obvious SEU symptoms such as memory errors but the real issues are at the system-level. Xilinx has done extensive

28nm testing using accepted labs and testing standards with respect to SEUs. Xilinx FPGAs have been rolling along on Mars in rovers for years and recently helped to capture the elusive Higgs Boson at CERN's Large Hadron Collider in the Swiss Alps so Xilinx is quite familiar with SEUs. Xilinx's high-reliability, generation-ahead 28nm silicon exhibits the lowest intrinsic SEU FIT rate of any commercial SRAM-based technology, based on LANSCE (Los Alamos Neutron Science Center) beam testing according to JESD89A/89-3A. These devices are ideal for long-life applications. The Xilinx SEU advantage is further extended with SEU mitigation and analysis solutions including fully supported soft error mitigation IP (SEM IP), an SEU FIT rate calculator, publicly available data and test methods, and expert design guidance. Xilinx's dedicated focus on silicon reliability and SEU FIT rate makes its devices the clear choice for systems developers targeting systems requiring the highest performance with unsurpassed levels of integration in a programmable device.

There are also other aspects to system reliability beyond SEUs. For example, all members of the Zynq family have an on-chip thermal sensor and on-chip A/D converters with an analog multiplexer so that Zynq devices can monitor their own environment including temperature levels and power supply voltages. System designers can also connect intrusion photodetectors and other analog sensors to the Zynq platform's analog inputs to create fail-safe systems that are aware of any environmental challenges to safe systems operation. These kinds of features are required to meet new regulations such as the new IEC 61508 standard with its multiple Safety Integrity Levels (SILs).

Unmatched Performance and Power

None of the above capabilities are compelling unless supported by the best performance at the lowest possible power consumption. Those terms define the Zynq-7000 All Programmable SoC platform. Performance comes from a powerful mix of high-performance components and architectural decisions. Low-power operation is based on the right choice of 28nm process technology—TSMC's 28nm HPL process in the case of Xilinx's Zynq platform—coupled with the right design choices to take full advantage of what the process technology offers.

Reason 4: The only 1GHz, dual-core ARM Cortex-A9 MPCore processor

Xilinx's use of the TSMC 28nm HPL process technology has resulted in a device family that offers unmatched performance with low operating power, starting with the 1GHz dual-core ARM Cortex-A9 MPCore processor. The ARM microprocessors in the fastest speed-grade Zynq-7000 All Programmable SoCs operate faster than the microprocessors in any competitive device. To a first-order approximation, faster processors deliver more performance but there are other significant performance-defining factors—memory in particular.

Reason 5: The largest and highest-performance memory system

By itself, the best processor performance does not ensure a high-performance system. Memory performance also plays a significant role and the Zynq platform features the fastest SDRAM memory controllers available. The hardened SDRAM controller in the Zynq platform's PS can operate SDRAMs as fast as DDR3-1333. Memory controllers placed in the on-chip FPGA fabric of Zynq devices with Kintex™-7 PL can drive SDRAMs as fast as DDR3-1866 and you can place multiple copies of these SDRAM controllers in the PL if needed.

The Zynq-7000 All Programmable SoC's hardened SDRAM controller supports 32- and 16-bit SDRAM widths with parity and 16-bit SDRAMs with ECC. If your design requires 32-bit SDRAM with ECC or 64- or 128-bit SDRAM with or without ECC, then the soft-core version of the Xilinx SDRAM memory controller can provide that capability—with even more performance.

Reason 6: Lowest power and fastest logic fabric

The Zynq platform gives you two choices for the PL based on the industry-leading 28nm Xilinx Kintex-7 and Artix™-7 FPGAs. The higher-speed Kintex-7 FPGA fabric is optimized for the best mix of price and performance with performance comparable to the previous-generation, high-end Xilinx Virtex®-6 FPGAs at half the power consumption (twice the power/performance). The Artix-7 FPGA fabric is optimized for the lowest power and cost, delivering twice the performance of the previous generation Spartan®-6 FPGAs with a 50% reduction in operating power. Depending on the design, Artix-7 FPGAs offer on average 15% higher performance that competing low-end 28nm FPGAs and Kintex-7 devices are on average 50% faster than competing mid-range 28nm FPGAs.

The scalable, optimized architecture shared by the 7 series FPGA families including the Kintex-7 and Artix-7 fabrics in the Zynq-7000 All Programmable SoC family of devices inherently produces more portable RTL and IP. Since the lowest-level building blocks of the architecture are shared across all of Xilinx's 7-series FPGA fabrics, design teams can port hand-coded RTL with

block instantiations of memories, DSP blocks, or logic elements to any member of the Zynq-7000 series without modifications or time-consuming re-optimizations.

Proven Productivity

The Xilinx Zynq platform unlocks the door to design productivity by allowing design teams to create new designs at any programmable abstraction level—software or hardware. The Zynq platform's two 1GHz ARM Cortex-A9 processor cores can execute ARM-targeted software faster than competing solutions so development teams can spend less time and effort optimizing code. For more speed, software development teams can transform key algorithms into hardware accelerators that can be instantiated in the Zynq PL and plugged into the Zynq SoC's AXI interconnect. Vivado HLS can make this task quick and efficient by converting C, C++, and SystemC code into hardware. In addition, logic designers can create more hardware blocks that further enhance a system design's ability to rapidly execute tasks.

The Zynq platform is uniquely oriented towards getting design teams from concept to implementation in the absolute minimum amount of time. That's the definition of productivity.

Reason 7: Industry-leading high-level synthesis

Do you want to know the secret way to go from algorithm to high-speed logic in a minimum amount of time? It's called High-Level Synthesis (HLS). Algorithm developers can write their algorithms in C, C++, or SystemC and then debug these algorithms on PCs and servers. When the algorithm is proven, the fastest way to implement the algorithm is to simply recompile the code to run on one of the Zynq platform's ARM Cortex-A9 MPCore processors.

But what if that implementation is not fast enough? Then you need a hardware implementation. Before HLS, hardware implementation required a logic designer's touch to recode high-level algorithms written in C, C++ , or SystemC in VHDL or Verilog. It was a slow, manual, error-prone process that required lots of debugging. With HLS, the process goes a lot faster. Feed C, C++, or SystemC code into the HLS tool and out comes the HDL code needed to implement a hardware accelerator, complete with AXI interface, ready to plug into the Zynq SoC's FPGA fabric.

The Xilinx HLS tool is part of the Vivado Design Suite and it's a central feature that permits rapid development of hardware accelerators that speed execution of critical tasks on the Zynq platform. The HLS tool included in the Xilinx Vivado Design Suite provides synthesizable support for a large subset of all three input C standards (C, C++ and SystemC) enabling it to synthesize hardware from the C code with minimal modifications. The Vivado HLS tool performs two distinct types of synthesis upon the design:

- Algorithm Synthesis takes the content of the functions and synthesizes the functional statements into RTL statements over a number of clock cycles.
- Interface Synthesis transforms the function arguments (or parameters) into RTL ports with specific timing protocols, allowing the design to communicate with other designs in the system.

The Vivado HLS tool can perform a number of design optimizations to produce high quality RTL satisfying performance and area goals. Although the sequential nature of the C language (and its lack of concurrency) puts artificial dependencies on operations that must wait their turn for execution, the Vivado HLS tool has the ability to automatically pipeline both functions and loops to ensure the RTL design does not suffer from such limitations.

Vivado HLS is the system designer's secret weapon for rapid development of hardware accelerators.

Reason 8: Widest selection of software environments and tools

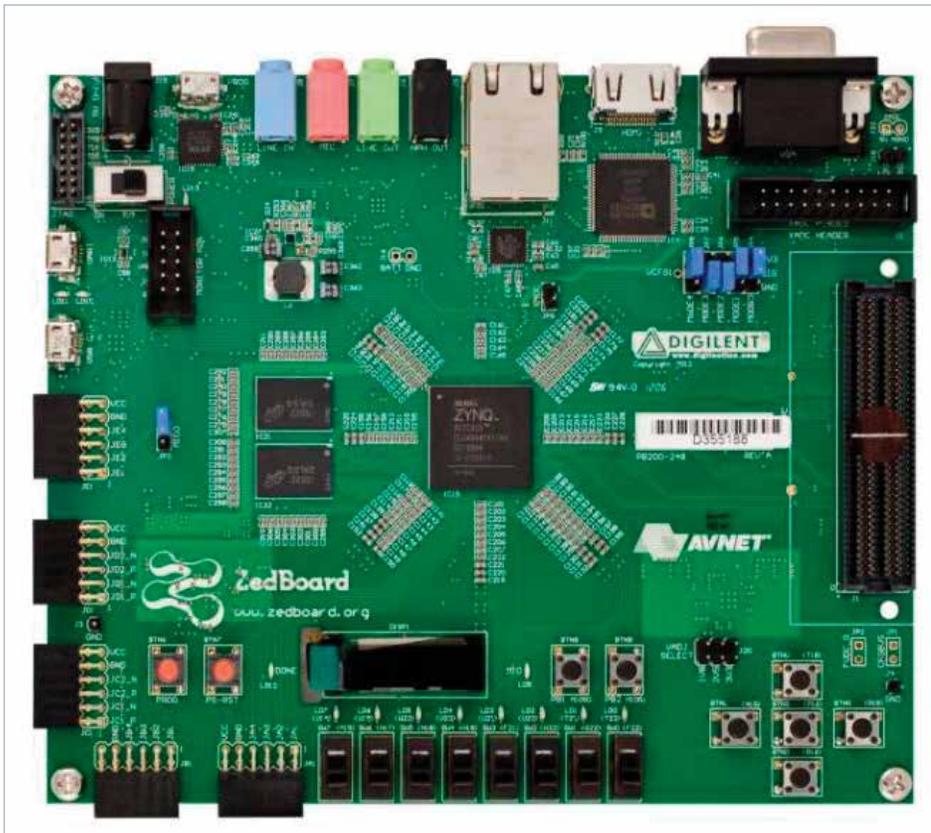
It's no secret that software-development teams have preferred tools and that these preferences vary from team to team; sometimes from project to project. Consequently, it's critical for a universal development platform, like the one based on the Xilinx Zynq-7000 All Programmable SoC family, to offer design teams a choice of development tools. Xilinx provides a free software-development tool suite to enable Linux-based and bare-metal software development plus multi-core software debugging.

Leading third-party development environments and tools for the Zynq platform include the ARM Development Studio 5 (DS-5), the Mentor Sourcery CodeBench toolchain, the Wind River WorkBench, Green Hills' MULTI IDE, Microsoft Visual Studio, Lauterbach TRACE32 PowerTools, the Computex PALMiCE3 and PALMiCE2H debuggers, and Kyoto Microcomputer's PARTNER debugger.

Some Xilinx partners offer very advanced, high-level software-development tools. For example, The MathWorks supports model-based design for the Zynq-7000 platform using both MATLAB and Simulink with support for continuous test and verification throughout the design. MATLAB is the leading environment for developing technical computing applications. Simulink is the leading environment for system-level modeling, simulation, and verification. These two development tools from The MathWorks are widely used for developing many diverse applications including:

- Motor control
- Computer and machine vision
- Wireless communications
- Data analysis
- Security and surveillance
- Robotics

THE ZYNQ-BASED ZEDBOARD FROM ZEDBOARD.ORG



Together, MATLAB and Simulink can reduce design cycle time by as much as 80% compared to hand-coding methods.

In addition, National Instruments has demonstrated support for Zynq-based platforms with its LabVIEW FPGA graphical development environment. LabVIEW is a system-design platform and development environment employing a visual, dataflow programming language originally developed by National Instruments in 1986.

Reason 9: Largest portfolio of IP, design kits, and reference designs

Xilinx offers a large number of IP blocks, design kits, and reference designs to help design teams get a head start in creating new systems. Over the past several years, for example, Xilinx has acquired strategic IP vendors such as Sarance, Omiino, Modesat, and Modelware in addition to internally developing additional IP blocks to create a massive collection of SmartCORE IP that aids in systems development for smarter networks.

Design teams needing to start immediate development need instant platforms and Xilinx offers several hardware- and software-based development platforms including:

- The ZedBoard low-cost evaluation board
- The ZC702 Evaluation Kit for developing non-video application
- The Zynq Video and Imaging Kit
- The Zynq SDR Kit for developing wireless applications
- The ZC706 Evaluation Kit for systems requiring high-speed SerDes transceivers

The Zynq-7000 SoC Virtual Platform—a software-based emulation platform that allows you to develop simulation-friendly system models that you can instantly email to developers anywhere in the world

In addition, a growing number of third-party vendors including iVeia, Enclustra, and V3 Technology offer evaluation development boards based on the Xilinx Zynq platform.

Bonus Reason

Reason 10: Award-winning technology

The Zynq-7000 family and Zynq platform has won numerous industry awards and received two very prestigious awards at the end of 2012. The first was the Analysts' Choice award for Best Embedded Processor of 2012 from the Microprocessor Report, published by the Linley Group. The award issue of the Microprocessor Report said:



“Keeping in mind the notion that creativity lies at the intersection of distinct points of view, we selected Xilinx’s Zynq Z-7020 (see MPR 3/7/11, “Xilinx ReARMs FPGAs”) as the Best Embedded Processor of 2012. From one perspective, Zynq is an FPGA, but from another, it is an embedded processor. It’s not exactly either, but the Z-7020 and products like it will change the embedded-processor business—stealing sockets from conventional processors and opening new design opportunities.”

The second award was presented by Electronic Products Magazine, which wrote:



“We selected the Zynq-7000 All Programmable SoC for this year’s Product of the Year award, recognizing Xilinx as the pioneer FPGA company offering the industry’s first all programmable SoC to incorporate an ARM® dual-core Cortex™-A9 MPCore™ processing system with tightly coupled programmable logic and I/O on a single die,” said Jim Harrison, editor of Electronic Products. “We distinguish that Xilinx’s unique technology combination dramatically increases performance and therefore improves processing-intensive applications across multiple markets, ranging from consumer and broadcast equipment to wired communications, amongst many others”

Conclusion

End-market applications that require multi-functionality, high-speed signal processing, and real-time responsiveness drive the need for smarter systems with higher levels of embedded system performance. Applications such as smarter video and vision (driver assistance, surveillance, and automation), smarter networks, smarter data centers, smarter aerospace and defense (military and avionics systems), and smarter broadcast (cameras, content, and transmission) possess several common requirements including:

- Advanced decision and control processing
- Complex user or control system interfaces
- Control and analytics based on multiple input streams of complex data
- High-performance, low-latency signal processing

All of these applications are under pressure to meet tighter deadlines with constantly evolving requirements with smarter systems that scale from cost-effective to feature-rich solutions.

The Xilinx Zynq-7000 All Programmable SoC platform is the smartest solution for developing smarter systems for these nine reasons:

- Most efficient ARM + FPGA for analytics and control
- Most extensive OS, middleware, and stack ecosystem
- Highest level of security and reliability
- Only All Programmable SoC with two 1GHz ARM Cortex-A9 MPCore processors
- Largest and highest performance memory system
- Lowest power and fastest logic fabric
- Industry-leading high-level synthesis
- Widest selection of software environments and tools
- Largest portfolio of IP, design kits, and reference designs

These factors coupled with the flexibility of hardware, software, and I/O programmability enable customers to reduce development times and investments, resulting in improved financials and faster time-to-market and time-to-money. Furthermore, system definition risk is greatly reduced and possibly eliminated while upgrades/updates are enabled, making it easier to service systems and end customers.

Unrivaled performance, optimized partitioning, lower power, lower cost, lower risk, improved financials, system flexibility, scalability, upgrade-ability, supported by world-class tools, ecosystems, IP based on industry open standards and familiar programming environments—these are compelling attributes.

Call your local Xilinx office now to get more information about Xilinx's Zynq-7000 All Programmable SoC platform, which can provide huge development efficiencies and large opportunities for differentiation in your next smarter system design projects.

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