

Versal™ Premium Series with AI Engines

Built for Extreme Signal Processing

OVERVIEW

The Versal Premium series delivers industry-leading adaptive signal processing capacity by integrating AI Engines.

While providing 4X signal processing capacity¹ compared to previous generation FPGAs, the Versal Premium series also includes highly scalable serial bandwidth, power-optimized networking IP cores, and massive on-chip memory to eliminate data movement bottlenecks.

As a heterogeneous compute platform, Versal Premium series enable a significantly reduced size, weight, and power (SWaP) advantage for a wide range of signal processing intensive applications in aerospace & defense and test & measurement markets.

HIGHLIGHTS

Architectural Innovation for Industry-Leading Adaptive Compute Performance

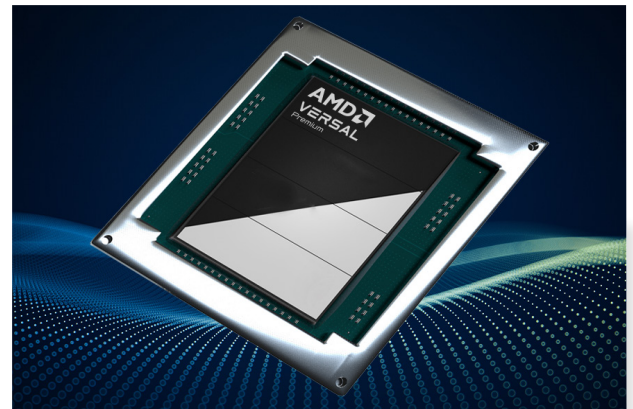
- > 4X signal processing capacity vs. previous generation FPGAs
- > Customizable memory hierarchies and locality to maximize bandwidth and minimize latency per workload
- > Re-architected programmable logic at 2X density vs. previous gen FPGAs

Eliminating I/O Bottlenecks to Support Higher Density Antennas and Devices Under Test (DUTs)

- > Offers scalable serial bandwidth in a smaller area with power efficiency
- > Provides secure, multi-terabit networking via integrated connectivity IP
- > Enables high-density antenna and DUT designs with a breadth of protocols

Reduced Size, Weight, and Power (SWaP) through Heterogeneous, Power-Optimized Integration

- > 4X more processing in a 67% smaller footprint at 43% lower power
- > Eliminates additional processor ICs for smaller, lower power designs
- > Simplifies system-level development and debug



TARGET APPLICATIONS

RADAR

- > Digital Array Radar (DAR)
- > Adaptive Beamforming
- > Space Time Adaptive Processing (STAP)
- > Synthetic Aperture Radar (SAR)

SIGNALS INTELLIGENCE

- > RF Machine Learning
- > Digital RF Memory (DRFM)
- > Direction Finding
- > Digital Receiver / Exciter (DREX)

WIRELESS TESTERS

- > 5G Protocol Tester
- > 5G Production Tester
- > WLAN Device Tester
- > Wireless Network Tester

SEMICONDUCTOR AUTOMATED TEST EQUIPMENT (ATE)

- > RF Transceiver
- > Analog/Mixed signal
- > Radar/Camera Sensor
- > SoC

1: Total equivalent DSP Engine capacity vs. Virtex™ UltraScale+™ VU13P FPGA

FEATURES

| FEATURE HIGHLIGHTS | |
|---|---|
| AI Engines | <ul style="list-style-type: none"> > Tile-based architecture of 1.3GHz VLIW/SIMD vector processors > Array of interconnected cores with terabytes-per-second of interface bandwidth to other engines for greater compute throughput > Up to 10CTOPs with CINT16 and FP32 compute bandwidth for signal processing > C/C++-programmable, compile in minutes, and library-base design for framework developers |
| DSP Engines | <ul style="list-style-type: none"> > Enhanced architecture for fixed point and high-precision floating point support with low latency > Up to 99TOPs with INT8 and 23TFLOPs of FP32 compute bandwidth for signal processing > Code portability from previous generation devices |
| Adaptable Engines | <ul style="list-style-type: none"> > Fine-grained parallel processing for higher compute capacity and less routing utilization > Up to 123TB/s of programmable memory hierarchy for optimal compute efficiency > Dynamic Function eXchange (DFX) to swap functionality in milliseconds, reducing device cost and system power and enabling adaptability as algorithms evolve |
| Scalar Engines | <ul style="list-style-type: none"> > Dual-core Arm® Cortex®-A72 application processing unit for Linux-class operating systems > Dual-core Arm Cortex-R5F real-time processing unit with low latency and determinism > Platform management for quick boot, power and thermal management, and safety and security enclave |
| Programmable Network on Chip | <ul style="list-style-type: none"> > Terabits of dedicated bandwidth for guaranteed QoS with flexible bit-widths and no logic routing consumption > Software programmable framework with memory-mapped access to all resources > Easy IP and kernel placement with hardened connectivity to DDR, PCIe, and peripherals |
| NRZ and PAM4 Transceivers | <ul style="list-style-type: none"> > Up to 9Tb/s of serial bandwidth to support more antennas or testers without I/O bottlenecks > 32G NRZ transceivers for mainstream power-optimized 100G interfaces > 58G/112 PAM4 transceivers for the latest protocols and maximized bandwidth density |
| Integrated 100G Multirate and 600G Ethernet Cores | <ul style="list-style-type: none"> > Up to 5Tb/s of flexible Ethernet connectivity enabled by hardened 100G/600G cores > Multirate: Bidirectional 400/200/100/50/40/25/10G with FEC > Multi-standard: FlexE, Flex-O, eCPRI, FCoE, OTN |
| 400G High-Speed Cryptography Engines | <ul style="list-style-type: none"> > Up to 1.6Tb/s of line rate encryption throughput for secure networking > Bulk encryption: AES-GCM-256/128, MACsec, IPsec > Channelized rates from 40x10G to 1x400G per engine |
| PCIe® Gen5 with DMA and CCIX | <ul style="list-style-type: none"> > Symmetric/asymmetric access to memory with cache coherent interconnect for accelerators > Efficient communication to backend processing systems or test analyzers |
| Integrated 600G Interlaken Cores with FEC | <ul style="list-style-type: none"> > Scalable chip-to-chip interconnect from 10Gb/s to 600Gb/s > Integrated RS-FEC for power-optimized error correction |

TAKE THE NEXT STEP

For more information about the Versal Premium series, visit <https://www.xilinx.com/versal-premium>.

DISCLAIMERS

The information contained herein is for informational purposes only and is subject to change without notice. While every precaution has been taken in the preparation of this document, it may contain technical inaccuracies, omissions and typographical errors, and AMD is under no obligation to update or otherwise correct this information. Advanced Micro Devices, Inc. makes no representations or warranties with respect to the accuracy or completeness of the contents of this document, and assumes no liability of any kind, including the implied warranties of noninfringement, merchantability or fitness for purposes, with respect to the operation or use of AMD hardware, software or other products described herein. No license, including implied or arising by estoppel, to any intellectual property rights is granted by this document. Terms and limitations applicable to the purchase or use of AMD's products are as set forth in a signed agreement between the parties or in AMD's Standard Terms and Conditions of Sale.

COPYRIGHT NOTICE

© 2023 Advanced Micro Devices, Inc. All rights reserved. Xilinx, the Xilinx logo, AMD, the AMD Arrow logo, Alveo, Artix, Kintex, Kria, Spartan, Versal, Vitis, Virtex, Vivado, Zynq, and other designated brands included herein are trademarks of Advanced Micro Devices, Inc. Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies. AMBA, AMBA Designer, ARM, ARM1176JZ-S, CoreSight, Cortex, and PrimeCell are trademarks of ARM in the EU and other countries. PCIe, and PCI Express are trademarks of PCI-SIG and used under license. PID# 231846771-H

