SOLUTION BRIEF

Functional Safety Solution Brief

INTRODUCTION

AMD's comprehensive functional safety design flow simplifies and accelerates safety certifications supporting IEC 61508, ISO 13849 and ISO 26262. Together with unique architecture of adaptive SoC, functionally safe implementations at the smallest size are possible.

Artificial Intelligence (AI) requires compliance to Safety standards to guarantee predictable behavior for autonomous decision-making. AMD's SoCs have a rich history supporting the markets Industrial Automation, Automotive, Medical, Aerospace and Defense with safe products. Advantages are:

- High performance computing with acceleration in programmable logic
- On-chip heterogenous hardware redundancy with Arm Cortex A9/A53, Cortex R5 and MicroBlaze RISC softcore processors
- OTA Silicon - Updates are possible throughout the entire lifecycle
- Integration of complex and complete systems into a single device
- Long-term availability and extended temperature support

Adaptive SoCs, designed with safety in mind, are developed to meet established standards for safety and reliability requirements. AMD co-operates with leading test institutes to assess adaptive FPGAs and SoCs, design flows and tool architectures. Certificates are available for all parts of applicable design flows. AMD supports:

- Certifiable design flow to detect and avoid systematic failures
- Monitoring of the system at runtime to detect random failures
- Monitoring of the system at runtime to detect common cause failures
- Action on detected failures and transition into a safe state

AMD ZYNQ — PROVEN TECHNOLOGY

AMD Vivado — CERTIFIED DESIGN FLOW

COMPLETE SET OF IP AND TOOLS

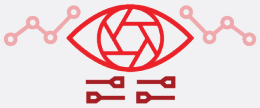
AMD Complete Functional Safety Design Concept

INDUSTRIAL AND HEALTHCARE IOT SOLUTIONS STACK

APPLICATION

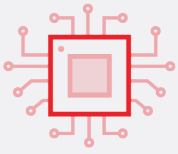
EDGE AI

EMBEDDED SW
FOR MIXED CRITICALITY



ANY-TO ANY CONNECTIVITY
SMARTER CONTROL
EMBEDDED VISION

FUNCTIONAL SAFETY
& CYBERSECURITY



SILICON ARCHITECTURE

SAFETY STANDARDS

Leading test institutes assessed and certified Design Tools for following standards:

- Vivado™ Design Suite for all releases from 2015.2 to 2021.2 by TÜV Süd
  - IEC 61508-3:2010
  - ISO 26262-8:2011
- Tool Chain of Vitis Core Development Kit for releases from 2019.2 to 2021.2 by TÜV Süd
  - IEC 61508-3:2010
  - ISO 26262-8:2011
- ISE for release 14.7 by TÜV Süd IEC 61508-3:2010
  - ISO 26262-8:2011
- MicroBlaze Compiler (GNU Compiler) for all releases from 2015.2 to 2021.2 by SGS TÜV Saar
  - IEC 61508:2010 up to SIL 4 class, T3 tool
  - ISO 26262:2011 up to ASIL D, TCL1
- Zynq UltraScale+ MPSoC for Device Architecture and Safety Manual by Exida
  - IEC 61508:2010 part 1, 2 and 3 up to SIL 3 with HFT=1
  - ISO 26262:2011 parts 2,4,5,6,7,8,9 and 10 up to ASIL C

AMD SAFETY DESIGN SOLUTION

AMD's comprehensive functional safety design flow solution for FPGA and Adaptive SoCs includes:

- Certificates and related reports for development and validation tool flows and methods
- Safety Manuals
- Software Safety User Guides (only for SoCs)
- ISO 13849 Technical Report for designs up to PLe and CAT 4 from TÜV Süd
- Reliability Reports and FIT rate calculator
- Triple Modular Redundancy and two core Lockstep with MicroBlaze Softcore RISC Processor

AMD's certified tool flows and devices

- Functional blocks to detect and correct errors in netlist (Single Event Upsets) and identification of "essential bits" in a device configuration Software test libraries (STLs) for Zynq Ultrascale+ MPSoC
- Web-based FMEDA tool and FMEDA calculation examples
- Application Notes and scripts to calculate base failure rates
- Built-in system monitors in AMD FPGAs and adaptive SoCs devices
- Application Notes for Isolation Design Flow for the separation of safe and non-safe functions

ANNUAL FUNCTIONAL SAFETY WORKING GROUP

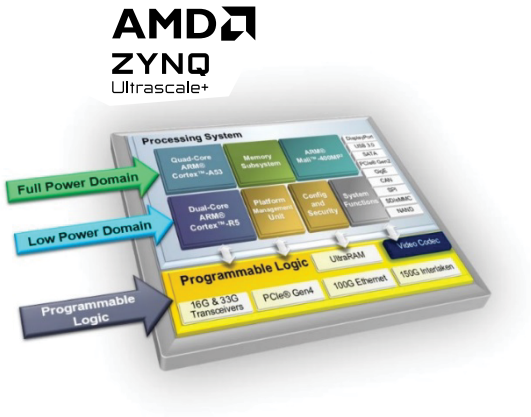
Meet AMD's safety architects and systems engineers at our annual Functional Safety Working Group meetings. Dates and places of the events are announced on the website for AMD Functional Safety (https://www.xilinx.com/products/technology/functional-safety.html, click on tab "Functional Safety Working Group" for event details).

INNOVATIVE DEVICE ARCHITECTURE FOR FUNCTIONAL SAFETY

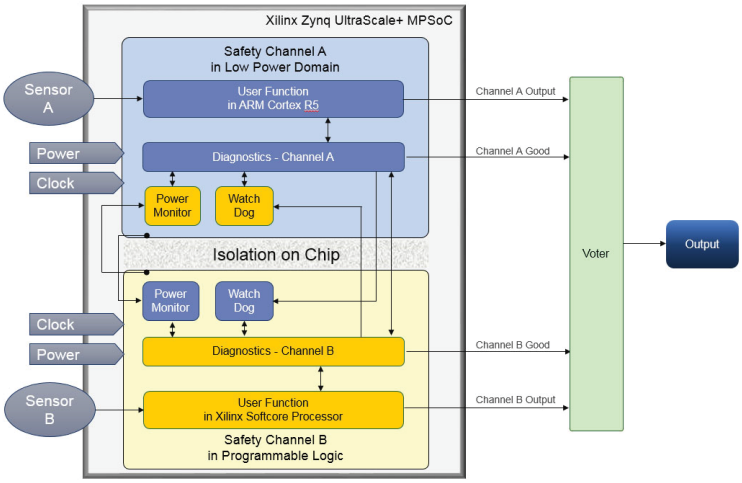
Zynq™ UltraScale+ MPSoC is designed to be Functional Safety certifiable.
That results in a versatile System-on-Chip which fits ideally in modern Safety Concepts.

Essential Characteristics

- Three separated chip domains with independent power supply and clocks to achieve HFT≥1
  - Low Power Domain
  - Full Power Domain
  - Programmable Logic Domain
- Low FIT
  - Reliable and power-saving 16 nm FinFET technology
- Protection for safety-critical elements
  - Triple Modular Redundant Boot, Safety & Error Management processors
  - Split mode and Lockstep mode for Arm Cortex R5
- ECC on all critical memories
- Hardened Memory Protection Units and Periphery Protection Units
- Configuration and Security Unit with triple modular redundancy
- System monitors for Common Cause Failure detection:
  - Voltage - Temperature - Clocks
- Testable Architecture
  - Logic BIST - Memory BIST - Error injection - Software Test Libraries



AMD's Zynq UltraScale+ MPSoC Overview



On-chip heterogenous hardware redundancy with Zynq UltraScale+ MPSoC

FUNCTIONAL SAFETY PACKAGE

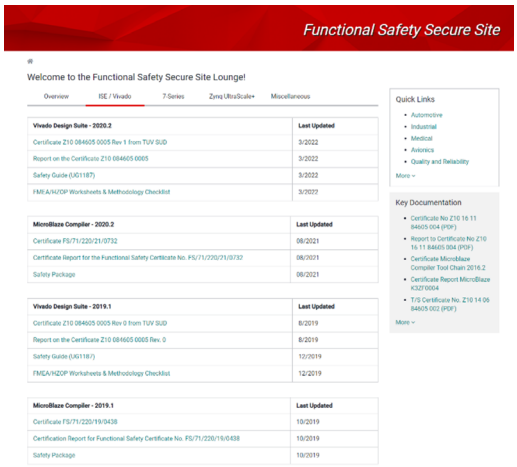
The Functional Safety Package gives you access to the entire Safety documentation and all tools. A web-based Functional Safety Lounge which is exclusive to subscribers provides access to latest information.

LICENSING AND ORDERING INFORMATION

The Functional Safety Package can be purchased with the order code **EM-DI-SAFETY-SITE**. That gives full access to the functional safety solutions as well as real time updates for one year.

Extensions of existing licenses are offered at 75% discount with order code **EMR-DI-SAFETY-SITE**.

For more detailed discussions about the Functional Safety design flow solution, please contact your local AMD sales representative.



AMD's web-based Functional Safety Lounge

CONCLUSION

Zynq UltraScale+ MPSoC was designed with safety and security in mind and is the ideal architecture to support industrial IoT platforms and future generations of automotive, aviation, and AI-based systems.

With the innovative Zynq UltraScale+ MPSoC architecture in combination with the recent IEC 61508 safety certification of the supporting Vivado Design Suite by TÜV Süd and the MicroBlaze™ compiler for additional soft processors by SGS-TÜV Saar, Xilinx now provides a complete ecosystem based on robust design flows that includes supporting documentation, assessment reports, and IP to minimize risks for customers.

Developers can retrieve tools and resources to support highly integrated safety-critical systems design by purchasing access to AMD's online Functional Safety Lounge. Privileges include access to the Safety Manual for Zynq UltraScale+ MPSoC, device and architecture updates, tool-flows and documentation including future reports and assessments.

To learn more, visit https://www.xilinx.com/applications/industrial/functional-safety.html