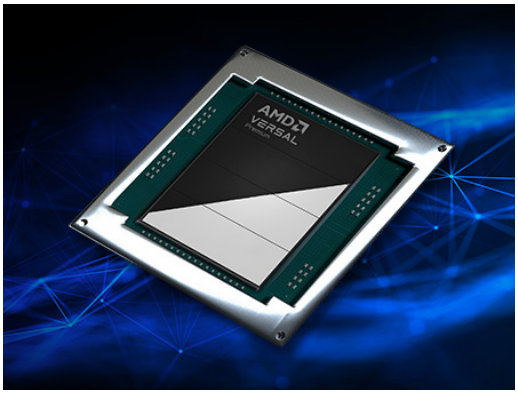
SOLUTION BRIEF

Network Accelerator with Versal™ Premium Series

> Hardened infrastructure for greater power efficiency than competing FPGAs
> Dynamically adapts for diverse workloads with custom datapaths
> Complete network acceleration platform programmed in HLS or RTL

CHALLENGE

The growth of data and compute complexity in data centers and cloud service providers has made it critically important to develop and integrate hardware accelerators to offload a broad range of applications from host CPUs. As network port speed and packet processing rates are overwhelming servers, additional packet processing and computational resources are required to have server CPU resources for other tasks. A new class of hardware accelerators has emerged to help offload CPU-intensive application processing to build a more scalable, low-latency processing pipeline.



SOLUTION: VERSAL PREMIUM SERIES FOR NETWORK ACCELERATION

AMD network accelerators revolutionize the effective use of the CPU by providing composable and extensible dataplane programmability while offloading compute-extensive network processes such as IPsec and NVMeoF. Versal™ Premium series provide fundamental NIC functions as hard IP and deliver exceptional compute density to offload a wide range of workloads from network to compute to storage at low power to meet the PCIe® form factor requirements in many data centers and cloud environments.

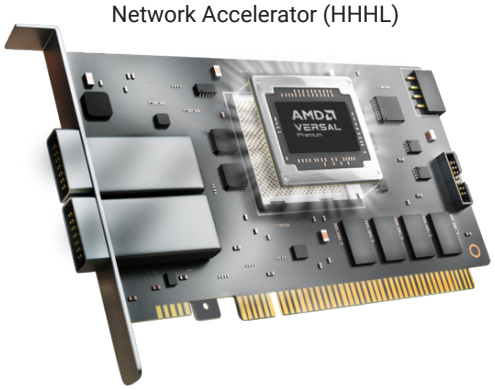
Hardened Infrastructure for Superior Performance/Watt

Versal Premium devices feature networked, power-optimized cores including Ethernet cores, High-Speed Crypto Engines, integrated PCIe Gen5 with hardened DMA, a programmable network on chip (NoC), and DDR memory controllers. These key hard IP deliver power-efficient NIC functionality and have more device resources for hardware differentiation, such as inline machine learning and custom packet processing functions.

30%

Less Power[1]

Versal Premium for 2x100G Network Accelerator (HHHL)



Dynamically Adapts for Diverse Workloads with Custom Datapaths

Equipped with a rich set of multicore, heterogeneous compute engines, Versal Premium devices offer unmatched composability to support new protocols, custom offloads, and application-specific datapaths. Software programmable hardware architecture with dynamic function exchange (DFx) allows users to swap compute kernels in milliseconds to provision network accelerators with streamlined orchestration for the most efficient use of cloud infrastructure.

Complete Network Acceleration Platform Programmed in HLS or RTL

Co-optimized for Vivado™ Design Suite and Vitis™ unified software platform, Versal Premium series provide a comprehensive suite of acceleration solutions to enable full custom RTL design, program abstractions such as HLS, and compute acceleration frameworks to enable both AMD and 3rd party applications.

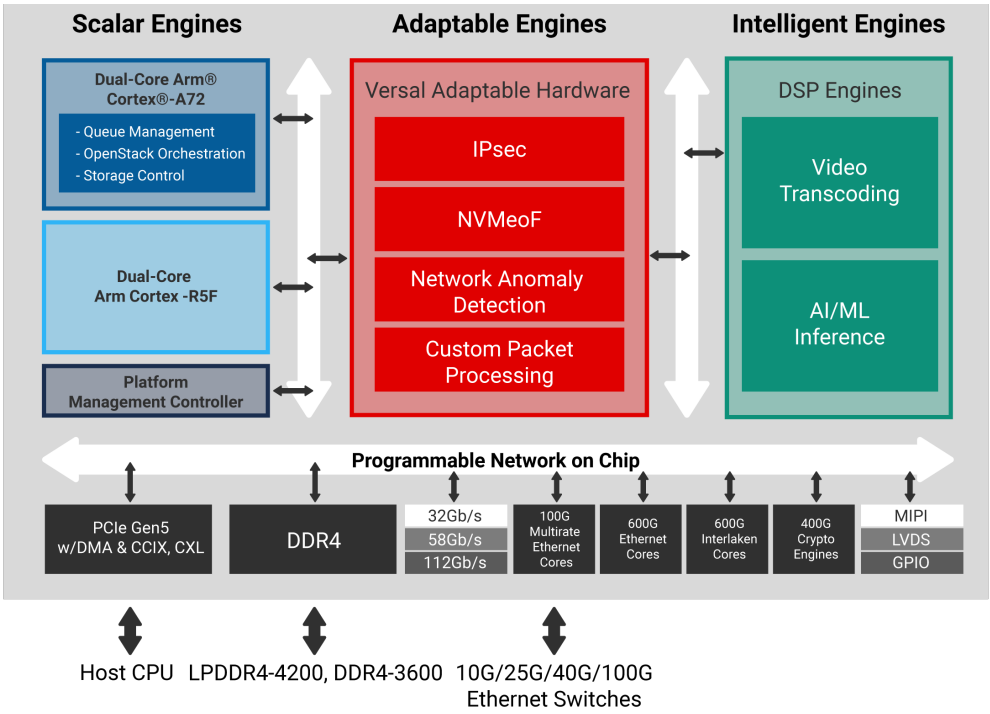
1: Versal Premium VP1202 vs. Intel Agilex AGF027 FPGA for 2x100G Network Accelerator

VERSAL ADAPTIVE SOC IMPLEMENTATION

2X100G Network Accelerator in a 75W PCIe Form Factor

A Versal Premium series implementation provides heterogeneous engines for optimal acceleration, a hardened shell for power-optimized fundamental infrastructure for network processing, hardware adaptability for composable dataplane programmability, and a form factor ideal for data center deployment.

VERSAL PREMIUM SERIES



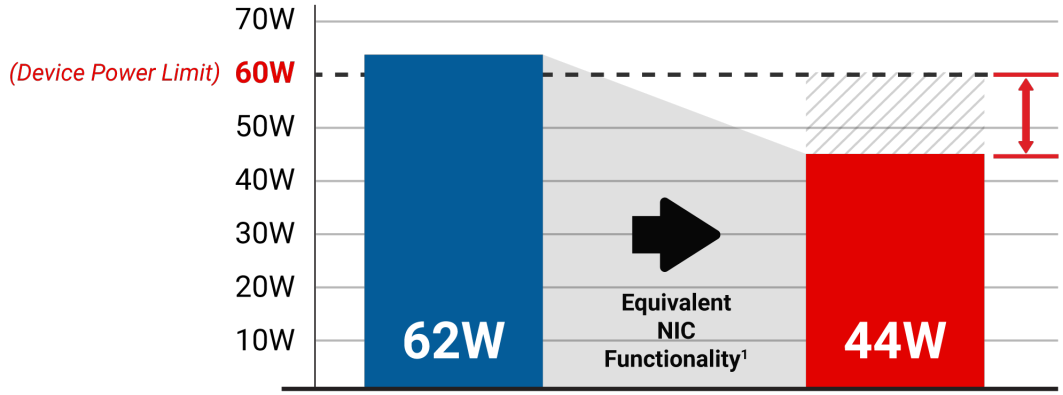
PLATFORM HIGHLIGHTS	
Adaptable Engines	> Adaptable to offload regularly changing workloads across a broad set of applications including inline machine learning, video transcoding, hashing for blockchains, custom packet processing, and more > Enable network traffic filtering, overlay network processing, and custom datapath features with low latency
Intelligent (DSP) Engines	> Variable fixed- and floating-point DSP compute with up to 1GHz performance > Ideal for video transcoding and AI / ML inference workloads
Scalar Engines	> Arm processing subsystem for queue management, OpenStack orchestration, and storage controller > Platform management controller for security, power management, and bitstream management
Programmable Network on Chip	> Seamless on-chip data movement for all engines and key interfaces > Simplifies kernel and IP placement, reducing soft logic needed for connectivity > Streamlines programming experience for software and hardware developers
Integrated Shell	> Hardened host interface (PCIe Gen5 w/DMA, DDR4 controllers), interconnected by programmable NoC > Ensures streamlined device bring-up and connectivity to off-chip interfaces–making the platform available at boot > Delivers pre-engineered timing closure and logic resource savings
Multirate Ethernet MAC and Transceivers	> Supports the latest optical and electrical communication standards while preserving existing infrastructure > Scalable and robust serial bandwidth for high-speed networking connectivity

BENCHMARK

75W Form Factor Network Accelerator

Shown below is a comparison of estimated power consumption of a Versal Premium device vs. a competing 10nm Agilex FPGA for a network accelerator application in an HHHL PCIe form factor and 75W power envelope. The Versal architecture's hardened infrastructure enables a power-optimized implementation with 16W power headroom for additional hardware differentiation. In contrast, the competing Intel Agilex FPGA exceeds the device power delivery limit. Hardened IP leveraged by Versal Premium adaptive SoCs include the integrated shell—comprising the programmable NoC, integrated PCIe Gen5 with integrated DMA, and DDR4 controllers–delivering programmable logic savings of 200K LUTs, as well as High-Speed Crypto Engines for security functions.

DEVICE POWER CONSUMPTION



16W of headroom for additional functionality

- In-line machine learning
- Hashing for blockchains
- Video transcoding
- Electronic trading
- Network traffic filtering
- Custom packet processing
- Other hardware differentation

	Intel Agilex AGF027		Versal Premium VP1202
Crypto	Insufficient Logic Capacity	Hard IP	No LUTs required[1]
PCIe DMA Engine	80K ALMs	Hard IP	No LUTs required[2]
Memory Interconnect	20k ALMs	Hard IP	No LUTs required[3]
Total Power	**62 Watts[4]**	**30% Less**	**44 Watts**

1: Versal adaptive SoCs feature hardened full-duplex 400G High-Speed Crypto Engines

2: Versal Premium Versal adaptive SoCs provide fully hardened PCIe Gen4/5 and DMA IP; Intel Agilex FPGAs provide PCIe Gen4 with soft DMA implementation only

3: The Versal adaptive SoCs NoC provides hardened connectivity for memory subsystem

4: Quartus Power & Thermal Calculator 21.2 for Intel Agilex FPGA power calculation, includes SmartVID claimed static power savings

TAKE THE NEXT STEP

> To learn more about the breakthrough integration of Versal Premium series, watch the video

> To try the above benchmark yourself, visit www.xilinx.com/versal-performance-elevated

> For more information on the Versal Premium series, visit www.xilinx.com/versal-premium

> To apply to the Versal Premium Evaluation Kit Early Access Program, visit Contact Sales

Versal Premium Evaluation Kit
Contact Sales for Early Access

DISCLAIMERS

The information contained herein is for informational purposes only and is subject to change without notice. While every precaution has been taken in the preparation of this document, it may contain technical inaccuracies, omissions and typographical errors, and AMD is under no obligation to update or otherwise correct this information. Advanced Micro Devices, Inc. makes no representations or warranties with respect to the accuracy or completeness of the contents of this document, and assumes no liability of any kind, including the implied warranties of noninfringement, merchantability or fitness for purposes, with respect to the operation or use of AMD hardware, software or other products described herein. No license, including implied or arising by estoppel, to any intellectual property rights is granted by this document. Terms and limitations applicable to the purchase or use of AMD's products are as set forth in a signed agreement between the parties or in AMD's Standard Terms and Conditions of Sale.

COPYRIGHT NOTICE

© 2023 Advanced Micro Devices, Inc. All rights reserved. Xilinx, the Xilinx logo, AMD, the AMD Arrow logo, Alveo, Artix, Kintex, Kria, Spartan, Versal, Vitis, Virtex, Vivado, Zynq, and other designated brands included herein are trademarks of Advanced Micro Devices, Inc. Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies. AMBA, AMBA Designer, ARM, ARM1176JZ-S, CoreSight, Cortex, and PrimeCell are trademarks of ARM in the EU and other countries. PCIe, and PCI Express are trademarks of PCI-SIG and used under license.
PID# 1846750-C