

Assembly Challenges in Developing 3D IC Package with Ultra High Yield and High Reliability

Raghunandan Chaware, Ganesh Hariharan, Jeff Lin, Inderjit Singh, Glenn O'Rourke, Kenny Ng, S. Y. Pai
Xilinx Inc.
2100 Logic Drive, San Jose, CA 95124

Chien-Chen. Li, Zill Huang and S. K. Cheng
Taiwan Semiconductor Manufacturing Company, Ltd.
6, Creation Rd. 2, Hsinchu Science Park, Hsinchu, Taiwan 300-77

Abstract

As the size and complexity of the designs grows larger, Field Programmable Gate Array (FPGA) based design solutions are becoming more dominant in system designs due to their ability to offer higher logic capacity and more on chip resources. FPGA based design solutions that offer higher capacity and higher bandwidth with low latency and power can provide system level functionality similar to Application Specific Integrated Circuits (ASICs). Stacked die technology enables high bandwidth connectivity between the multiple die by providing significantly large number of connection via microbumps. This interposer based die stacking approach provides low power and latency, but also adds manufacturing complexity. Any assembly process technology is viable only if it is manufacturable with high yields. This paper discusses key challenges observed during manufacturing of 28nm 3DIC products with CoWoS™ (Chip-On-Wafer-On-Substrate) process.

During the initial product ramp stage, most of the failures observed were related to interposer level assembly process. Common failure modes were ubump opens, interposer metal line opens and shorts, interposer metal line shorts and TSV to C4 opens. Specific isolation patterns were developed to isolate the interconnect failure to single ubump. After identifying the ubump, the failure was verified with failure analysis. The failure was then mapped on the interposer wafer and analyzed for any inline process deviations. With such close loop feedback process, this problem was resolved quickly to provide very stable and high yielding interconnection process.

Another unique failure mode observed during assembly was transistor damage caused during 3DIC assembly. In order to identify the root cause and isolate the problem, different assembly process splits and process corner studies were performed. A C4 probe card was designed to provide an intermediate test point at a major process loop after wafer level die assembly and before flip chip assembly of the stacked die on the organic package. The results of the intermediate probing suggested that multiple process steps could be contributing to this type of failure mode. Failure isolation was performed by post processing of final test data. With specialized isolation patterns, the failure locations were mapped on the interposer wafers and the FPGA wafer. Results suggested that wafer fab process changes did not have an impact on the failure mode and transistor defects were introduced during integration and assembly of FPGA die on the interposer wafer. Series of assembly improvements implemented in the assembly process will be discussed in the paper.

The process improvement qualification was completed by subjecting the parts to temperature cycling and high temperature storage (HTS) tests. Extended temperature cycling tests were performed and the parts were subjected to Level 4 preconditioning followed by 1500 cycles of -55°C to 125°C temperature cycle condition. Evaluation units were also subjected to 4000 hours of HTS. All the parts successfully passed the extended reliability evaluations.

Introduction

In the fast changing world, where the need to quickly complete new designs to compete in market place is driving this critical need to deliver more with minimum changes to the first design and quickly create a product that provides differentiated features. This fast pace, agile development environment has created a programmable imperative, which is to create differentiated products with programmable design platforms. Programmable FPGA based products can offer high capacity, lower power and higher bandwidth with added benefit of programmability and shorter time to market compared to Application Specific Integrated Circuits (ASICs) and Application Specific Standard Products (ASSPs).

In order to run a complex design, most of the times two or more FPGAs are needed to be connected together to create a larger virtual FPGA. Packaging technology is one of the key factors to the I/O limitation. However, even with advancements in the package technology over the years, the latest packaging technology than can only offer approximately 1,200 I/O pins, significantly lower than the actual number of I/Os required. Traditional packaging technology, such as Multi-Chip Module (MCM) is inadequate to deliver an optimal solution because of limitations related to no of I/Os, latency, power consumption and signal integrity [1].

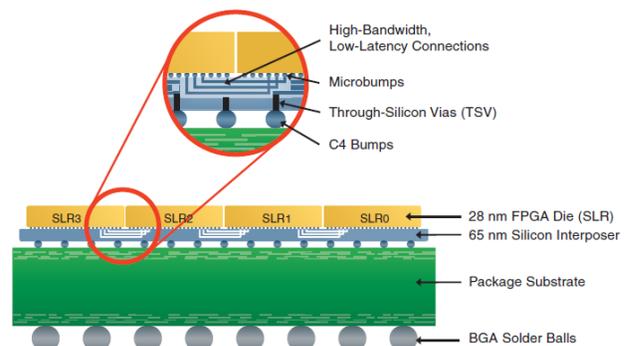


Figure 1. Schematic X-section of Virtex®-7 2000T FPGA Assembled with Interposer with TSVs

To overcome these limitations, Xilinx employed interposer with through silicon vias (TSVs) to stack FPGA die side by side to each other. Figure 1 shows the schematic cross-section of the Virtex®-7 2000T FPGA. This method provides high-bandwidth connectivity between multiple die by providing thousands of inter-die connections. This approach significantly reduces power consumption (80% reduction compared to MCMs or multiple FPGA solution) and provides very low latency, while allowing connectivity to large amount of interconnect logic, transceivers, and on-chip resources within a single package. [1]

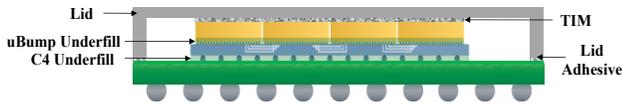


Figure 2. Virtex®-7 2000T FPGA Assembled Package Construction

Table 1. Materials Used in Stacked Die Package

Package Construction	Material Set
Lid	Standard (Cu – Ni Plating)
TIM	Standard
uBump	Lead Free (Cu Pillar)
uBump Underfill	Capillary UF
C4 Bump	Eutectic
C4 Underfill	Capillary UF
Package Substrate	Standard Build Up

Figure 2 and Table 1 show the schematic package construction. The package uses standard sets of assembly materials widely used in flip chip assembly process, offering a low risk assembly solution for such an advanced package. Even though the FPGA die and interposer are made from silicon, a capillary underfill is used between the FPGA die and silicon interposer to reduce the stress induced in the ubump during assembly process. The FPGA and interposer stack is then assembled on to the package and a capillary C4 underfill is used to couple the two. After underfill cure process, a standard lid is attached to the die and package and package with the use of thermal interface material and lid adhesive.

Assembly Process

The production process utilizes TSMC’s Chip on Wafer on Substrate (CoWoS™) assembly technique. A simplified assembly flow is described in Figure 3. FPGA die is sorted for known good die (KGD) and ubump process is completed. The known good die are then diced and prepared for assembly. The interposer with TSV is also tested during fabrication process to ensure there are no systematic defects created during fabrication process. Interposer wafer is then ubumped and kept ready for top die assembly. FPGA dies are assembled on the interposer by reflow process. After interposer and top die assembly, fine filler ubump underfill is dispensed at the edge of each FPGA die. After ubump underfill cure, FPGA and interposer stack goes through TSV reveal process where backside of the interposer is polished to expose TSVs.

After TSV reveal process, C4 ubumps are created to connect FPGA stack through the interposer to a package. The wafer then goes through dicing process where individual stacked dies are created. These stacked die modules are attached on to organic substrates and joint together using standard mass reflow process. Reflow process is followed by C4 underfill dispense and underfill cure steps. In the end, lid or heat spreader is attached to die and the package and BGA balls attached to BGA pads on the substrate. Packages are then subjected to final test to sort out the good units. [2]

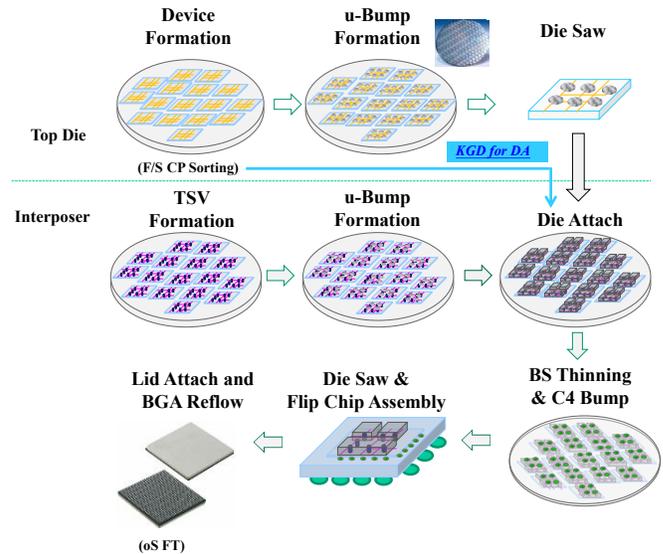


Figure 3. Simplified Package Assembly Process Flow

Assembly Challenges and Yield Improvement

As described in Figure 3, stacked die assembly process involves many additional steps related to wafer level assembly process. Very similar to the flip chip assembly process, interposer open and shorts were the most common defects related to top die and interposer. Interposer fabrication process has become very mature and issues related copper via fill were encountered in the production. The interface between the TSV and C4 bump can have defects due to depth variation in the blind TSVs. This type of defect will be discussed in this section.

Interposer Opens and Shorts

Most of the defects that caused interposer open failures were result of inline defects that were not caught during inline inspection or during the interposer test. Since multiple FPGA die are interconnected through the interposer, the interconnection lines that connect two adjacent FPGA die are very difficult to test electrically. So, to minimize yield loss, it is extremely important to catch the defects during inline inspection. In order to establish the correct defect codes, an iterative continuous improvement process is required. In this case, during the early phase of production, a significant amount of effort was made to do failure analysis on a number of units that had failed for interposer open and shorts. The data from the failures was utilized to improve defects scans and improve the yields in the subsequent lots.

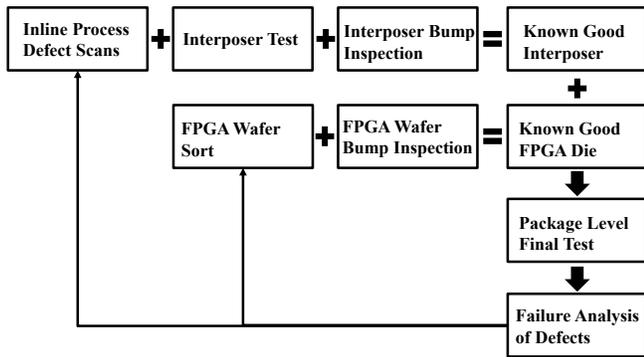


Figure 4. Continuous Yield Improvement Process Flow

In order to quickly isolate the interposer opens and shorts, a specific diagnostic test with a special test pattern was developed. The test output data collected from this test pattern can be post processed to provide exact coordinates of the failure. This allowed us to reduce the failure analysis turnaround time. This test pattern is similar to an EXTEST performed during printed circuit board interconnection test, but in this case it is done on an interposer.

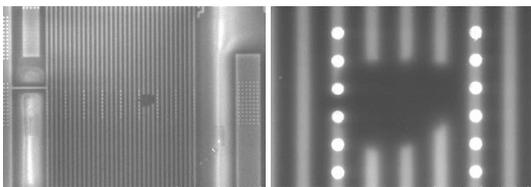


Figure 5(a). An Example of Interconnect Line Defect

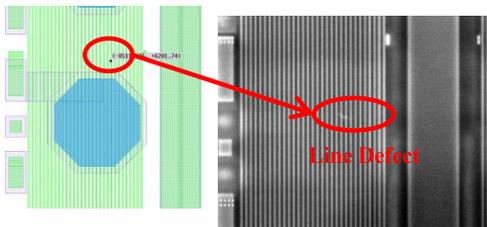


Figure 5(b). An Example of An Interconnect Line Defect

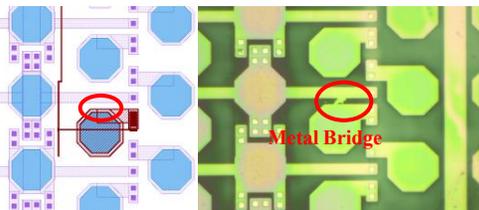


Figure 5(c). An Example of Metal Bridge in RDL Layer

Interposer opens can also be caused by ubump related failures. uBump opens are usually caused by defective ubump or due to particle defects. Failure analysis performed on all the ubump open failures was not conclusive due to presence of underfill material in the vicinity. It is believed that some type of particle defect or contaminant affected the solder joint formation during reflow. This type of defect was relatively easy to process as the defect could be quickly detected using a 3D X-

ray technique. An example of a malformed bump is shown in Figure 6.

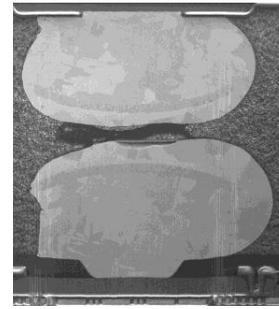


Figure 6. Example of uBump Open Caused by Contamination

Another interface that is critical to the overall yield and reliability is the interface between the TSV and C4 pad. All the TSVs need to be exposed completely to ensure good adhesion and bond formation between the C4 bump under bump metallization (UBM) and TSV. During early production, it was observed that an interposer open failure could be caused by insufficient removal of TSV liner. An example of such defect is shown in Figure 7. All such defects were observed at the wafer edge. This type of defect was completely eliminated by optimizing the backside grinding process. Wafer warpage variation has to be taken into consideration when setting the optimal parameters for wafer grinding and chemical mechanical polish (CMP).

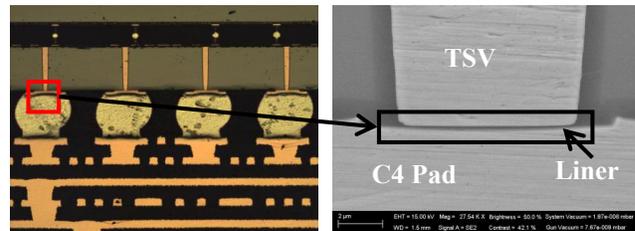


Figure 7. TSV to C4 Bump Pad Open

In the existing process, as the FPGA dies are assembled on the interposer at the start of the assembly, the stacked die assembly goes through significant number of the process steps before final package completion. In the early stages of production, significant number of tests and diagnostic patterns were developed to isolate the failures. One of the new failure modes seen in the early stage of the production was the transistor damage. As shown in Figure 4 earlier, all the FPGA die were fully tested for defects before assembly and this type of defect was not expected to be observed after assembly. This type of failure is quite different compared to standard flip chip assembly. Figure 8 shows an example with transistor OD damage. Possibility of electrostatic discharge (ESD) causing damage to the active area has been discussed earlier. Some of the critical steps, such as pick and place of top die on to an interposer or wafer thinning and TSV exposure can introduce transistor level defects due to ESD. Therefore, the whole process flow was carefully studied. [3]

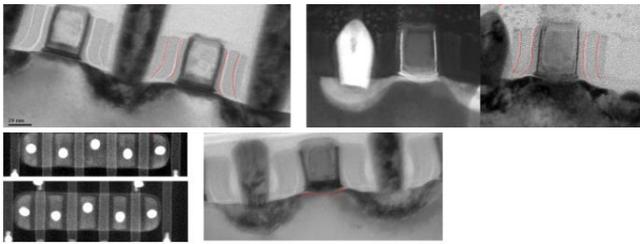


Figure 8. Transistor Level Defect Observed After Stacked Die Assembly

After assembly of the known good FPGA die on the interposer wafer, the stacked assembly goes through various wafer level process steps. After singulation, the stacked die assembly also follows the standard flip chip assembly process where it is attached to the organic package or substrate. In order to isolate the source of the failure, an intermediate test point was introduced between wafer level process and substrate level assembly. A C4 probe card and simple test patterns similar to final test were developed. Figure 9 shows the test point insertion after C4 bumping process before flip chip assembly. Test data was recorded for each stack die assembly after C4 probing. This data was then compared with the final test data collected during package level test. The comparison suggested that there was no change in failure rate after C4 probing, indicating that the main failure was caused during wafer level assembly process.

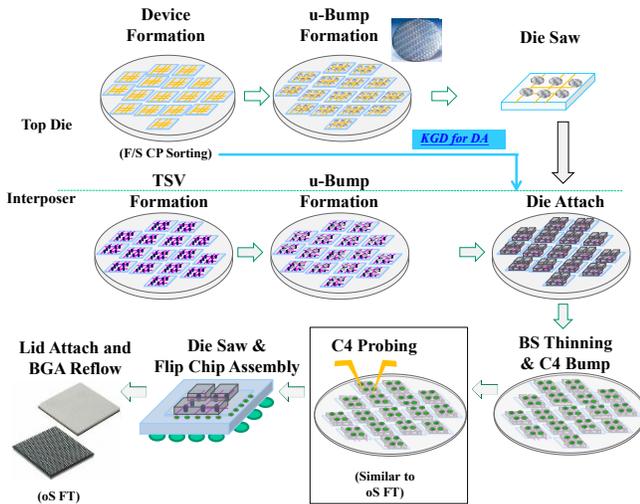


Figure 9. Process Flow with Additional C4 Probe Test Point

In order to eliminate this defect, experiments were focused on three key major factors, namely FPGA fabrication process, interposer design and stacked die assembly process. More than 35 different process splits were performed. A high level result summary is given in Table 2. The FPGA process or interposer design/process change did not show any improvement and the failure mode could not be eliminated with these changes. However, stacked die assembly process improvements had significant impact on the yield. After implementing all the improvements in the process, this defect was completely eliminated.

Table 2. Materials Used in Stacked Die Package

Factor	Yield Improvement
FPGA Fab Process	None
Interposer Design	None
Stacked Die Assembly Process	Highest Impact

Currently stacked die assembly production yield are very high, approaching equivalent monolithic (standard) flip chip assembly yields. Figure 10 shows failure Pareto (percentage of percentage failures) for some recent lots. Important point to note here is that the TSVs in the interposer are very robust and failure rate related to TSVs is almost negligible. With adequate process optimization, high interposer and stacked die assembly yields are possible. The major assembly defects are still related to open and shorts caused by C4 bump and interconnect failures. Other functional rejects are due to wafer fab related defects that are not caught during wafer sort. These defects will reduce further as the silicon node becomes more mature.

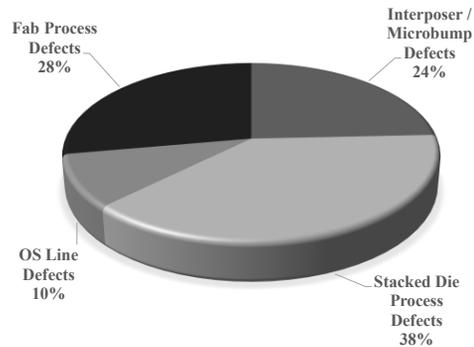
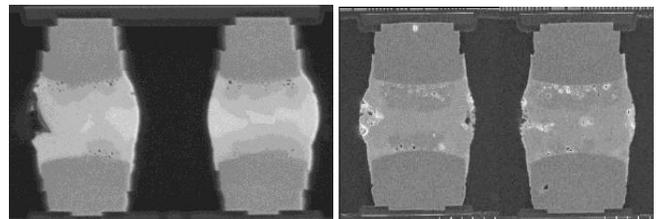


Figure 10. Failure Pareto (% of % Defects) for Assembly

Reliability Evaluations

Main focus of the reliability evaluations was to understand the impact of temperature on various critical components of the package such as microbumps, TSV, and adhesion of the underfill to top FPGA die and thin TSV interposer. Microbump reliability challenges have been discussed in various papers at length. In order to assess the long term reliability the parts were subjected high temperature storage test much longer than JEDEC guidelines. HTS tests were continued well beyond 1000 hrs and currently the HTS test has completed 5000 hrs. The parts were also subjected to L4 preconditioning and -55C to 125C thermal cycling. Similar to HTS tests, thermal cycling of the parts was continued to 1500 cycles beyond the JEDEC guideline.



(a) uBump after 1000 hrs. (b) uBump after 4000 hrs.

Figure 11. uBump Shape and Structure after HTS

Figure 11 shows the integrity of the ubump after 1000 hrs and 4000 hrs of HTS testing. All the ubumps maintained the shape and there was very minimal degradation after 1000 hrs of HTS. As seen the Figure 10(a) small amount of void formation was observed at the copper pillar and solder boundary due to intermetallic growth. Some ubumps exhibited uneven surface at the edges, which was probably result of the volumetric change caused by intermetallic formation. Extended hours of high temperature storage did not have any adverse impact on the integrity of the ubump. No major degradation was observed even after 4000 hrs of exposure. All the lots subjected to level 4 preconditioning and 1500 cycles of temperature cycles passed without any failures. Along with electrical test data, numerous mechanical cross-section were performed after completion of the temperature cycling evaluations to ensure that all the interfaces were intact after testing. No delamination or cracking was observed in critical interfaces such as ubumps, TSV side walls, TSV to C4 UBM interface etc. These test results demonstrated that the stacked die assembly process was very robust and had no long term reliability issues.

Conclusions

An overview of the various assembly related defects was provided in this paper. Most of the assembly related interconnect opens were related to interconnect line defects coming that result from fab process defects. These defects are very difficult to detect and a close loop continuous improvement cycle is required to improve the defect scan process. Similar to C4 bumps opens, ubump opens were observed during the assembly process. Most of these ubump opens were related to ubump contamination or ubump defects which were not captured during the interposer inspection. In very early stages of production, transistor level defect was observed after final test. In order to isolate the failure, C4 probe point was inserted in the process. The defect was caused during the stack die assembly process and interposer related wafer level processes. Numerous process splits for wafer fab process, interposer design, and stacked die assembly process were conducted. This defect was completely eliminated by optimizing the stacked die assembly process. Extended reliability tests, namely HTS and TCB, were performed to evaluate the package robustness. All units passed 4000 hrs of 150°C HTS test and no degradation in the ubump structure. All units also passed 1500 cycles of -55°C to 125°C temperature cycling tests without any failure. Production data and reliability evaluations show that interposer based stacked die assembly process is very robust and can achieve high yields very similar to standard flip chip process.

Acknowledgments

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