



Versal™ ACAP AI Core Series Product Selection Guide



Industry's First Adaptive Compute Acceleration Platform (ACAP)

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Versal™ AI Core Series – Resources

		VC1352	VC1502	VC1702	VC1802	VC1902	VC2602	VC2802
Intelligent Engines	AI Engines Tiles	128	198	304	300	400	0	0
	AI Engine-ML Tiles	0	0	0	0	0	152	304
	AI Engine Data Memory (Mb)	32	50	76	75	100	76	152
	AIE-ML Shared Memory (Mb)	0	0	0	0	0	304	304
	DSP Engines	928	1,032	1,312	1,600	1,968	984	1,312
Adaptable Engines	System Logic Cells (K)	540	815	981	1,586	1,968	820	1,139
	LUTs	246,784	372,352	448,512	725,000	899,840	375,000	520,704
	NoC Master / NoC Slave Ports	10	21	21	28	28	21	21
	Distributed RAM (Mb)	8	11	14	22	27	11	16
Memory	Total Block RAM (Mb)	16	30	34	28	34	17	21
	UltraRAM (Mb)	59	110	130	91	130	63	74
	Accelerator RAM (Mb)	32	0	0	0	0	0	0
	Total PL Memory (Mb)	115	151	178	141	191	91	111
	DDR Memory Controllers	2	3	3	4	4	3	3
	DDR Bus Width	128	192	192	256	256	192	192
Scalar Engines	Application Processing Unit	Dual-core Arm® Cortex®-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC						
	Real-time Processing Unit	Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC						
	Memory	256KB On-Chip Memory w/ECC						
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)						
Serial Transceivers	GTY Transceivers (32.75Gb/s)	0	32	44	44	44	0	0
	GTYP Transceivers (32.75Gb/s)	8	0	0	0	0	32 ⁽¹⁾	32 ⁽¹⁾
Integrated Protocol IP	CCIX & PCIe® w/DMA (CPM)	–	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	2 x Gen5x8, CCIX	2 x Gen5x8, CCIX
	PCI Express®	1 x Gen4x8	4 x Gen4x8	4 x Gen4x8	4 x Gen4x8	4 x Gen4x8	4 x Gen5x4	4 x Gen5x4
	100G Multirate Ethernet MAC	1	3	4	4	4	2	2
	Video Decoder Engines (VDEs)	–	–	–	–	–	2	4
	Platform Management Controller	Boot, Security, Safety, Monitoring, and High-Speed Debug						

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Notes:

1. 16 GTYP transceivers are dedicated to CPM5 for PCI Express use.

Versal™ AI Core Series – Packaging

			VC1352	VC1502	VC1702	VC1802	VC1902	VC2602	VC2802
Package	Package Dimensions (mm)	Ball Pitch (mm)	XPIO DDR Only, XPIO DDR+PL HDIO, MIO GTY, GTYP						
NBVA1024	31x31	0.92	168, 210 22, 78 0, 8						
NSVE1369	35x35	0.92	168, 210, 44, 78 0, 8						
NSVG1369	35x35	0.92		132, 246 22, 78 24, 0	132, 246 44, 78 24, 0				
NSVH1369	35x35	0.92						132, 192 44, 78 0, 32	132, 192 44, 78 0, 32
VSVA1596 ⁽¹⁾	37.5x37.5	0.92		132, 246 22, 78 32, 0	132, 246 44, 78 32, 0				
VIVA1596 ⁽¹⁾	40x40	0.92				132, 246 44, 78 32, 0	132, 246 44, 78 32, 0		
VSVD1760	40x40	0.92				186, 462 0, 78 24, 0	186, 462 0, 78 24, 0		
VFVH1760	40x40	0.92						186, 300 44, 78 0, 32	186, 300 44, 78 0, 32
VSVA2197	45x45	0.92		192, 294 22, 78 32, 0	192, 294 44, 78 44, 0	186, 462 44, 78 44, 0	186, 462 44, 78 44, 0		

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Notes:

1. Devices in VIVA1596 and VSVA1596 support peak LPDDR4 data rates in 324 I/O only. The remaining 54 I/O support limited data rates. See the associated data sheet.

Versal™ AI Core Series – Figures of Merit

			VC1352	VC1502	VC1702	VC1802	VC1902	VC2602	VC2802
Intelligent Engines	AI Engine Peak Perf – INT8x4	TOPs	43	83	101	100	133	202	405
	AI Engine Peak Perf – INT8	TOPs	43	83	101	100	133	101	202
	AI Engine Peak Perf – INT8x16	TOPs	21	41	51	50	67	51	101
	AI Engine Peak Perf – INT16	TOPs	11	21	25	25	33	25	51
	AI Engine Peak Perf – CINT16	Complex TOPs	3	5	6	6	8	3	6
	AI Engine Peak Perf – FP32	TFLOPs	3	5	6	6	8	8	17
	AI Engine Peak SRAM Bandwidth	Tb/s	170	330	405	399	532	202	405
	DSP Engine Peak Perf – INT8	TOPs	6.4	9.1	9.1	11.0	13.6	6.8	9.1
	DSP Engine Peak Perf – INT24	TOPs	2.1	3.0	3.0	3.7	4.5	2.3	3.0
	DSP Engine Peak Perf – CINT18	Complex TOPs	0.9	1.3	1.3	1.6	1.9	1.0	1.3
DSP Engine Peak Perf – FP32	TFLOPs	1.5	2.1	2.1	2.6	3.2	1.6	2.1	
Adaptable Engines	Adaptable Engine Peak Perf – INT1	TOPs	258	381	469	758	941	392	544
	Adaptable Engine Peak Perf – INT2	TOPs	118	175	215	347	431	180	250
	Adaptable Engine Peak Perf – INT4	TOPs	31	45	56	90	112	47	65
	Adaptable Engine Peak Perf – INT8	TOPs	8	12	14	23	29	12	17
Scalar Engines	Arm® Cortex-A72 Performance	DMIPs	19,516	19,516	19,516	19,516	19,516	19,516	19,516
	Arm Cortex-R5F Performance	DMIPs	2,505	2,505	2,505	2,505	2,505	2,505	2,505
Memory	Total Bandwidth - Block RAM	Tb/s	64	79	137	115	139	69	86
	Total Bandwidth - Ultra RAM	Tb/s	22	23	49	35	49	24	28
	Total Bandwidth - Accelerator RAM	Tb/s	0.4	0.0	0.0	0.0	0.0	0.0	0.0
	Total SRAM Bandwidth	Tb/s	86	102	186	150	188	92	114
I/O	Transceiver Bandwidth	Tb/s	0.52	1.44	2.88	2.88	2.88	2.10	2.10
	Sensor I/O Bandwidth	Gb/s	672	941	941	1,478	1,478	960	960
Platform Engines	DDR4 Memory Bandwidth	GB/s	51.2	51.2	76.8	102.4	102.4	76.8	76.8
	LPDDR4 Memory Bandwidth	GB/s	68.3	68.3	102.4	136.5	136.5	102.4	102.4
	NoC Cross-sectional Bandwidth	Tb/s	1.1	1.2	1.7	2.2	2.2	1.7	1.7

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Versal™ ACAP Ordering Information



Device Name			Device Attributes					Package Definition			
XC	V	C	1902	-1	M	S	E	V	S	V	D1760
Xilinx XC: Commercial XA: Automotive XQ: Defense	Architecture Versal	Series Name E: AI Edge C: AI Core M: Prime P: Premium H: HBM	Device Number Digits 1-3: Value Identifier Digit 4: # of Primary Cores	Speed Grade -1: Slowest -2: Mid -3: Highest	Voltage L: Low (0.7V) M: Mid (0.80V) H: High (0.88V)	Static Screen S: Standard L: Low Static	Temp Grade E: 0 to 110°C ⁽¹⁾ I: -40 to 110°C ⁽¹⁾ Q: -40 to +125°C M: -55 to +125°C	Ball Pitch V: 0.92mm, w/LSC N: 0.92mm, no LSC S: 0.8mm L: 1.0mm	Lid S: Lidless, w/Stiffener Ring F: Lidded B: Lidless, no Stiffener Ring H: Lidded Overhang I: Lidless, w/Stiffener Ring & Overhang	RoHS6 Code ⁽²⁾ V: Pb-free Ball Q: Eutectic Ball R: Ruggedized, Eutectic Ball	Footprint

Note:

1. Operation at 110°C Tj is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of device lifetime—except -1E and -3E (standard 0–100°C).
2. All packages have Pb-free bumps.