

Virtex UltraScale+ 58G PAM4 FPGA

- > Fastest transceiver in a programmable device
- > Enables scalable adoption of emerging optics and protocols
- > Doubles performance on legacy equipment

OVERVIEW

The Virtex® UltraScale+™ 58G PAM4 FPGA implements the latest 50G/100G/200G/400G optics and protocols with superior port density and performance-per-watt while minimizing system-level cost. It enables new and existing platforms to meet ever increasing demand for bandwidth.

Integrated 58G PAM4 transceiver technology provides flexible connectivity to backplanes, optical modules, and chip-to-chip interfaces. Further integration of KP4-FEC for 50 to 400G Ethernet, 100G Ethernet with KR4-FEC, 150G Interlaken, and up to 500Mb of on-chip RAM enables footprint and BOM cost reductions.

Users can double transmission rates on legacy 25G backplanes and extend ASIC lifetimes by using Virtex UltraScale+ 58G PAM4 FPGAs to bridge to the latest optics modules such as QSFP-DD. Logic and I/O resources are adaptable to evolving optics form factors and standards, enabling you to future-proof your system.

HIGHLIGHTS

Increased System Performance

- > 48 transceivers running up to 58Gb/s PAM4 for multi-terabit systems
- > 32 transceivers operating at 32.75Gb/s for 25G interoperability
- > 38 TOPs (22 TeraMACs) DSP compute performance
- > 2,666Mb/s DDR4 in the mid speed grade

Adaptable System Integration

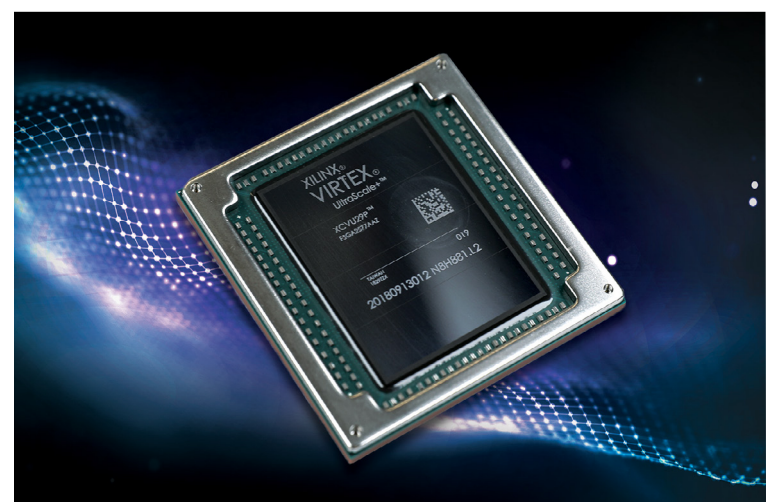
- > Integrated 100G Ethernet MAC with KR4-FEC and 150G Interlaken cores
- > Integrated blocks for PCI Express® Gen3 x16
- > Up to 3.8M system logic cells
- > Up to 500Mb of total on-chip integrated memory

BOM Cost Reduction

- > Eliminates discrete ICs for Ethernet, gearboxes, memory, and PCIe
- > VCXO and fractional PLL integration reduces clocking component cost

Total Power Reduction

- > Up to 50% lower system power vs. a 28G discrete gearbox solution
- > Voltage scaling options for performance and power
- > Tighter CLB packing reduces dynamic power



TARGET APPLICATIONS

- > Transport and Metro Networks
- > Routers and Switches
- > Network Test Equipment
- > Military Communications
- > Network Security/Firewalls

FEATURES

16nm low power FinFET+ process technology from TSMC	<ul style="list-style-type: none"> > Industry-leading process from the #1 service foundry delivers a step function increase in performance-per-watt > The same scalable architecture and tools as Virtex UltraScale™ FPGAs
Massive I/O bandwidth and dramatic latency reduction	<ul style="list-style-type: none"> > 28G and 58G backplane support > 32.75G and 58G chip-to-chip and chip-to-optics support > High-density I/O for smaller area and greater power efficiency per pin
Integrated 100G Ethernet MAC and 150G Interlaken Cores	<ul style="list-style-type: none"> > Saves 60K–100K system logic cells per port > Up to 90% dynamic power savings vs. soft implementation > KR4-FEC (Ethernet MAC) for optics error correction > KP4-FEC for PAM4 optics and backplanes
Integrated blocks for PCI Express	<ul style="list-style-type: none"> > Native Gen3x 16 Integrated PCIe block for 100G applications > Integrated MSI-X tables > Expanded virtualization for data center applications > Large number of tags to support more PCIe requests enabling overall system performance
UltraRAM for deep memory buffering	<ul style="list-style-type: none"> > Up to 360Mb on-chip UltraRAM for SRAM device integration > 8X capacity-per-block vs. traditional embedded memory > Deep-sleep power modes
Enhanced DSP slices for diverse applications	<ul style="list-style-type: none"> > Up to 22 TeraMACs (38 TOPs) of DSP compute bandwidth > Double-precision floating point using 30% fewer resources > Complex fixed-point arithmetic in half the resources
Massive memory interface bandwidth	<ul style="list-style-type: none"> > DDR4 support of up to 2,666Mb/s > Support for server-class DIMMs (8X capacity vs. Virtex-7 FPGAs) > Support for DDR3, DDR3L, QDR-IV, and LPDDR3 memory types
UltraScale enhanced clocking and routing	<ul style="list-style-type: none"> > Lower skew, faster performing clock networks > Up to one speed grade advantage vs. comparable solutions > Efficient CLB use and placement for reduced interconnect delay

TAKE THE NEXT STEP

For more information about Xilinx Virtex UltraScale+ 58G PAM4 FPGAs, go to www.xilinx.com/virtex-ultrascale-plus-58g.

Virtex UltraScale+ 58G PAM4 FPGAs are supported by comprehensive developments tools, reference designs, an IP catalog, and evaluation platforms. Visit [Virtex UltraScale+ FPGA VCU129 evaluation kit](#) page to start evaluating the latest Virtex UltraScale+ 58G PAM4 FPGAs.

Start by contacting your [Xilinx Sales Representative](#) to arrange an on-premises transceiver performance evaluation.

Corporate Headquarters

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
USA
Tel: 408-559-7778
www.xilinx.com

Xilinx Europe

One Logic Drive
Citywest Business Campus
Saggart, County Dublin
Ireland
Tel: +353-1-464-0311
www.xilinx.com

Japan

Xilinx K.K.
Art Village Osaki Central Tower 4F
1-2-2 Osaki, Shinagawa-ku
Tokyo 141-0032 Japan
Tel: +81-3-6744-7777
japan.xilinx.com

Asia Pacific Pte. Ltd.

Xilinx, Asia Pacific
5 Changi Business Park
Singapore 486040
Tel: +65-6407-3000
www.xilinx.com

India

Meenakshi Tech Park
Block A, B, C, 8th & 13th floors,
Meenakshi Tech Park, Survey No. 39
Gachibowli(V), Seri Lingampally (M),
Hyderabad -500 084
Tel: +91-40-6721-4747
www.xilinx.com

