



# Tips and Tricks for IP Integrator

Presented By

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Interaction Design  
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# The Evolution of IP Integrator

**2013 - IPI**  
IP Integrator debut – replaces XPS

**2015 - HLx**  
Vivado HLx Methodology – IP Integrator for shell  
SDx / HLS for differentiation

**Next – ACAP**  
Versal ACAP debut – IP Integrator enables H/W shell with Versal heterogeneous features  
IP Integrator improves WYSIWYG RTL

# What You'll See in this Presentation



## > Technical, demo centric, methodology tips presentation

- >> Helpful today
- >> Needed for tomorrow

## > We'll see, using a real-world design

- >> Features of IP Integrator to rapidly build designs with complex IP
- >> New Ease-of-Use features (Find, Pinning)
- >> New Design Migration capabilities
- >> New Design Differencing

# Most Common Requests for IP Integrator

## > Ease-of-Use

- >> Finding IP, Freezing IP
- >> Example Designs in IP Integrator

## > Migration Hurdles

- >> Selectively updating IP
- >> Migrating to next generation devices

## > Team Based Design

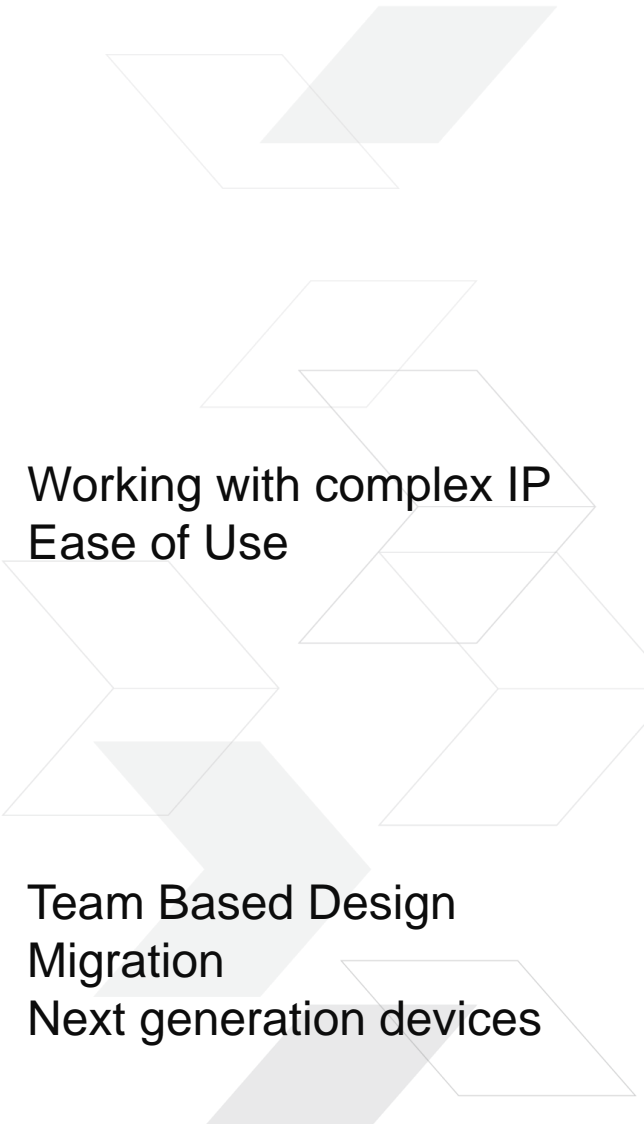
- >> Enable teams to work in tandem (Spring 2019)
- >> Visualize differences between Block Diagrams



# Visual Walkthrough

## > Start to End

1. Creating a new design for the KCU105
2. Creating an example design for HDMI
3. Using Find and hierarchical partitioning
4. Migrating from ProjectA.bd to ProjectB.bd
5. Cross Probing with timing closure
6. The toolbar review
- 2018.3 Preview ---
7. Selective migration from Vivado 2018.1 to 2018.3
8. What changed during upgrade in the block diagram
9. Migrating to the Versal NoC

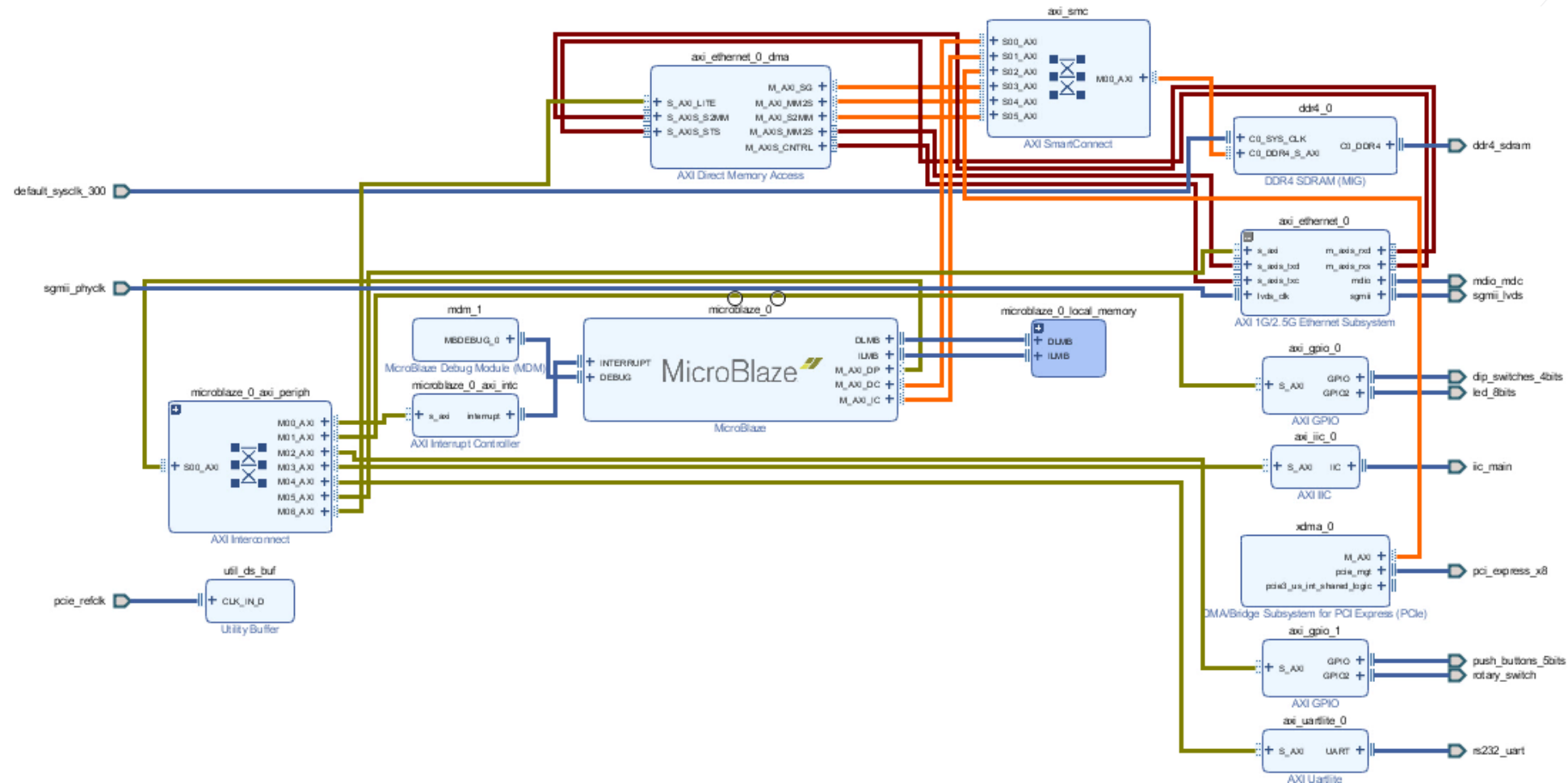


Working with complex IP  
Ease of Use

Team Based Design  
Migration  
Next generation devices

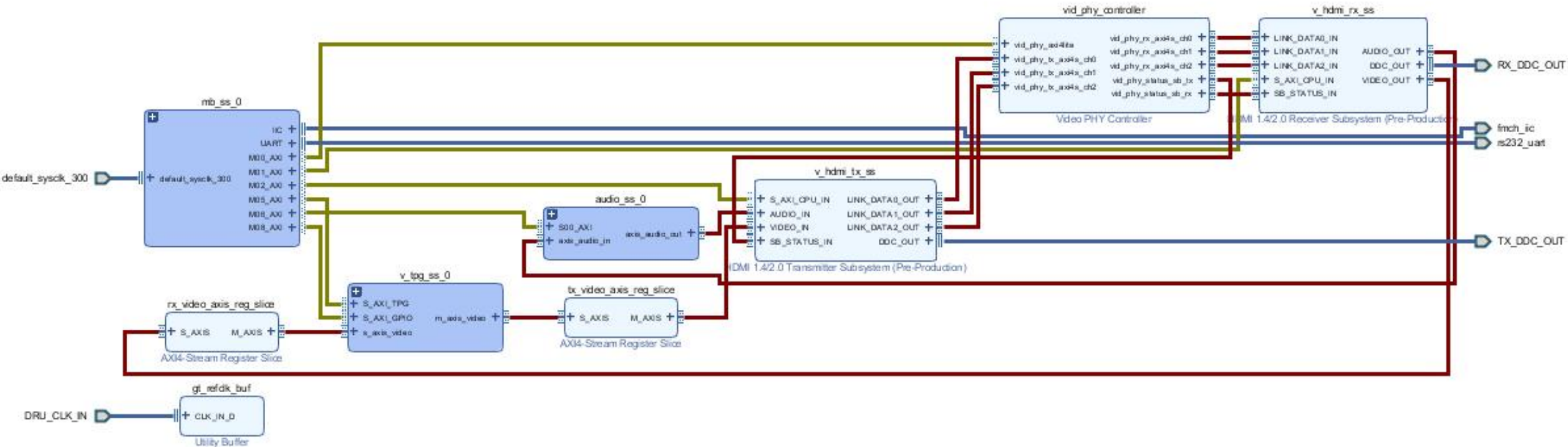
# 1. Ease of Use – Designer Assistance

> Board, Block, and Connectivity Automation helps to put together systems



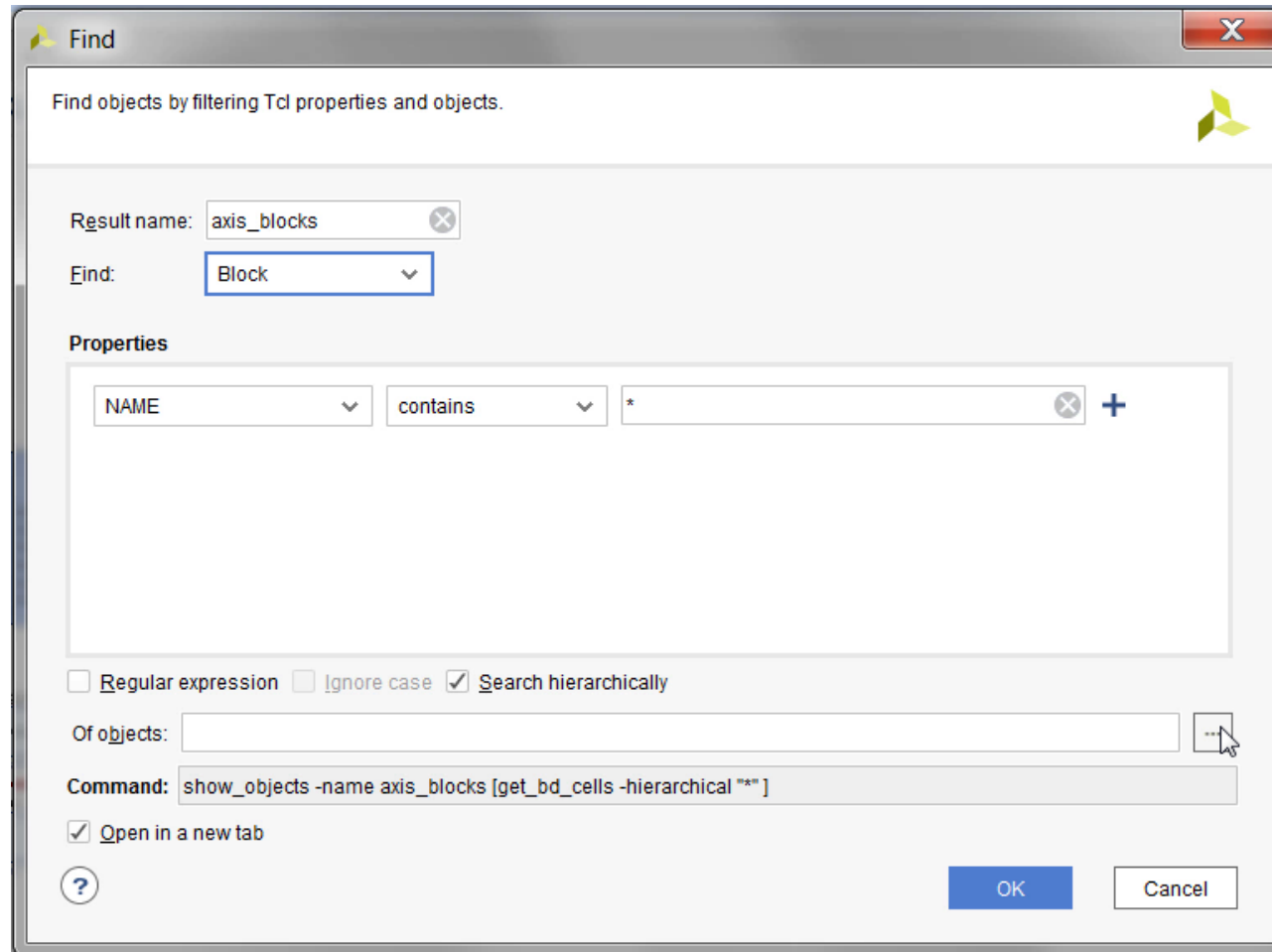
# 2. Example – Example Designs

> Example Designs can be launched from IP Integrator or IP Catalog



# 3. Ease of Use – “Super Find” in IP Integrator

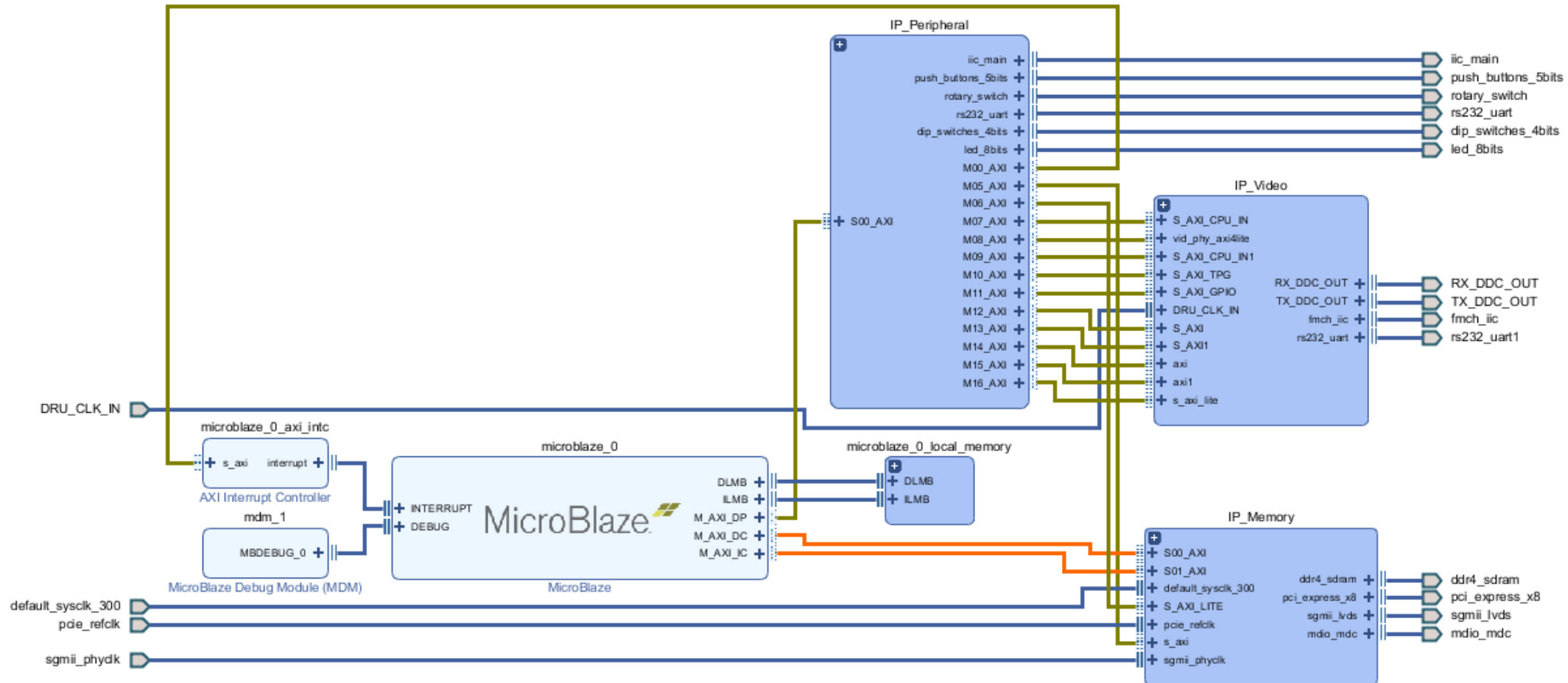
- > Find items on the canvas based on connectivity, naming, or properties





# 4. Migration – From One Block Diagram to Another

> Block diagrams should be in the same project



# 5. Ease of Use – Cross Probe from Timing Analysis

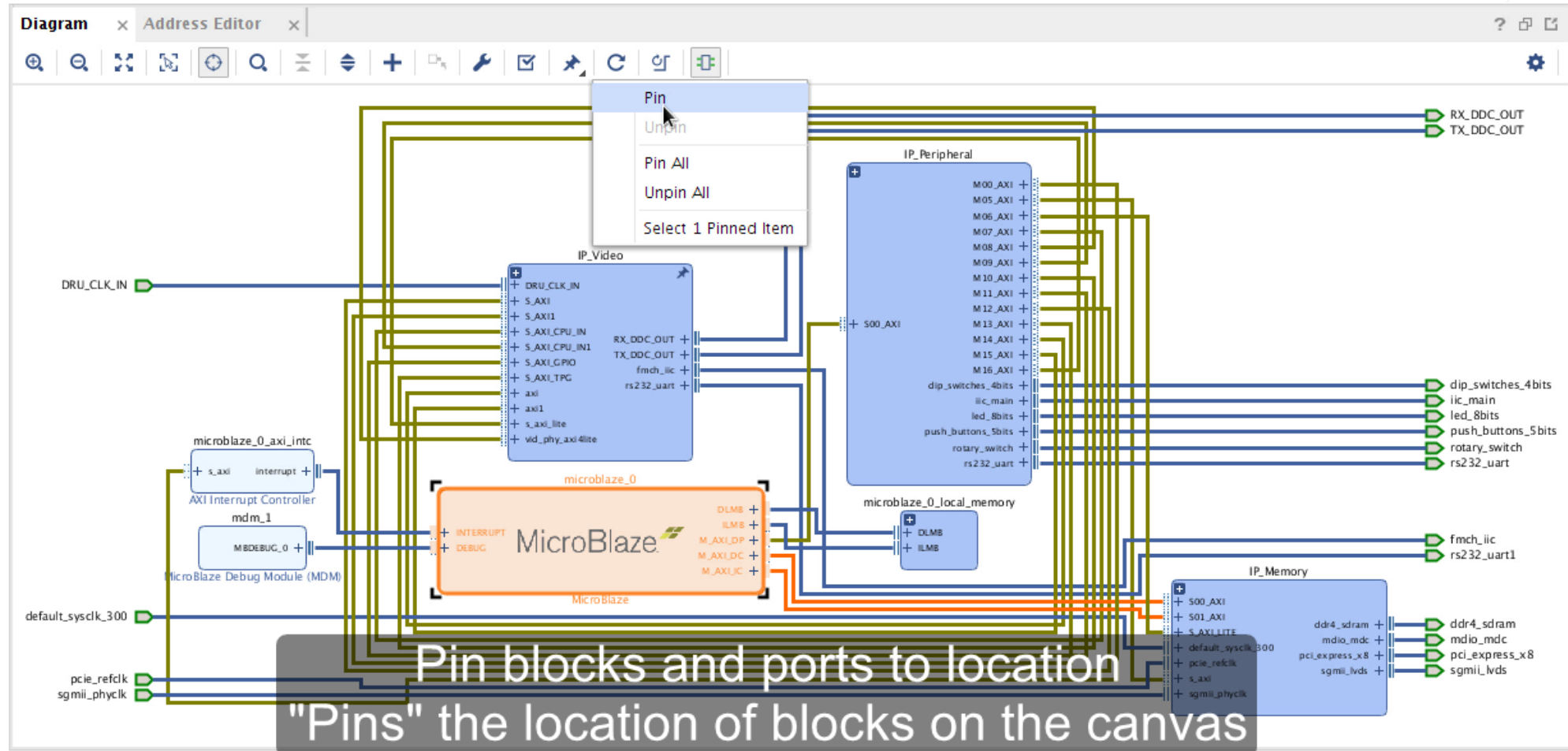
> Quickly find areas that need improvement

The image displays two side-by-side screenshots of the Xilinx Vivado IDE. The left window, titled 'IMPLEMENTED DESIGN - xcku040-ftva1156-2-e (active)', shows a netlist on the left and a device grid on the right. The right window, titled 'BLOCK DESIGN - video\_400', shows a block diagram with various components like 'Video Timing Controller' and 'Video In Axis D'. A 'Timing' window is open at the bottom, showing a table of failing timing paths. A callout box with the text 'Select Failing Timing Paths' points to the table.

Slack	Levels	High Fanout	From
Setup -0.022 ns (10)	-0.022	2	37 video_400_i/MicroBlaze_subsystem/microblaze_0_axi_periph/m01_couplers/auto_cc/inst/gen_clock_conv/gen_sync_conv/gen_conv_read_ch_ar_...
Hold -0.038 ns (10)	-0.022	2	37 video_400_i/Mic...oab_r_reg[8]/C
m01_couplers to m01_couplers	-0.016	2	
m01_couplers to m01_couplers	-0.016	2	
m01_couplers to m01_couplers	-0.016	2	
m01_couplers to m01_couplers	-0.016	2	

# 6. Ease of Use – Stop Squirming - Pin IP on Canvas

> A review of the toolbar actions




# A Preview of IP Integrator's Migration Assistance in 2018.3



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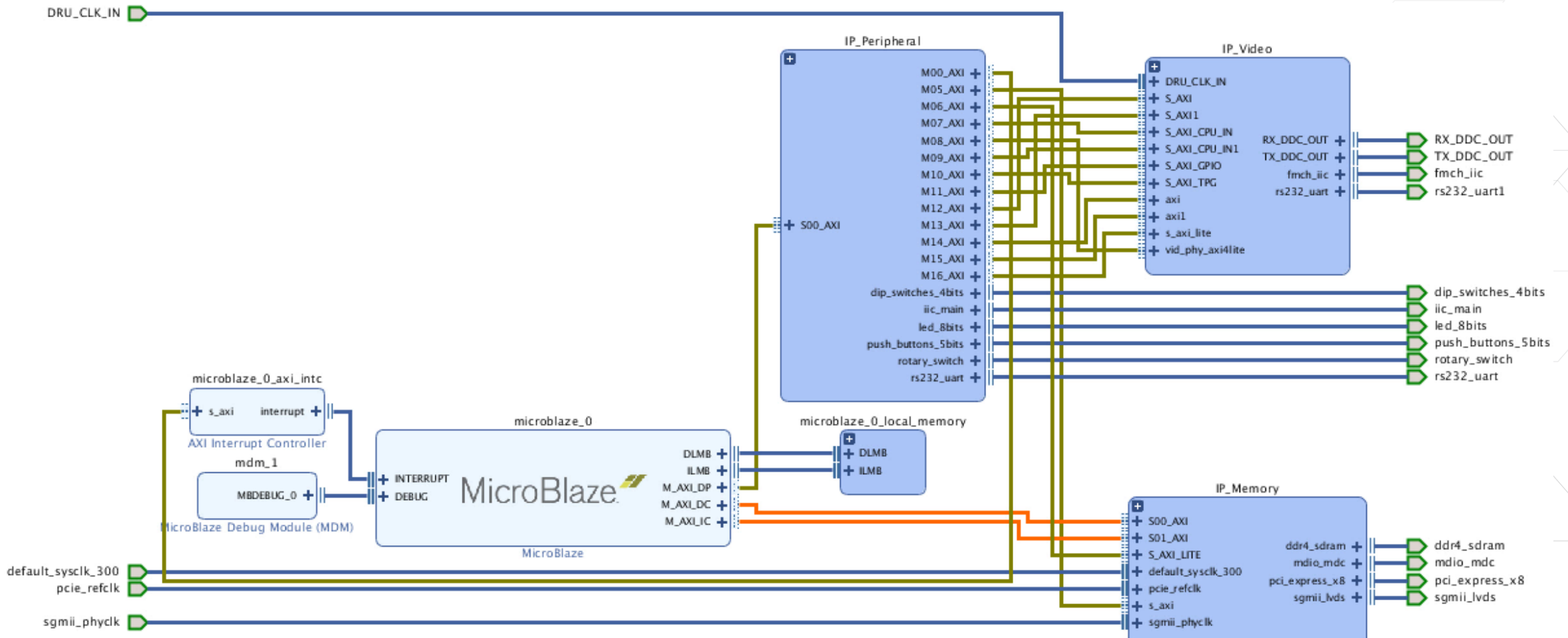


Working with complex IP  
Ease of Use

Team Based Design  
Migration  
Next generation devices

# 7. Migration – Vivado Versions via Partial Update

> Keep the blocks which have been previously validated in-system



# 8. What Changed In the Upgrade?

> New interactive report shows differences between block diagrams

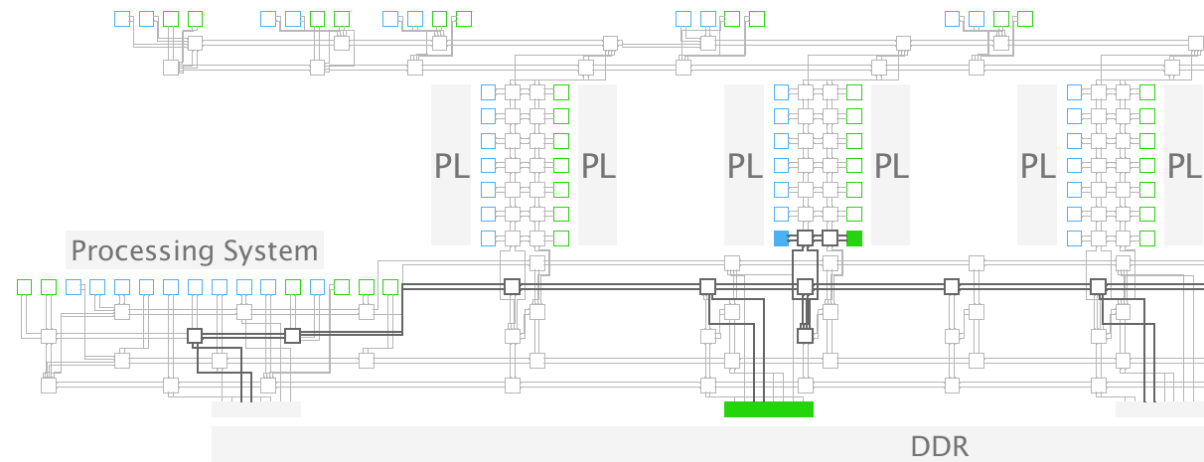
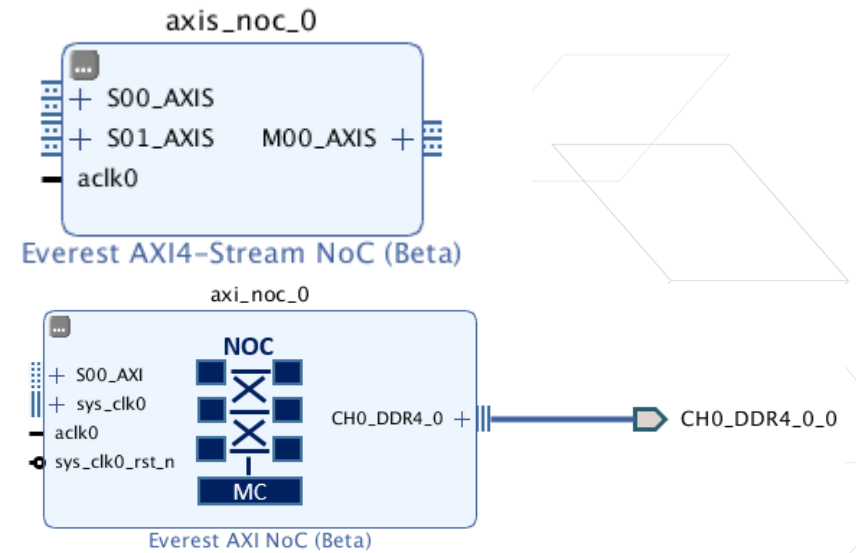
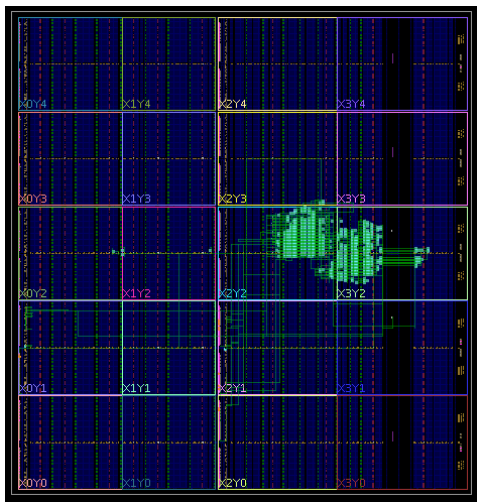
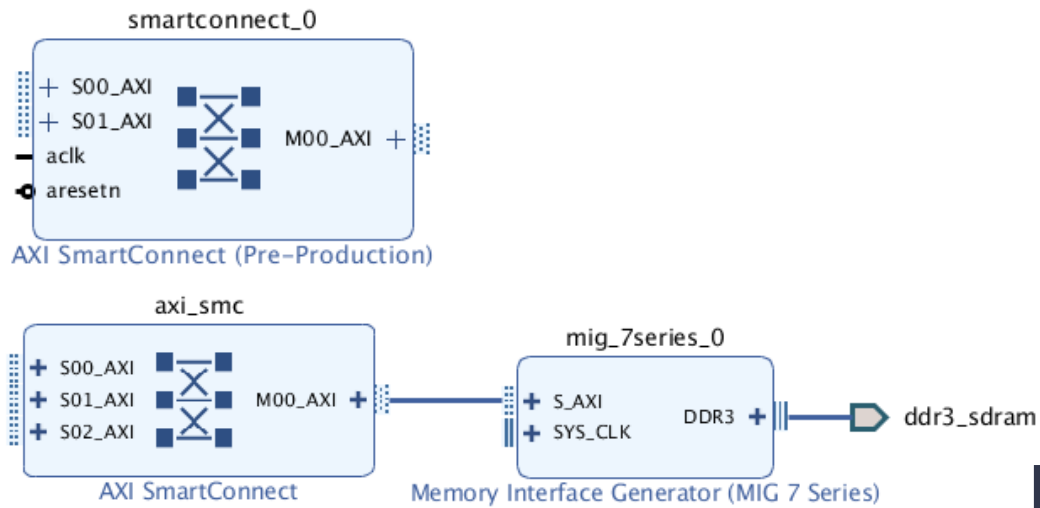
**Block Diagram Differences**

# Previous Next Show Filter Expand All Expand Diffs Collapse All

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design_1.bd	/home/danielm/Desktop/vivLogs/XDF18/combined/combined/srcs/sources_1/bd/design_1/design_1.bd
<ul style="list-style-type: none"><li>Design<ul style="list-style-type: none"><li>Components (9)<ul style="list-style-type: none"><li>IP_Memory<ul style="list-style-type: none"><li>Components (3)<ul style="list-style-type: none"><li>IP_DDR_MPMC<ul style="list-style-type: none"><li>Components (3)<ul style="list-style-type: none"><li>axi_smc<ul style="list-style-type: none"><li>Interface Ports (7)<ul style="list-style-type: none"><li>S00_AXI</li></ul></li></ul></li></ul></li></ul></li></ul></li></ul></li></ul></li></ul></li></ul>	<ul style="list-style-type: none"><li>Design<ul style="list-style-type: none"><li>Components (9)<ul style="list-style-type: none"><li>IP_Memory<ul style="list-style-type: none"><li>Components (3)<ul style="list-style-type: none"><li>IP_DDR_MPMC<ul style="list-style-type: none"><li>Components (3)<ul style="list-style-type: none"><li>axi_smc<ul style="list-style-type: none"><li>Interface Ports (7)<ul style="list-style-type: none"><li>S00_AXI<ul style="list-style-type: none"><li>memory_map_ref=S00_AXI</li></ul></li></ul></li></ul></li></ul></li></ul></li></ul></li></ul></li></ul></li></ul></li></ul>

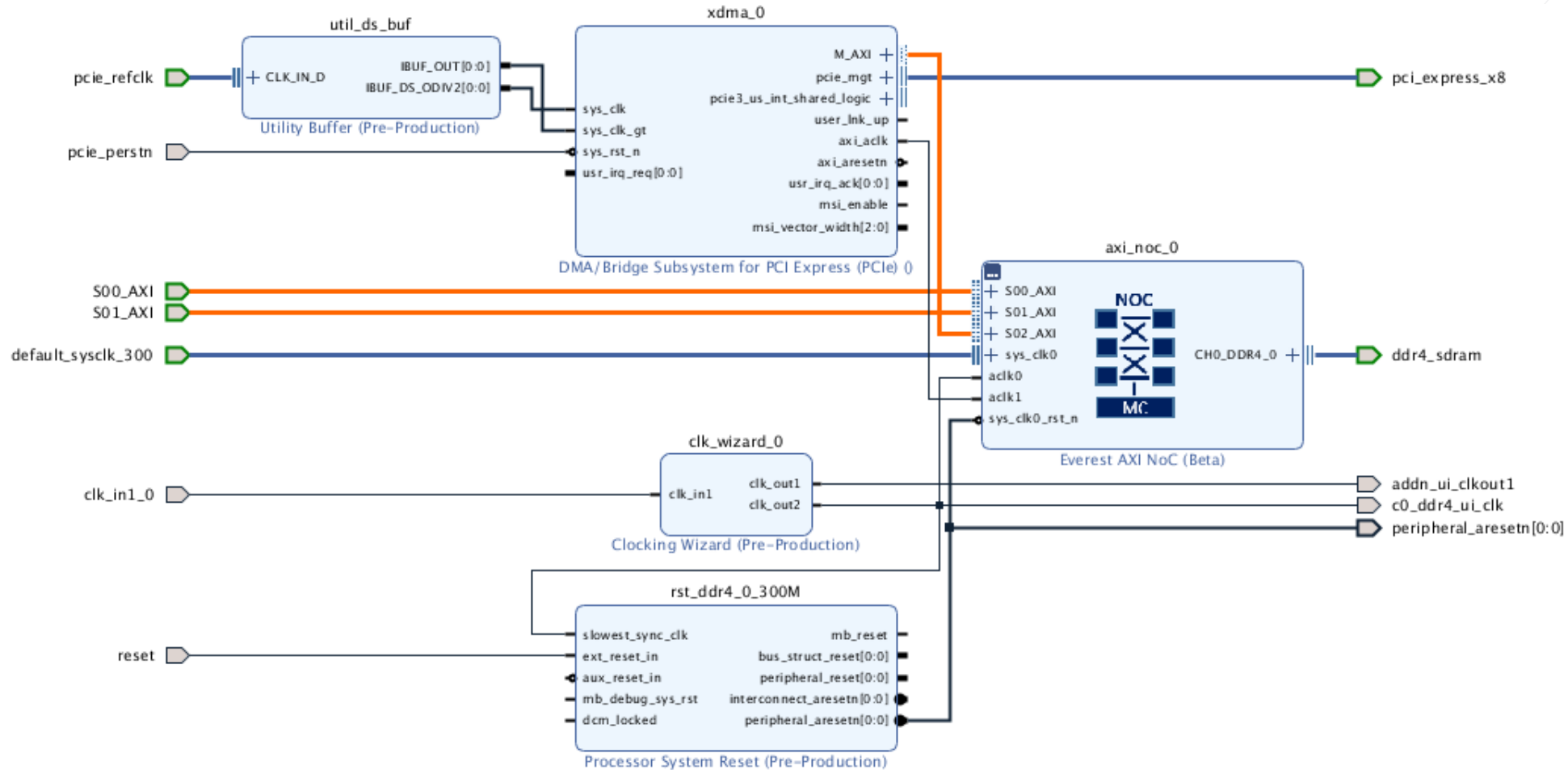
# Preview: Versal NoC!





# 9. Migrating to Versal ACAP

> Upgrading our current project to reduce programmable logic resources (area)



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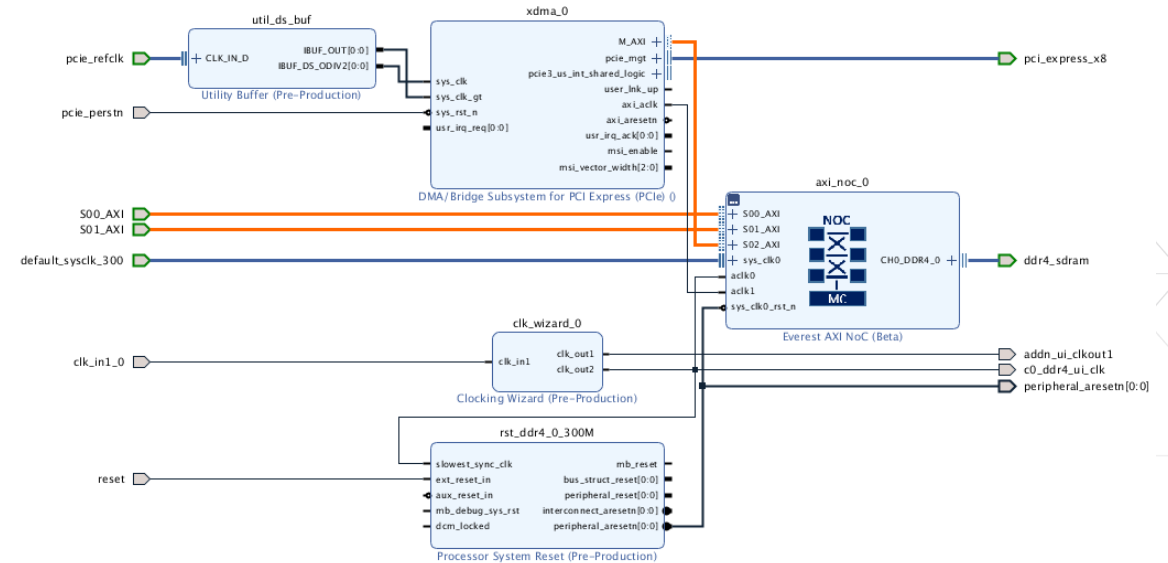
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# Changes to Our Release Schedule

- > **Vivado previously had four full releases per year**
  - >> 2017.1 & 2017.3 introduced new features
  - >> 2017.2 & 2017.4 improved quality – Many users installed only the even releases
- > **In 2018, we will have three full releases**
  - >> 2018.3 is coming soon
- > **And two in 2019**
  - >> Spring and Fall – No more wait states for new features or quality
  - >> Quality is our top priority



# Key Concepts: Vivado IP Integrator 2018.3

## Board, Block, Connectivity, and Migration Assistance

- > Take advantage of IP Integrator's built in assistance to create your ideal processing system -- including adding customized interfaces for networking, video, and DSP

## Getting ready to migrate to Versal ACAP

- > The migration to Versal ACAP will continue to add new assistance features and increase the traceability of IP Integrator

The logo features a red chevron pointing right, followed by the letters 'XDF' in a white, bold, sans-serif font.

XILINX  
DEVELOPER  
FORUM

