Defense-Grade FPGAs

Virtex®-5Q FPGAs

	Part Number	XQ5VLX30T	XQ5VLX85	XQ5VLX110	XQ5VLX110T	XQ5VLX155T	XQ5VLX220T	XQ5VLX330T	XQ5VSX50T	XQ5VSX95T	XQ5VSX240T	XQ5VFX70T	XQ5VFX100T	XQ5VFX130T	XQ5VLX200T
Logic Resources	Slices[2]	4,800	12,960	17,280	17,280	24,320	34,560	51,840	8,160	14,720	37,440	11,200	16,000	20,480	30,720
	Logic Cells[3]	30,720	82,944	110,592	110,592	155,648	221,184	331,776	52,224	94,208	239,616	71,680	102,400	131,072	196,608
	CLB Flip-Flops	19,200	51,840	69,120	69,120	97,280	138,240	207,360	32,640	58,880	149,670	44,880	64,000	81,920	122,880
Memory Resources	Maximum Distributed RAM (Kb)	320	840	1,120	1,120	1,640	2,280	3,420	780	1,520	4,200	820	1,240	1,580	2,280
	Block RAM/FIFO w/ECC (36 Kb each)	36	96	128	148	212	212	324	132	244	516	148	228	298	456
	Total Block RAM (Kb)	1,296	3,456	4,608	5,328	7,632	7,632	11,664	4,752	8,784	18,576	5,328	8,208	10,728	16,416
Clock Resources	Digital Clock Manager (DCM)	4	12	12	12	12	12	12	12	12	12	12	12	12	12
I/O Resources	Phase-Locked Loop/PMCD	2	6	6	6	6	6	6	6	6	6	6	6	6	6
	Maximum Single-Ended Pins	360	560	800	680	680	680	960	480	640	960	640	680	840	960
	Maximum Differential I/O Pairs	180	280	400	340	340	340	480	240	320	480	320	340	420	480
Embedded Hard IP Resources	DSP48E Slices	32	48	64	64	128	128	192	288	640	1,056	128	256	320	384
	PowerPC® 440 Processor Blocks	—	—	—	—	—	—	—	—	—	—	1	2	2	2
	Interface Blocks for PCI Express®	1	—	—	1	1	1	1	1	1	1	3	3	3	4
	10/100/100 Ethernet MAC Blocks	4	—	—	4	4	4	4	4	4	4	4	4	6	8
	RocketIO™ GTP Low-Power Transceivers	8	—	—	16	16	16	24	12	16	24	—	—	—	—
	RocketIO GTX High-Speed Transceivers	—	—	—	—	—	—	—	—	—	—	16	16	20	24
Configuration	Configuration Memory (Mb)	9.4	21.9	29.1	31.2	43.1	55.2	82.7	20	35.8	79.7	27.1	39.4	49.3	70.9
Miscellaneous	Speed Grades	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1	-1	-1, -2	-1	-1	-1, -2	-1, -2	-1, -2	-1
	Manufacturing Grades	I	I	I	I	I	I	I	I	I	I	I, M[7]	I, M[7]	I	I

Package	Area	Available User I/O: SelectIO™ Interface Pins[4] (GTP/GTX Serial Transceivers)													
EF676	27 x 27 mm		440	440											
EF1153	35 x 35 mm			800											
FF323	19 x 19 mm	172 (4)													
EF665	27 x 27 mm								360 (8)			360 (8)			
EF1136	35 x 35 mm				640 (16)	640 (16)				640 (16)		640 (16)	640 (16)		
EF1738	42.5 x 42.5 mm						680 (16)	960 (24)					680 (16)	840 (20)	
FF1738	42.5 x 42.5 mm										960 (24)				960 (24)

XMP076 (v2.3)

Notes: 1. A single Virtex-5Q FPGA CLB comprises two slices, with each containing four 6-input LUTs and four flip-flops (twice the number found in a Virtex-4 FPGA slice), for a total of eight 6-LUTs and eight flip-flops per CLB.

2. Virtex-5 FPGA logic cell ratings reflect the increased logic capacity offered by the new 6-input LUT architecture.

3. Digitally Controlled Impedance (DCI) is available on I/Os of all devices.

4. I/O standards supported: HT, LVDS, LVDSEXT, RSDS, BLVDS, ULVDS, LVPECL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVTTL, PCI33, PCI66, PCI-X, GTL, GTL+, HSTL I (1.2V,1.5V,1.8V), HSTL II (1.5V,1.8V), HSTL III (1.5V,1.8V), HSTL IV (1.5V,1.8V), SSTL2 I, SSTL2 II, SSTL18 I, and SSTL18 II.

5. One system monitor block included in all devices.

6. Available I/O for each device-package combination: number of SelectIO interface pins (number of RocketIO transceivers).

7. M-grade available only in -1 speed grade and EF1136 package.

Manufacturing Grades

http://www.xilinx.com/products/milaero/rpt003.pdf

Grade	Description	Temperature
V	Xilinx V-Grade Flow[1] Military Ceramic	T_j = –55°C to +125°C
H	Flip-Chip Radiation Tolerant Ceramic	T_j = –55°C to +125°C
B	SMD Radiation Tolerant and Non-RT SMD Military Ceramic	T_j = –55°C to +125°C
N	Military Plastic	T_j = –55°C to +125°C
M	Military Ceramic or Plastic	T_j = –55°C to +125°C
I	Industrial Plastic	T_j = -40°C to +100°C

Notes: 1. Per ADQ0007

Important: Verify all data in this document with the device data sheets found at www.xilinx.com