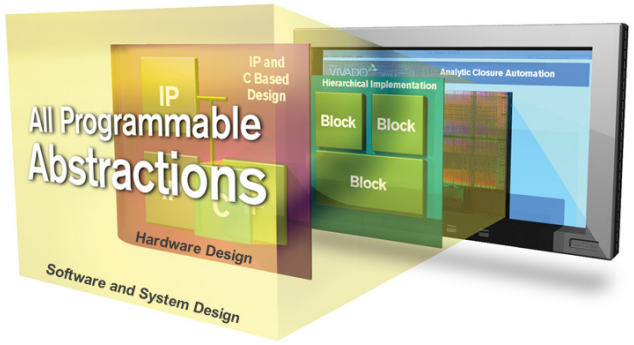
ALL PROGRAMMABLE ABSTRACTIONS
THE WAY FORWARD FOR ALL PROGRAMMABLE REALIZATION

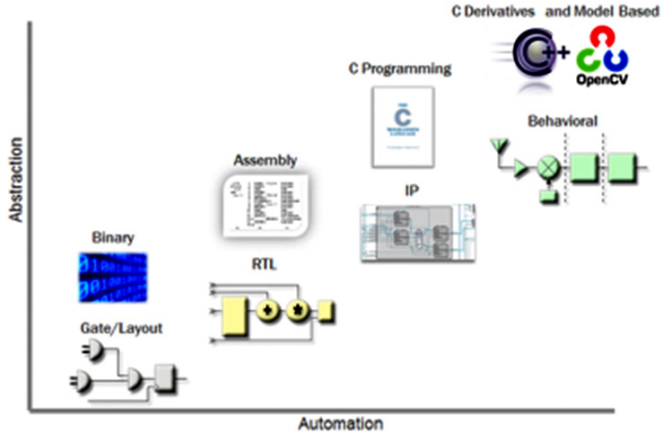
All Programmable Abstractions are a set of design flow abstractions from Xilinx and its Ecosystem of Alliance members that accelerates product development, enables software developers to use custom hardware accelerators and assists systems engineers to optimize hardware / software performance. All Programmable Abstractions push beyond traditional RTL design methodologies to automate all aspects of system development and algorithm deployment into all programmable FPGAs, SoC and 3D ICs. Xilinx and its Alliance members are working together to deliver a comprehensive set of solutions that accelerate the development process by leveraging abstractions that best fit the design team and target application.

ALL PROGRAMMABLE ABSTRACTION AND AUTOMATION



Automation of abstractions is made possible by the adoption of industry standards and open source communities. By leveraging industry standard programming languages and the Eclipse-based tool chain, the ARM® AMBA AXI4 interface, standards based plug-and-play IP with IP-XACT and IEEE1735 encryption, Xilinx and its ecosystem are delivering industry leading design methodologies, tools and IP that facilitates the automation of All Programmable FPGAs, SoCs and 3D ICs.

ABSTRACTIONS THAT HAVE DRIVEN AUTOMATION



Accelerating Development for Hardware Engineers

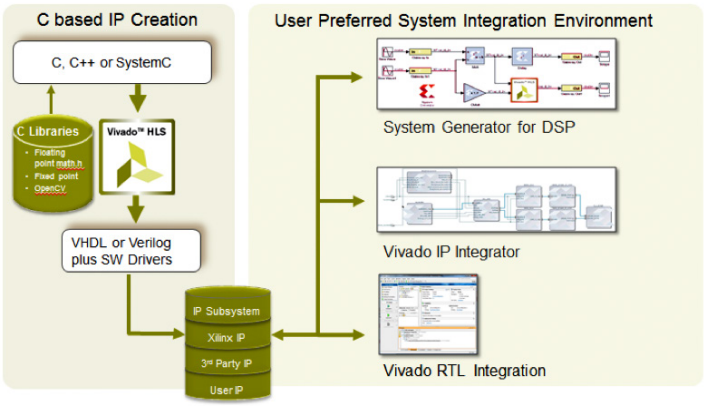
In 1981, the United States Department of Defense was "addressing the hardware life cycle crisis" with the development of the VHSIC Hardware Description Language (VHDL)*. The requirement called for a language with a wide range of descriptive capabilities that would produce equivalent results on any simulator and be independent of technology and design methodology. In parallel, a company called Gateway Design Automation developed a logic simulator, Verilog-XL that was later acquired by Cadence® Design Systems. The language was then put into the public domain, enabling other EDA companies to build automation around it. VHDL and Verilog quickly became standards and automation soon followed.

The Xilinx All Programmable Abstractions initiative builds on this foundation with new, robust, IP-centric design flows that deliver significant productivity improvements that helps designers get products to market faster so companies can achieve the first to market advantage.

C-based IP Generation with Vivado High-Level Synthesis

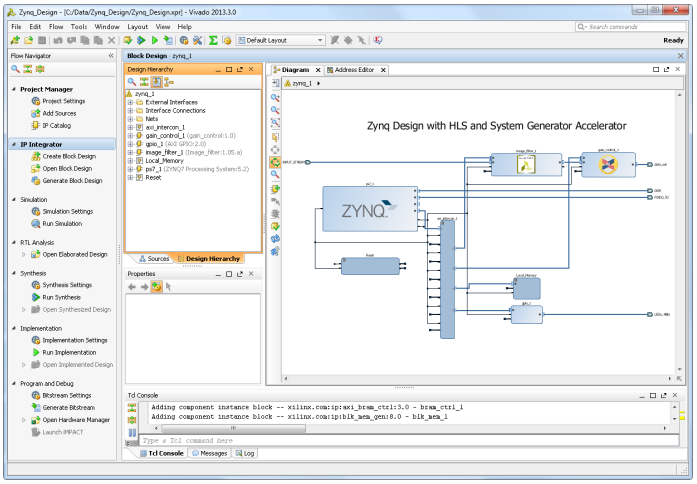
Advanced algorithms used today in wireless, medical, defense, and consumer applications are more sophisticated than ever before. To model these algorithms, many design teams turn to C/C++ or SystemC because of the sheer simulation performance over RTL based simulations. In some cases the C code runs 1000X faster than the corresponding RTL. The challenge becomes the need to recode these algorithms in RTL for hardware implementation which is time consuming and error prone.

VIVADO HIGH LEVEL SYNTHESIS



With C-based IP generation with Vivado® High Level Synthesis (HLS), this process is greatly accelerated, by enabling the C specification to be directly targeted into Xilinx All Programmable devices without the need to manually create RTL. Vivado HLS is part of the Vivado Design Suite, System Edition.

VIVADO IP INTEGRATOR



Block-based IP Integration with Vivado IP Integrator

The Vivado® Design Suite is also now delivering intelligent IP integration with the new IP Integrator feature. Vivado IP Integrator (IPI), provides a graphical and Tcl based, correct-by-construction, IP- and system-centric design development flow. This integration environment is platform aware which simplifies the integration of hardware board peripherals and device aware to ensure that maximum system bandwidth is achieved.

Working at the interface level, design teams can rapidly assemble complex systems that leverages IP created with Vivado HLS, System Generator, SmartCORE™ IP and LogiCORE™ IP, Alliance Member IP as well as customer's proprietary IP.

The Vivado IPI built-in automated interface, device driver, and address map generation, speeds design assembly, enabling faster systems implementation than ever before.

Enabling Software Developers with Custom Hardware Performance

Innovations like the C programming language, developed at Bell Laboratories in 1972 by Dennis Richie, made it possible to have a high level, machine independent programming that still allowed the programmer to control the behavior of individual bits of information. Because of C's power and flexibility the UNIX operating system, which was originally written in assembly code, was almost immediately re-written in C. With this close tie to UNIX and the availability of C compliers (automation), C spread rapidly, becoming an ANSI standard in 1983.

While researching his PhD thesis in 1978, Bjarne Stroustrup began work on "C with Classes" which as the name implies was meant to be a superset of the C language. His goal was to add object-oriented programming into the C language while maintaining the portability without sacrificing performance or low-level controllability. In 1983 the name was changed to C++ and new features were added along with additional complier support.*

Today over 60% of embedded systems are programmed in C and companies typically employ 4-5 software engineers for every hardware engineer. Xilinx All Programmable Abstractions helps enable this software-centric design community to take advantage of the performance acceleration that can be achieved in custom hardware "accelerators" implemented in programmable logic on FPGAs and All Programmable SoC devices.

C-based IP Generation with Vivado High Level Synthesis

Vivado HLS not only offers a significantly faster way for hardware developers to create IP that can be integrated into system designs using IP Integrator, but also offers way to target software developed in C/C++ to hardware accelerators for programmable logic.

Software-based System Realization with C/C++ and OpenCL

Xilinx is now working with early customers on a new system level, heterogeneous parallel programming environment that leverage abstractions such as C/C++ or OpenCL®, in a comprehensive Eclipse-based development environment.

This new environment provides market-specific libraries to significantly improve productivity of verified heterogeneous systems and is architected to empower system architects and SW application developers who require a parallel architecture, to increase system performance, reduce BOM cost and lower total power with development times in line with ASSP, DSPs, and GPUs.

Hardware Abstraction with QEMU and Cadence Virtual Platform

Finally for SW developers who need to start application code development before the hardware platform is available, Xilinx provides hardware virtualization with Quick Emulator or QEMU, an open source virtual machine that emulates the system hardware/software interfaces for both the MicroBlaze™ soft processor and the Zynq® All Programmable SoC. The earlier software development results in higher productivity, and continuous hardware/software integration validation.

In addition Xilinx has partnered with Cadence® Design Systems to provide their Virtual System Platform targeted specifically for the Zynq-7000 All Programmable SoC. These virtual platforms, together with the Xilinx Software Development Kit (SDK), deliver true homogenous and heterogeneous multi-processor design and debug, enabling design teams to shave months off development schedules.

Rapid Algorithms to Platform Deployment for Systems Engineers

All Programmable Abstractions, through system modeling environment Alliance Members like the MathWorks® and National Instruments®, allows system engineers to evaluate the feasibility and performance of their algorithms on All Programmable FPGAs and SoCs early in the development process and to optimize system performance through hardware / software partitioning. These abstractions automate the rapid deployment of algorithms onto application specific hardware platforms interfaced to real world signals, videos or networks.

Model-based Design with MathWorks MATLAB and Simulink

For Model-based design, the MathWorks has released a new guided workflow with their R2013b release. The guided workflow enables software developers and hardware design engineers to create and model their algorithms in MATLAB™ and Simulink™, partition their designs between software and hardware, and automatically target, integrate, debug and test those models on Xilinx targeted design platforms for Zynq-7000 All Programmable SoC devices. Building on MathWorks

extensive portfolio of application specific toolbox libraries and robust embedded software and hardware code generation technology, this new functionality helps users verify and optimize system performance, and enables a wider community of developers to take advantage of the industry's first All Programmable SoC. With the new flow, users partition an algorithm into SW and HW modules and then generate C code for the ARM processor-based Zynq SoC with the MathWorks Embedded Coder and RTL code for the programmable logic using the MathWorks HDL Coder or Xilinx's System Generator. For more information about this flow please visit **www.mathworks.com/zynq**

The Vivado® Design Suite System Edition also includes Xilinx's System Generator for DSP, the industry's leading high-level tool for creating production-quality DSP algorithms in a fraction of time compared to traditional RTL. System Generator accelerates the development of highly parallel systems by empowering developers to seamlessly integrate arithmetic functions, LogiCORE IP blocks, custom RTL and C-based Vivado HLS blocks with the industry's most advanced All Programmable system modeling from Simulink and MATLAB .

Platform-based Design with National Instruments RIO Platforms and LabVIEW

Embedded system designers use LabVIEW and National Instruments® (NI) re-configurable I/O (RIO) hardware to abstract the complexity of traditional RTL design and avoid the time consuming tasks of building an operating system, drivers, and middleware for deployment targets. National Instruments created a platform-based approach to embedded design that includes off the shelf re-configurable hardware and intuitive graphical programming. With a single-click, the NI LabVIEW 2013 development environment can compile, debug, and deploy applications written for processor or programmable logic on NI targets. This development environment currently supports multiple Xilinx All Programmable devices. NI chose Xilinx All Programmable SoCs and FPGAs for the RIO computing core, platform of over 60 deployable targets. For information about this flow please visit **www.ni.com/xilinx**

Summary

Xilinx is committed to providing abstractions that can be leveraged by all design team members targeting All Programmable devices. The goal is clear: accelerate time to market and reduce development costs while automating the development process. With All Programmable Abstractions systems, software and hardware designers can go from concept to released products faster than ever before. For more information, please visit **www.xilinx.com/apa**

Take the NEXT STEP

To learn more about the Vivado Design Suite featuring the IP Integrator, please visit **www.xilinx.com/apa**

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*Historical data source: Wikipiedia.org

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