Xilinx Plug-and-Play IP: Accelerating Productivity and Design Reuse

Introduction

As today's designs integrate increasing amounts of functionality, designers must have access to proven, up-to-date, easy-to-use IP from reliable sources to accelerate their design cycles. The ability to deliver high-performance systems at the lowest total design cost on time and within budget depends upon the ability to rapidly combine and configure dozens or hundreds of design elements including on-chip logic blocks, processor cores, and a wide range of IP cores. The Plug-and-Play IP initiative is the Xilinx response to the growing customer demand for system-level design support for the use of multiple IP cores from diverse internal and third-party sources. Plug-and-Play IP cores from Xilinx® and its Alliance Program members meet this demand by providing simple yet powerful capabilities that vastly improve designer productivity by supporting easier IP reuse, allowing design teams to create complex systems with minimal effort.

These Plug-and-Play IP blocks combined with Xilinx All Programmable device families including FPGAs, SoCs and 3D ICs allow design teams to maximize system performance, lower power consumption, and reduce BOM costs with maximum design flexibility across a wide range of end markets and target applications. The high-speed serial transceivers, high-performance programmable logic, and massive DSP processing bandwidth incorporated into these All Programmable devices in combination with the Xilinx Vivado® Design Suite with its broad offering of Plug-and-Play SmartCORE™ and LogiCORE™ IP cores accelerates designer productivity through fast and efficient design reuse. Further, Xilinx is delivering a major ease-of-use IP improvement with the release of Vivado Design Suite 2013.3. This upgrade improves design verification and enables designers to customize and debug IP cores according to their system needs, without having to manually edit the core.

To ensure portability and interoperability among IP offerings from Xilinx and its Alliance members, Xilinx has taken a standards-based approach to delivering proven, easy-to-use IP cores. The three critical standards that enable the development of Plug-and-Play IP are:

- The AMBA® AXI™4 interconnect protocol developed in conjunction with ARM
- The IEEE P1735 encryption and rights-management standard for design IP
- The IP-XACT XML Schema specifying IP metadata and interconnection from Accellera and based on IEEE 1685-2009

The Xilinx Plug-and-Play IP initiative leverages these industry standards to accelerate IP integration in system-level designs.

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AMBA AXI4 IP Interconnect

Xilinx worked closely with ARM to define AXI4, the fourth generation of the AMBA interface. By using AXI4 as a standard interface, Xilinx Plug-and-Play IP cores eliminate the overhead of integrating IP that have incompatible interfaces. Benefits to designers include:

- **Increased productivity:** The AXI4 specification eliminates the need for multiple legacy or custom interfaces formerly required to integrate IP cores from various sources.

- **Greater flexibility:** The AXI4 specification accommodates a wide range of system performance and resource requirements. It is inherently scalable, enabling system designers to optimize their designs for the highest possible FMAX, maximum throughput, lower latency, smaller area, or a combination of these attributes.

- **Greater IP availability:** The AXI4 specification enables and encourages the Xilinx IP ecosystem and the ARM IP ecosystem to efficiently develop IP for use in Xilinx's All Programmable FPGAs and SoCs.

- **Higher Quality IP:** By leveraging industry-standard verification IP and methodologies while standardizing on the AXI4 interface, IP providers and customers can accelerate production of high quality, pre-verified IP cores and design components. This results in faster design validation and reduces system debug effort enabling shorter development cycles.

Released as part of the next-generation AMBA specification (AMBA 4), the AXI4 specification consists of three interconnect protocols that cover the full gamut of IP interconnect requirements encountered in FPGA and ASIC designs today:

- **AXI4:** A traditional single-address burst interconnect supporting up to 256 data beats per burst, with a system-dependent data width.

- **AXI4-Lite:** An area-efficient subset of the AXI4 protocol that sends only one data word per transaction.

- **AXI4-Stream:** A data-streaming interconnect that supports unidirectional, high-speed data transfers from master to slave with greatly reduced signaling. This interconnect efficiently accommodates the high-bandwidth streaming I/O requirements of multi-gigabit serial protocols and non-processor based IP, as often used for video and audio designs.

Table 1 summarizes the attributes and use models for these three AMBA AXI4 protocols:

Interface	Applicability	Features
AXI4	High performance memory-mapped requirements	Traditional memory-mapped address/data interface Data burst support
AXI4-Lite	Simple, low-throughput memory-mapped communication	Traditional memory-mapped address/data interface Single data cycle only
AXI4-Stream	High-speed streaming data	Data-only burst

Table 1: AXI4 Use Models

Now using a common AXI4 interconnect, designers can easily add, remove, or replace IP blocks within a design—and that's a key hallmark of Xilinx Plug-and-Play IP.

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IEEE 1735 IP Encryption and Rights Management

Design teams increasingly rely upon third-party IP cores to shorten or at least maintain design cycle times as system-design complexity increases. This third-party IP is often sourced from several internal and third-party sources. Each source likely requires different protection levels within the design-tool flows. The various protection/encryption schemes developed by the many potential IP vendors complicate the use of protected IP in these design flows, including the design tools from Xilinx and its Alliance EDA providers.

As part of its Plug-and-Play IP initiative, Xilinx has adopted the IEEE P1735 encryption standard to ensure interoperability among IP sources, EDA tools, and the IP cores themselves. The IEEE P1735 standard specifies syntaxes for IP encryption and rights management and provides recommendations for integration with design-specification formats described in other standards. It also recommends use models for interoperable tool and hardware flows, which include encryption, encoding algorithms, and encryption key management.

The Vivado Design Suite 2013.3 leverages the IEEE P1735 standard to provide integrated flows that support verification of designs containing Xilinx LogiCORE and SmartCORE IP using the Cadence Incisive® Enterprise simulator, the Synopsys VCS® simulator, the ModelSim® and Questa® Advanced simulators from Mentor Graphics®, and the Xilinx Vivado simulator.

Use of IEEE 1735 for all Xilinx SmartCORE and LogiCORE IP simplifies the task of encryption and rights management for all IP used in a design. That's the second hallmark of Xilinx Plug-and-Play IP.

IP-XACT: Packaging and Catalog

The Vivado IP Packager and IP Catalog leverage the IP-XACT standard that was originally created by the SPIRIT Consortium as a standard structure for packaging, integrating, and reusing IP within tool flows. IP-XACT is now an approved IEEE Standard: IEEE 1685-2009.

The Vivado IP Packager makes a design with its constraints, test benches, and documentation available in an extensible IP catalog on a local or shared drive. A wizard-based flow in the IP Packager permits:

- Automatic generation of IP-XACT IP
- Automatic inference of many pieces of meta-data
- Support for the manual addition of meta-data not automatically inferred

The Vivado IP catalog provides an inventory of Xilinx, third-party, and intra-company IP that can be shared across a design team, a company division, or an entire company in a consistent and easy-to-use manner. All Xilinx IP—including embedded, DSP, video, interface, building block, and connectivity IP—is consolidated into a unified catalog view with a consistent access model across all designs and end applications.

Putting all Xilinx SmartCORE and LogiCORE IP into an easy-to-use, well-indexed catalog makes IP selection and use much easier for design team members. That's the third hallmark of Xilinx Plug-and-Play IP.

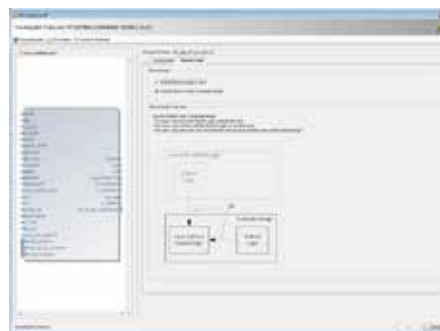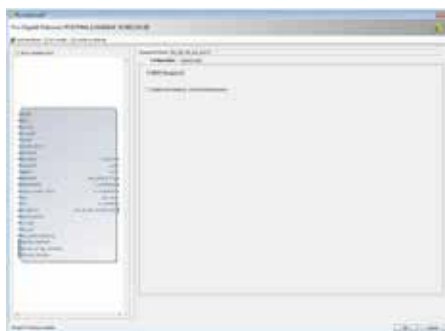**XILINX**

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IP Ease-of-Use in Vivado Design Suite 2013.3

The Vivado Design Suite 2013.3 release incorporates enhanced IP integration features that allow for system-wide co-optimization of a design and Xilinx IP. For instance:

- Designers can now share clocking resources throughout their design for connectivity IP cores such as an 10G Ethernet or RXAUI.
- Upgrades to the transceiver IP now provide easy top-level access to debug ports within the IP core.
- With new capabilities added to the Vivado logic analyzer, designers now have full read and write access to their AXI system at runtime. Designers can also perform hardware debug using advanced trigger features to detect and capture complex events.

These improvements are provided in an automated, but not automatic IP upgrade so that designers can customize and debug IP according to their system needs without having to manually edit an IP core. Designers can efficiently share clocking and reset resources across multiple connectivity IP instances to pack and target specific physical resources with easy top-level access to transceiver debug ports while generating the core through a simple dialog within the Vivado IP Catalog.

For example when implementing a 4x10G Ethernet implementation a designer may choose to use just one transceiver quad. Prior to the Vivado 2013.3 release, this choice required manual editing of the IP source hierarchy to pull out the GT common to the core's top level, to then delete all the extra GT common instances, and to connect the GT common output to the IP instances. With the new shared-clocking feature, it's much easier to put the GT common outside of the IP instance, thus making it available for other IP instances to use while also adding debug ports with the click of the mouse.

Summary

Xilinx has raised Plug-and-Play IP to the next productivity level by leveraging key industry standards and by adding major ease-of-use improvements and other enhancements to the Vivado Design Suite's intelligent integration feature, IP Integrator.

For more information on the IP ease-of-use features in Vivado 2013.3, please review the release notes and IP-specific Product Guides.

Take the NEXT STEP... please visit: www.xilinx.com/ipcenter

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