WIRELESS
Macrocell and Cloud-RAN Baseband Solutions

Industry Challenges

- An explosion of different air interfaces
- Evolving heterogeneous network architectures from single sector baseband units to high density Cloud-RAN installations
- Insatiable demand for data bandwidth
- Cost control: CAPEX/OPEX reduction
- Radio Densification: small cell backhaul
- Macro offload / WiFi integration
- Increasing transmission bandwidth while reducing system latency
- Lower power

Xilinx Baseband Solutions

- All Programmable FPGAs and SoCs for scalable, highly integrated macrocells (future-proof designs)
- Highly integrated devices delivering higher reliability while lowering power and BOM costs
- Inherently parallel architecture delivering massive bandwidth for advanced algorithms
- Dynamically programmable fabric for virtualization co-processing support in macrocell and C-RAN applications
- Class-leading tools and IP: Vivado® HLS for rapid development (C to RTL) and shortened time to market

Faster Time to Market For Highly Integrated, High-Performance Macrocell Baseband and Cloud-RAN Designs

Xilinx All Programmable FPGAs and system-on-a-chip (SoC) devices offer designers an ideal platform to address the rapidly changing requirements of evolving heterogeneous network infrastructure and virtualized network functions. Completely programmable and inherently scalable, Xilinx UltraScale™ devices are capable of delivering the dynamic balance of hardware/software processing and connectivity for emerging SDN/NFV network infrastructure. Unprecedented levels of integration enable designers to achieve higher reliability and fewer truck rolls along with reduced power and BOM costs.

A Generation Ahead for Scalable, Virtualized Network Performance

The Xilinx UltraScale family puts designers a generation ahead with a product portfolio enabling massive compute and connectivity bandwidth, dynamic reconfigurability to complement emerging visualization platforms and unrivaled performance per watt to address the incessant drive for more throughputs at lower power and cost. Leading-edge SerDes technology is enabling 28Gbps backplanes today and a scalable connectivity portfolio enables designers to accommodate the anticipated 25Gbps line rates for CPRI, SRIO and GbE.

In addition to All Programmable silicon platforms, Xilinx provides designers the with a rich portfolio of IP and high-level abstraction tools such as SDAccel™ and SDNet™ development environments to rapidly deliver proprietary signal and packet processing hardware accelerators. Together, the silicon and tools maximize IP reuse and platform design methodologies enabling rapid time to market for evolving Hetrogenous Networks comprising Cloud-RAN, virtualized network functions and multi-gigabit 5G air interfaces.

System Integration for Baseband

The move to Cloud-RAN, virtualized network functions and an all-IP evolved packet core is reshaping traditional baseband partitioning, its proprietary vertical integration with higher layers, scaleout of the baseband pool and IP-centric fronthaul connectivity to the radios. Xilinx UltraScale devices offer innovative designers an ideal platform to realize split Layer 1 processing, flexible 10GbE/CPRI connectivity and signal/packet processing hardware accelerators for emerging CPRI Aggregator Gateways in the fronthaul and dynamic hardware acceleration for virtualized network functions running on GPP's in the baseband pool.

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Emerging CPRI Aggregator / Gateway to Reduce Fronthual OPEX
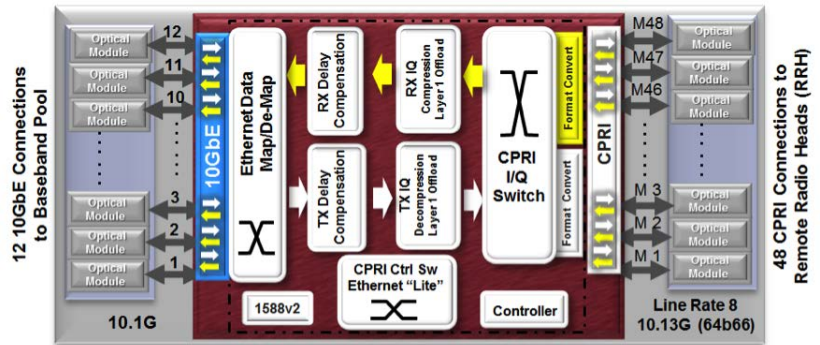
Motivations and Challenges for C-RAN GbE Fronthaul

Cloud-RAN strives to deliver lower CAPEX/OPEX costs through more efficient pooling of baseband resource, reduced site license costs and fewer truck rolls. Further cost reduction is anticipated with software LTE communication stacks dynamically provisioned as virtual functions running on general purpose processors and 10GbE delivering commodity transport/switching solutions out to the radio. However, with all of these innovations there are engineering and commercial challenges related to fronthaul fiber management and efficiency, system latency budgets, potential split partitioning of the LTE Layer 1 and delivering fronthaul over 10GbE/OTN while meeting the stringent jitter/latency requirements achieved with CPRI. Standards covering IQ over 10GbE and CPRI over OTN are not finalized, there are industry initiatives to drive CPRI, SRIO and GbE to 25Gbps and 5G brings a step function increase in the compute and connectivity requirements described above. In summary, there is a clear need to drive down costs but the needs are not clear in how best to solve the various challenges while maximizing market share with a commodity priced solution. Scalability, flexibility and design tools that minimize time to market are desirable features of next-generation solutions.

Xilinx Solutions for C-RAN & GbE Fronthaul

The Xilinx UltraScale portfolio enables developers to roll out pre-standards based equipment for 10GbE and CPRI over OTN solutions with the knowledge that these devices can adapt to standards when ratified and are able to address the evolving 25Gbps CPRI, Ethernet and SRIO initiatives when finalized.

Whether for a high-end fronthaul CPRI aggregator as shown in the diagram above, or a hardware accelerator offload engine to compliment established and emerging Layer 1 multi-core SOCs in the Cloud-RAN server racks, Xilinx UltraScale devices, Vivado Design Suite and a vibrant ecosystem deliver enabling technology solutions to address the needs of emerging heterogeneous network, Cloud-RAN and 5G platforms.

Take the NEXT STEP

Visit www.xilinx.com to learn more about the Xilinx wireless communications product portfolio and All Programmable FPGAs, 3D ICs and SoCs.

For information on Xilinx baseband solutions, visit
http://www.xilinx.com/applications/wireless-communications.html

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