WIRELESS
Connectivity & Timing




Design Challenges

- IO bandwidth within systems continue to increase
- While reliance on standards-based protocols is increasing, pseudo-proprietary protocols continue to flourish
- Exploding data traffic requires increased aggregation capability
- Scaling performance, port speeds, and port count to meet changing requirements
- Scalable and modular system designs to support a variety of form factors
- Reducing design development time, future proofing systems for protocol evolution, and accelerating market adoption

Xilinx Connectivity Platforms

- **JESD204B** IP core provides a serial data interface and the link protocol between data converters and logic devices
- **CPRI** IP core enables flexible base station architecture and is ideal for connectivity between Radio Equipment Controllers (REC) or baseband/ channel cards and one or more radio equipment (RE) units (radio cards)

XILINX
ALL PROGRAMMABLE™

DELIVERING HIGH-SPEED CONNECTIVITY CAPABILITIES

Xilinx Connectivity Platforms Simplify and Accelerate High-Speed Serial Deployment

Fast growing data traffic and increasing usage of mobile networks for multi-media traffic is resulting in a continuous need of increased I/O bandwidth within wireless infrastructure equipment. Scalable and modular system designs addressing a variety of equipment form factors with growing system capacity are increasing reliance on chip-to-chip and board-to-board interconnect despite growing integration and greater compute capabilities in semiconductor silicon. While there is a move to use Ethernet protocol across all the system interconnects, proprietary and pseudo-proprietary protocols continue to flourish, thereby making it more challenging to manage and optimize interconnects within systems.

All programmable, scalable, and flexible FPGA and SoC platforms from Xilinx enable efficient and differentiated system implementation and faster deployment of customer end-product systems.

Key elements of Xilinx platforms include:

- Inherent capabilities to support a variety of connectivity protocols (standards based, pseudo-proprietary and proprietary)
- Rich mix of logic, high-speed transceivers, signal, and compute processing capabilities to support connectivity and adjacent functions such as compression, processing, and security
- Future-proofing system implementation to support evolving standards, increasing speeds & feeds, and the associated functions
- Industry's best-in-class tools, software, off the shelf IP and plug-and-play methodologies for faster time to market and lower cost of implementation
- Rich ecosystem providing FPGA / SoC equipped development boards, tools, IP, and services for faster and economical system implementation

Complete Tool Flow Reduces Time-to-Market

State-of-the-art connectivity tools are integrated in the Vivado® Design Suite to implement both established as well as new serial protocols. They also include a comprehensive IP portfolio supporting industry leading serial protocols. In addition, Xilinx's scalable board strategy, enabled by on-board FPGA Mezzanine Card (FMC) connectors, empowers customers to focus on innovation by reusing the design elements of the targeted reference designs.

Xilinx Connectivity Platforms (cont.)

- **SRIO** core endpoint solution, designed to RapidIO specification, for low-latency, fast-path communication
- **Ethernet MAC, PHY soft and hardened IP** portfolio supports 10/100 Mbps to 100G Ethernet along with system backplane (10G-KR)
- Support for Gen1-Gen3 PCI Express (PCIe) ports via integrated hard block and soft block solutions from Xilinx and partners
- The Intel **QPI** protocol provides a low-latency, high-bandwidth serial link for processor-to-processor communications. Developers can leverage the QPI IP core and the power of Xilinx 7 series All Programmable devices for next-generation data center servers and appliances.
- Xilinx's Software Defined Specification Environment for Networking (SDNet™), allows for the creation of 'Softly' Defined Networks, a technology that supports SDN functionality while also allowing for game changing differentiation through software programmable data plane hardware
- **1588v2 Timing Synchronization**, Alliance partner IP for frequency synchronization, phase alignment, and accurate Time of Day (ToD)

Xilinx All Programmable Advantage

Xilinx All Programmable FPGAs and SoCs and proven IP put wireless network designers a generation ahead. The industry-leading 28nm portfolio helps meet fast-changing market requirements with high-performance, low-power silicon and productivity-boosting design tools. Additionally, lower geometry nodes such as 28nm, 20nm and 16nm bring significant increase in performance and decrease power dissipation.

Silicon for High-Performance Connectivity Solutions

Xilinx offers a comprehensive range of All Programmable FPGA and SoC devices ideally suited for wireless base station applications. Xilinx 7 series technology offers a range of devices well suited to base station connectivity and switching applications. The key attributes required for the applications are:

- Availability of numerous serial transceivers that can be configured to support the wide range of physical interfaces typically adopted within wireless base stations
- High-performance programmable logic used to implement the interface protocol itself and any switching functionality associated with it
- Integrated block RAM used to support switching functionality, and delay compensation mechanisms that are often employed in high-capacity base stations
- High-performance SelectIO™ technology, supporting lower-speed interfaces potentially required by the application
- DSP capability supporting the signal-processing functionality that can be applied to the data to condition the signals prior to transfer between modules (e.g., bandwidth compression and beam forming)

7 Series FPGA Families Comparison

Each family is power, performance and price optimized to meet target application needs.

Maximum Capability	Artix-7 FPGAs	Kintex-7 FPGAs	Virtex-7 FPGAs
Logic Cells	215K	478K	1,955K
Block RMA	13 Mb	34 Mb	68 Mb
DSP Slices	740	1,920	3,600
Peak DSP Performance (symmetric FIR)	929 GMACS	2,845 GMACS	5,335 GMACS
Transceiver Count	16	32	96
Peak Transceiver Speed	6.6 Gb/s	12.5 Gb/s	28.05 Gb/s
Peak Serial Bandwidth (full duplex)	211 Gb/s	800 Gb/s	2,784 Fb/s
PCI Express Interface	Gen2x4	Gen2x8	Gen3x8*
Memory Interface	1,066 Mb/s	1,866 Mb/s	1,866 Mb/s
I/O Pins	500	500	1,200
I/O Voltage	1.2V, 1.35V, 1.5V 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V 1.8V, 2.5V, 3.3V*
Packaging Options	Low cost wire-bond	Low cost lidless flip-chip and high performance flip-chip	Highest performance flip-chip

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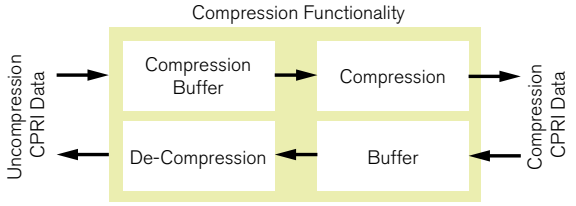
Example Baseband Switching & L1 Offload

- 12 x 12 CPRI processor plus radio I/Q sample compression
- Scalable solution: Kintex®-7 7K355T FPGA (88% full) and Kintex UltraScale™ KU060 device (60% full)
- Comparable power with room to grow within UltraScale device family



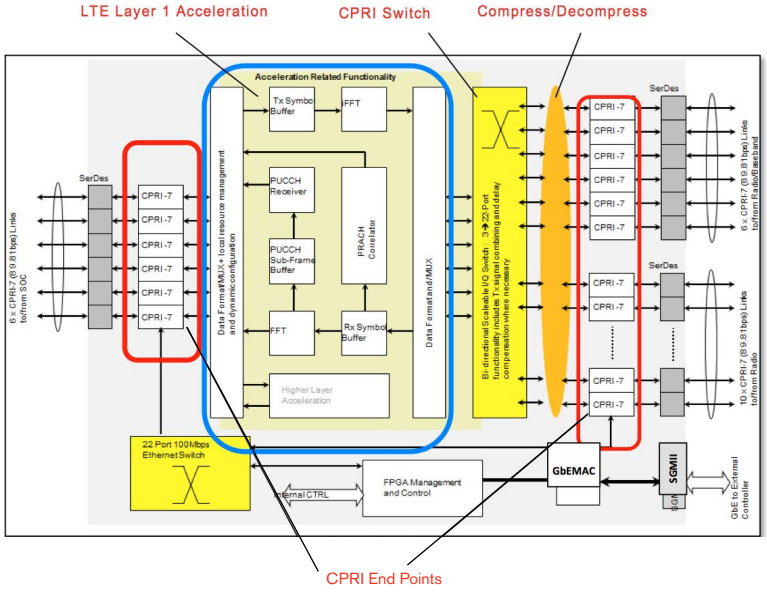


Table 8: **Device Utilization: 12x12 CPRI Processor plus Radio I/Q Sample Compression**

Device Type	FF	LUT	18K Block RAM	DSP	SERDES
XC7K355T	59%	88%	72%	70%	100%
XCKU060	39%	59%	48%	37%	75%

More information on this design example can be found in the Xilinx Switching White Paper at:
http://www.xilinx.com/support/documentation/white_papers/wp450-base-stn-connect.pdf

For information on Xilinx connectivity solutions, visit:
http://www.xilinx.com/applications/wireless-communications.html

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