7 Series
Product Selection Guide

SPARTAN ARTIX KINTEX VIRTEX

XILINX

Spartan-7 FPGAs

		I/O Optimization at the Lowest Cost and Highest Performance-per-Watt (1.0V, 0.95V)					
	Part Number	**XC7S6**	**XC7S15**	**XC7S25**	**XC7S50**	**XC7S75**	**XC7S100**
Logic Resources	Logic Cells	6,000	12,800	23,360	52,160	76,800	102,400
	Slices	938	2,000	3,650	8,150	12,000	16,000
	CLB Flip-Flops	7,500	16,000	29,200	65,200	96,000	128,000
Memory Resources	Max. Distributed RAM (Kb)	70	150	313	600	832	1,100
	Block RAM/FIFO w/ ECC (36 Kb each)	5	10	45	75	90	120
	Total Block RAM (Kb)	180	360	1,620	2,700	3,240	4,320
Clock Resources	Clock Mgmt Tiles (1 MMCM + 1 PLL)	2	2	3	5	8	8
I/O Resources	Max. Single-Ended I/O Pins	100	100	150	250	400	400
	Max. Differential I/O Pairs	48	48	72	120	192	192
Embedded Hard IP Resources	DSP Slices	10	20	80	120	140	160
	Analog Mixed Signal (AMS) / XADC	0	0	1	1	1	1
	Configuration AES / HMAC Blocks	0	0	1	1	1	1
Speed Grades	Commercial Temp (C)	-1,-2	-1,-2	-1,-2	-1,-2	-1,-2	-1,-2
	Industrial Temp (I)	-1,-2,-1L	-1,-2,-1L	-1,-2,-1L	-1,-2,-1L	-1,-2,-1L	-1,-2,-1L
	Expanded Temp (Q)	-1	-1	-1	-1	-1	-1

Package[1]	Body Area (mm)	Ball Pitch (mm)	**Available User I/O**: 3.3V SelectIO™ HR I/O					
CPGA196	8x8	0.5	100	100				
CSGA225	13x13	0.8	100	100	150			
CSGA324	15x15	0.8			150	210		
FTGB196	15x15	1.0	100	100	100	100		
FGGA484	23x23	1.0				250	338	338
FGGA676	27x27	1.0					400	400

Notes:
1. Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other Spartan-7 devices with the same sequence. The footprint compatible devices within this family are outlined.

Artix-7 FPGAs

		Transceiver Optimization at the Lowest Cost and Highest DSP Bandwidth (1.0V, 0.95V, 0.9V)							
	Part Number	XC7A12T	XC7A15T	XC7A25T	XC7A35T	XC7A50T	XC7A75T	XC7A100T	XC7A200T
Logic Resources	Logic Cells	12,800	16,640	23,360	33,280	52,160	75,520	101,440	215,360
	Slices	2,000	2,600	3,650	5,200	8,150	11,800	15,850	33,650
	CLB Flip-Flops	16,000	20,800	29,200	41,600	65,200	94,400	126,800	269,200
Memory Resources	Maximum Distributed RAM (Kb)	171	200	313	400	600	892	1,188	2,888
	Block RAM/FIFO w/ ECC (36 Kb each)	20	25	45	50	75	105	135	365
	Total Block RAM (Kb)	720	900	1,620	1,800	2,700	3,780	4,860	13,140
Clock Resources	CMTs (1 MMCM + 1 PLL)	3	5	3	5	5	6	6	10
I/O Resources	Maximum Single-Ended I/O	150	250	150	250	250	300	300	500
	Maximum Differential I/O Pairs	72	120	72	120	120	144	144	240
Embedded Hard IP Resources	DSP Slices	40	45	80	90	120	180	240	740
	PCIe® Gen2[1]	1	1	1	1	1	1	1	1
	Analog Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1	1
	GTP Transceivers (6.6 Gb/s Max Rate)[2]	2	4	4	4	4	8	8	16
Speed Grades	Commercial Temp (C)	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended Temp (E)	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3
	Industrial Temp (I)	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L

	Package[3, 4]	Dimensions (mm)	Ball Pitch (mm)	**Available User I/O**: 3.3V SelectIO™ HR I/O (GTP Transceivers)							
	CPG236	10 x 10	0.5		106 (2)		106 (2)	106 (2)			
	CPG238	10 x 10	0.5	112 (2)		112 (2)					
	CSG324	15 x 15	0.8		210 (0)		210 (0)	210 (0)	210 (0)	210 (0)	
	CSG325	15 x 15	0.8	150 (2)	150 (4)	150 (4)	150 (4)	150 (4)			
	FTG256	17 x 17	1.0		170 (0)		170 (0)	170 (0)	170 (0)	170 (0)	
	SBG484	19 x 19	0.8								285 (4)
Footprint Compatible	FGG484[5]	23 x 23	1.0		250 (4)		250 (4)	250 (4)	285 (4)	285 (4)	
	FBG484[5]	23 x 23	1.0								285 (4)
Footprint Compatible	FGG676[6]	27 x 27	1.0						300 (8)	300 (8)	
	FBG676[6]	27 x 27	1.0								400 (8)
	FFG1156	35 x 35	1.0								500 (16)

Notes:
1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates.
2. Represents the maximum number of transceivers available. Note that the majority of devices are available without transceivers. See the Package section of this table for details.
3. Leaded package option available for all packages. See DS180, *7 Series FPGAs Overview* for package details.
4. Device migration is available within the Artix-7 family for like packages but is not supported between other 7 series families.
5. Devices in FGG484 and FBG484 are footprint compatible.
6. Devices in FGG676 and FBG676 are footprint compatible.

Kintex-7 FPGAs

		Optimized for Best Price-Performance (1.0V, 0.95V, 0.9V)						
	Part Number	XC7K70T	XC7K160T	XC7K325T	XC7K355T	XC7K410T	XC7K420T	XC7K480T
Logic Resources	Slices	10,250	25,350	50,950	55,650	63,550	65,150	74,650
	Logic Cells	65,600	162,240	326,080	356,160	406,720	416,960	477,760
	CLB Flip-Flops	82,000	202,800	407,600	445,200	508,400	521,200	597,200
Memory Resources	Maximum Distributed RAM (Kb)	838	2,188	4,000	5,088	5,663	5,938	6,788
	Block RAM/FIFO w/ ECC (36 Kb each)	135	325	445	715	795	835	955
	Total Block RAM (Kb)	4,860	11,700	16,020	25,740	28,620	30,060	34,380
Clock Resources	CMTs (1 MMCM + 1 PLL)	6	8	10	6	10	8	8
I/O Resources	Maximum Single-Ended I/O	300	400	500	300	500	400	400
	Maximum Differential I/O Pairs	144	192	240	144	240	192	192
Integrated IP Resources	DSP48 Slices	240	600	840	1,440	1,540	1,680	1,920
	PCIe® Gen2[1]	1	1	1	1	1	1	1
	Analog Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1
	GTX Transceivers (12.5 Gb/s Max Rate)	8	8	16	24	16	32	32
Speed Grades	Commercial Temp (C)	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended Temp (E)	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3
	Industrial Temp (I)	-1, -2	-1, -2, -2L	-1, -2, -2L	-1, -2, -2L	-1, -2, -2L	-1, -2, -2L	-1, -2, -2L

	Package[2]	Dimensions (mm)	Ball Pitch (mm)	**Available User I/O**: 3.3V HR I/O, 1.8V HP I/Os (GTX)						
	FBG484[3]	23 x 23	1.0	185, 100 (4)	185, 100 (4)					
Footprint Compatible	FBG676[3]	27 x 27	1.0	200, 100 (8)	250, 150 (8)	250, 150 (8)		250, 150 (8)		
	FFG676	27 x 27	1.0		250, 150 (8)	250, 150 (8)		250, 150 (8)		
Footprint Compatible	FBG900[3]	31 x 31	1.0			350, 150 (16)		350, 150 (16)		
	FFG900	31 x 31	1.0			350, 150 (16)		350, 150 (16)		
	FFG901	31 x 31	1.0				300, 0 (24)		380, 0 (28)	380, 0 (28)
	FFG1156	35 x 35	1.0						400, 0 (32)	400, 0 (32)

Notes:
1. Hard block supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates. Gen3 supported with soft IP.
2. See DS180, *7 Series FPGAs Overview,* for package details.
3. GTX transceivers in FB packages support the following maximum data rates: 10.3Gb/s in FBG484; 6.6Gb/s in FBG676 and FBG900. See DS182, *Kintex-7 FPGAs Data Sheet: DC and AC Switching Characteristics*, for details.

Virtex-7 FPGAs

		Optimized for Highest System Performance and Capacity (1.0V)										
	Part Number	XC7V585T	XC7V2000T	XC7VX330T	XC7VX415T	XC7VX485T	XC7VX550T	XC7VX690T	XC7VX980T	XC7VX1140T	XC7VH580T	XC7VH870T
Logic Resources	Slices	91,050	305,400	51,000	64,400	75,900	86,600	108,300	153,000	178,000	90,700	136,900
	Logic Cells	582,720	1,954,560	326,400	412,160	485,760	554,240	693,120	979,200	1,139,200	580,480	876,160
	CLB Flip-Flops	728,400	2,443,200	408,000	515,200	607,200	692,800	866,400	1,224,000	1,424,000	725,600	1,095,200
Memory Resources	Maximum Distributed RAM (Kb)	6,938	21,550	4,388	6,525	8,175	8,725	10,888	13,838	17,700	8,850	13,275
	Block RAM/FIFO w/ ECC (36 Kb each)	795	1,292	750	880	1,030	1,180	1,470	1,500	1,880	940	1,410
	Total Block RAM (Kb)	28,620	46,512	27,000	31,680	37,080	42,480	52,920	54,000	67,680	33,840	50,760
Clocking	CMTs (1 MMCM + 1 PLL)	18	24	14	12	14	20	20	18	24	12	18
I/O Resources	Maximum Single-Ended I/O	850	1,200	700	600	700	600	1,000	900	1,100	600	300
	Maximum Differential I/O Pairs	408	576	336	288	336	288	480	432	528	288	144
Integrated IP Resources	DSP Slices	1,260	2,160	1,120	2,160	2,800	2,880	3,600	3,600	3,360	1,680	2,520
	PCIe® Gen2[1]	3	4	—	—	4	—	—	—	—	—	—
	PCIe Gen3	—	—	2	2	—	2	3	3	4	2	3
	Analog Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1	1	1	1	1
	GTX Transceivers (12.5 Gb/s Max Rate)[2]	36	36	—	—	56	—	—	—	—	—	—
	GTH Transceivers (13.1 Gb/s Max Rate)[3]	—	—	28	48	—	80	80	72	96	48	72
	GTZ Transceivers (28.05 Gb/s Max Rate)	—	—	—	—	—	—	—	—	—	8	16
Speed Grades	Commercial Temp (C)	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended Temp (E)[4]	-2L, -3	-2L, -2G	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L	-2L, -2G	-2L, -2G	-2L, -2G
	Industrial Temp (I)	-1, -2	-1	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1	-1	—	—

	Package[5]	Dimensions (mm)	Ball Pitch (mm)	**Available User I/O:** 3.3V HR I/O, 1.8V HP I/Os (GTX, GTH)							1.8V HP I/O (GTH, GTZ)	
	FFG1157[6]	35 x 35	1.0	0, 600 (20, 0)		0, 600 (20, 0)	0, 600 (0, 20)	0, 600 (20, 0)		0, 600 (0, 20)				
Footprint Compatible	FFG1761[6]	42.5 x 42.5	1.0	100, 750 (36, 0)		50, 650 (0, 28)		0, 700 (28, 0)		0, 850 (0, 36)				
	FHG1761	45 x 45	1.0		0, 850 (36, 0)									
	FLG1925	45 x 45	1.0		0, 1200 (16, 0)									
	FFG1158[6]	35 x 35	1.0				0, 350 (0, 48)	0, 350 (48, 0)	0, 350 (0, 48)	0, 350 (0, 48)				
Footprint Compatible	FFG1926	45 x 45	1.0							0, 720 (0, 64)	0, 720 (0, 64)			
	FLG1926	45 x 45	1.0									0, 720 (0, 64)		
	FFG1927[6]	45 x 45	1.0				0, 600 (0, 48)	0, 600 (56, 0)	0, 600 (0, 80)	0, 600 (0, 80)				
Footprint Compatible	FFG1928	45 x 45	1.0								0, 480 (0, 72)			
	FLG1928	45 x 45	1.0									0, 480 (0, 96)		
Footprint Compatible	FFG1930	45 x 45	1.0					0, 700 (24, 0)		0, 1000 (0, 24)	0, 900 (0, 24)			
	FLG1930	45 x 45	1.0									0, 1100 (0, 24)		
	FLG1155	35 x 35	1.0										400 (24, 8)	
	FLG1931	45 x 45	1.0										600 (48, 8)	
	FLG1932	45 x 45	1.0											300 (72, 16)

Notes:
1. Hard block supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates. Gen3 supported with soft IP.
2. 12.5 Gb/s support in "-3E", "-2GE" speed/temperature grade; 10.3125 Gb/s support in "2C", "-2LE", and "-2I" speed grade.
3. 13.1 Gb/s support in "-3E". "-2GE" speed grade; 11.3 Gb/s support in "2C" , "-2LE" and "-2I" speed/temperature grades.
4. -2G only applies to Stacked Silicon Interconnect devices and supports 12.5G GTX, 13.1G GTH, 28.05G GTZ with -2 fabric.
5. Leaded package options ("FFxxxx"/"FLxxxx"/"FHxxxx") available for all packages. "HCxxxx" is not offered in a leaded option.
6. See DS180, *7 Series FPGAs Overview* for package details.

Device Ordering Information

SPARTAN-7

XC	7	S	###	-1	FG	G	A	484	C
Commercial Xilinx	Generation	Family	Logic Cells In 1K units	Speed Grade -1 = Slowest -L1 = Low Power -2 = Mid	Package Type CP: Wire-bond (.5 mm) CS: Wire-bond (.8 mm) FG: Wire-bond (1 mm) FT: Wire-bond (1 mm)	G: RoHS 6/6	Package Designator	Package Pin Count	Temperature Grade (C, I, Q)

ARTIX-7

XC	7	A	###	-1	FB	G	484	C
Xilinx Commercial	Generation	Family	Logic Cells in 1K Units	Speed Grade -1 = Slowest -L1 = Low Power -L2 = Low Power -2 = Mid -3 = Highest	Package Type CP: Wire-bond (.5 mm) CS: Wire-bond (.8 mm) FB: Bare-Die Flip-Chip (1 mm) FF: Flip-Chip (1 mm) FG: Wire-bond (1 mm) FT: Wire-bond (1 mm) SB: Bare-Die Flip-Chip (.8 mm)	V: RoHS 6/6 G: RoHS 6/6 w/Exemption 15	Nominal Package Pin Count	Temperature Grade (C, E, I)

KINTEX-7

XC	7	K	###	-1	FF	G	900	C
Xilinx Commercial	Generation	Family	Logic Cells in 1K Units	Speed Grade -1 = Slowest -L2 = Low Power -2 = Mid -3 = Highest	Package Type FB: Bare-Die Flip-Chip (1 mm) FF: Flip-Chip (1 mm)	V: RoHS 6/6 G: RoHS 6/6 w/Exemption 15	Nominal Package Pin Count	Temperature Grade (C, E, I)

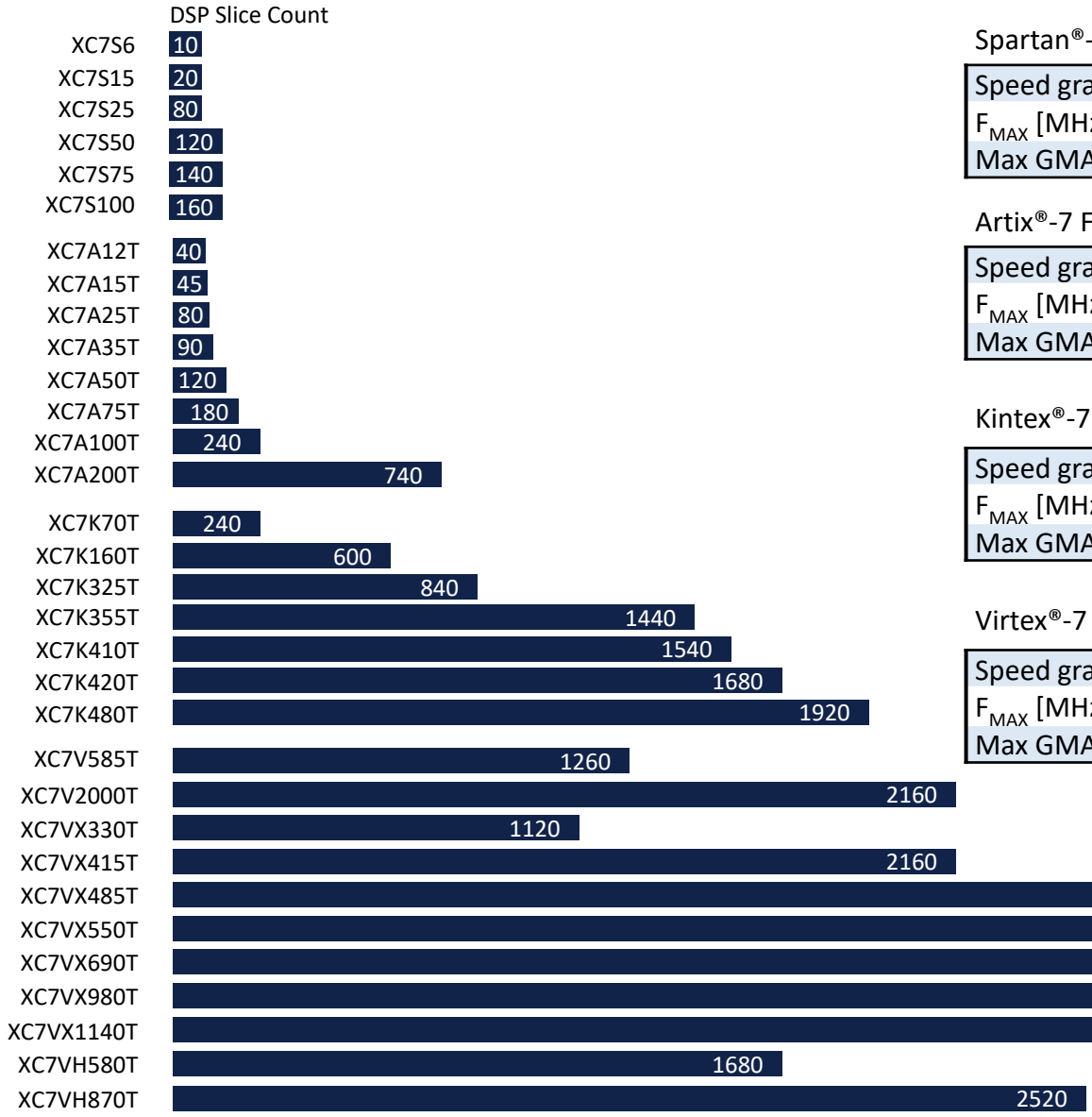
VIRTEX-7

XC	7	V	###	-1	FF	G	1156	C
Xilinx Commercial	Generation	Family	Logic Cells in 1K Units	Speed Grade -1 = Slowest -2 = Mid -L2 = Low Power -3 = Highest	Package Type FF: Flip-Chip (1 mm) FH: Flip-Chip (1 mm) FL: Flip-Chip (1 mm) HC: Ceramic Flip-Chip (1 mm)	V: RoHS 6/6 G: RoHS 6/6 w/Exemption 15	Nominal Package Pin Count	Temperature Grade (C, E, I)

Notes:
-L1 is the ordering code for the lower power, -1L speed grade.
-L2 is the ordering code for the lower power, -2L speed grade.

C = Commercial (Tj = 0°C to +85°C) E = Extended (Tj = 0°C to +100°C) I = Industrial (Tj = –40°C to +100°C) Q = Expanded (Tj = –40°C to +125°C)

Digital Signal Processing Metrics



Spartan®-7 FPGAs

Speed grade	-1	-2
F_{MAX} [MHz]	464	550
Max GMAC/s	148	176

Artix®-7 FPGAs

Speed grade	-1	-2	-3
F_{MAX} [MHz]	464	550	628
Max GMAC/s	686	814	929

Kintex®-7 FPGAs

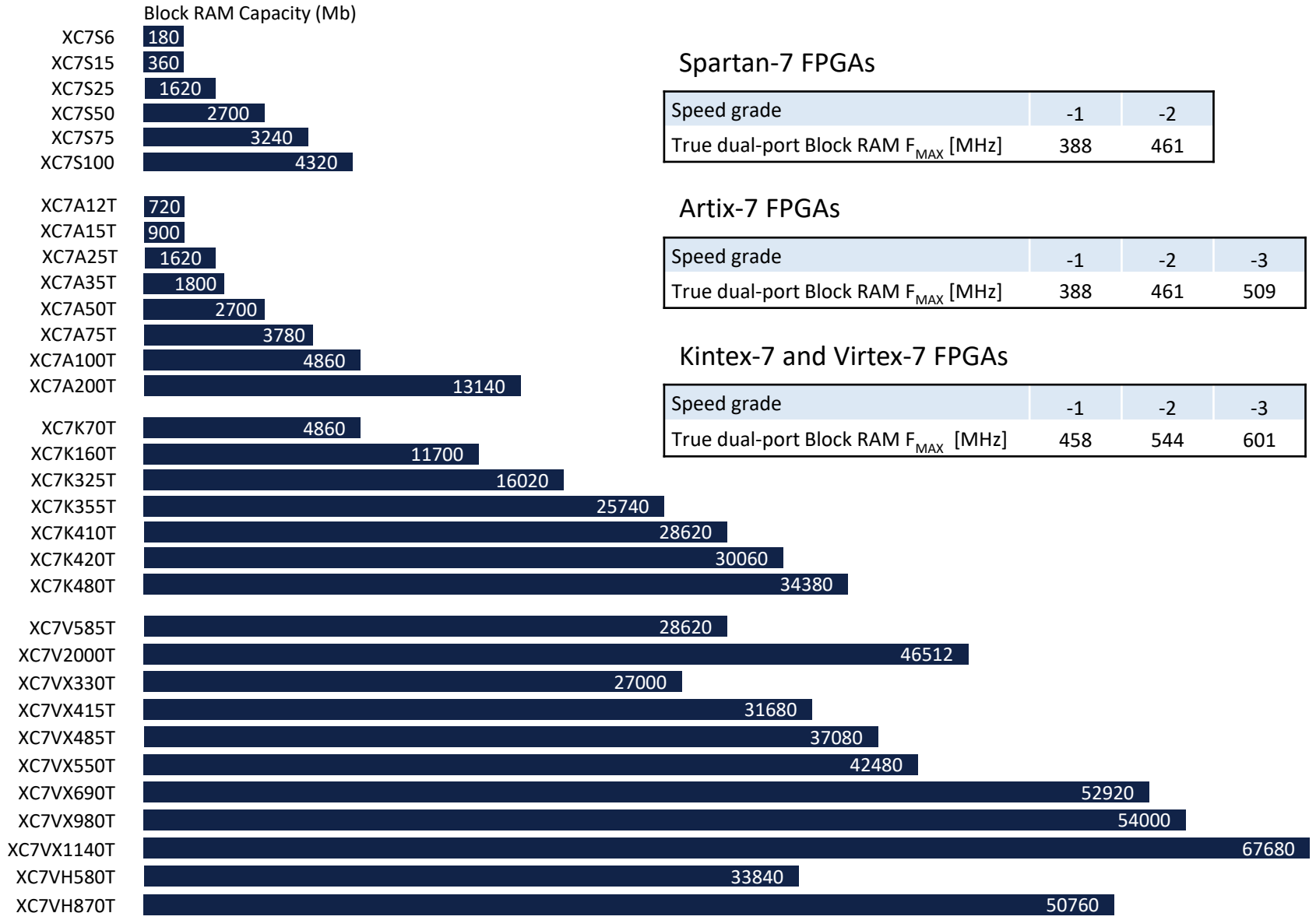
Speed grade	-1	-2	-3
F_{MAX} [MHz]	464	550	741
Max GMAC/s	1,781	2,112	2,845

Virtex®-7 FPGAs

Speed grade	-1	-2	-3
F_{MAX} [MHz]	547	650	741
Max GMAC/s	2,756	3,276	3,734

For more information, refer to: UG479, *7 Series FPGAs DSP48E1 Slice User Guide*

Block RAM Metrics



Spartan-7 FPGAs

Speed grade	-1	-2
True dual-port Block RAM F_{MAX} [MHz]	388	461

Artix-7 FPGAs

Speed grade	-1	-2	-3
True dual-port Block RAM F_{MAX} [MHz]	388	461	509

Kintex-7 and Virtex-7 FPGAs

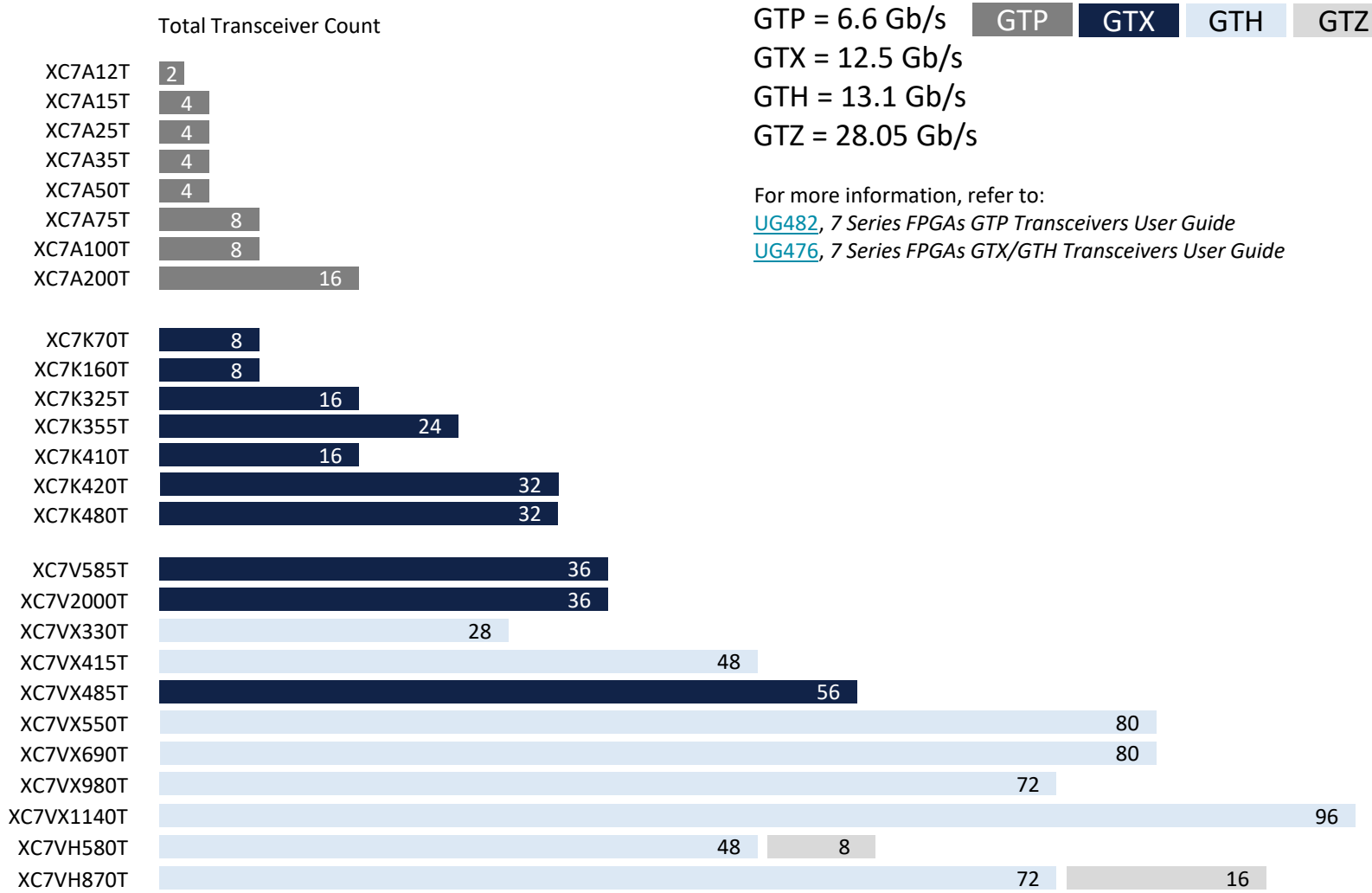
Speed grade	-1	-2	-3
True dual-port Block RAM F_{MAX} [MHz]	458	544	601

For more information, refer to: UG473, *7 Series FPGAs Memory Resources User Guide*

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

High-Speed Serial Transceivers

7 series devices provide a broad portfolio of transceivers for applications ranging from low-cost consumer products to high-end networking systems.



GTP = 6.6 Gb/s
GTX = 12.5 Gb/s
GTH = 13.1 Gb/s
GTZ = 28.05 Gb/s

GTP GTX GTH GTZ

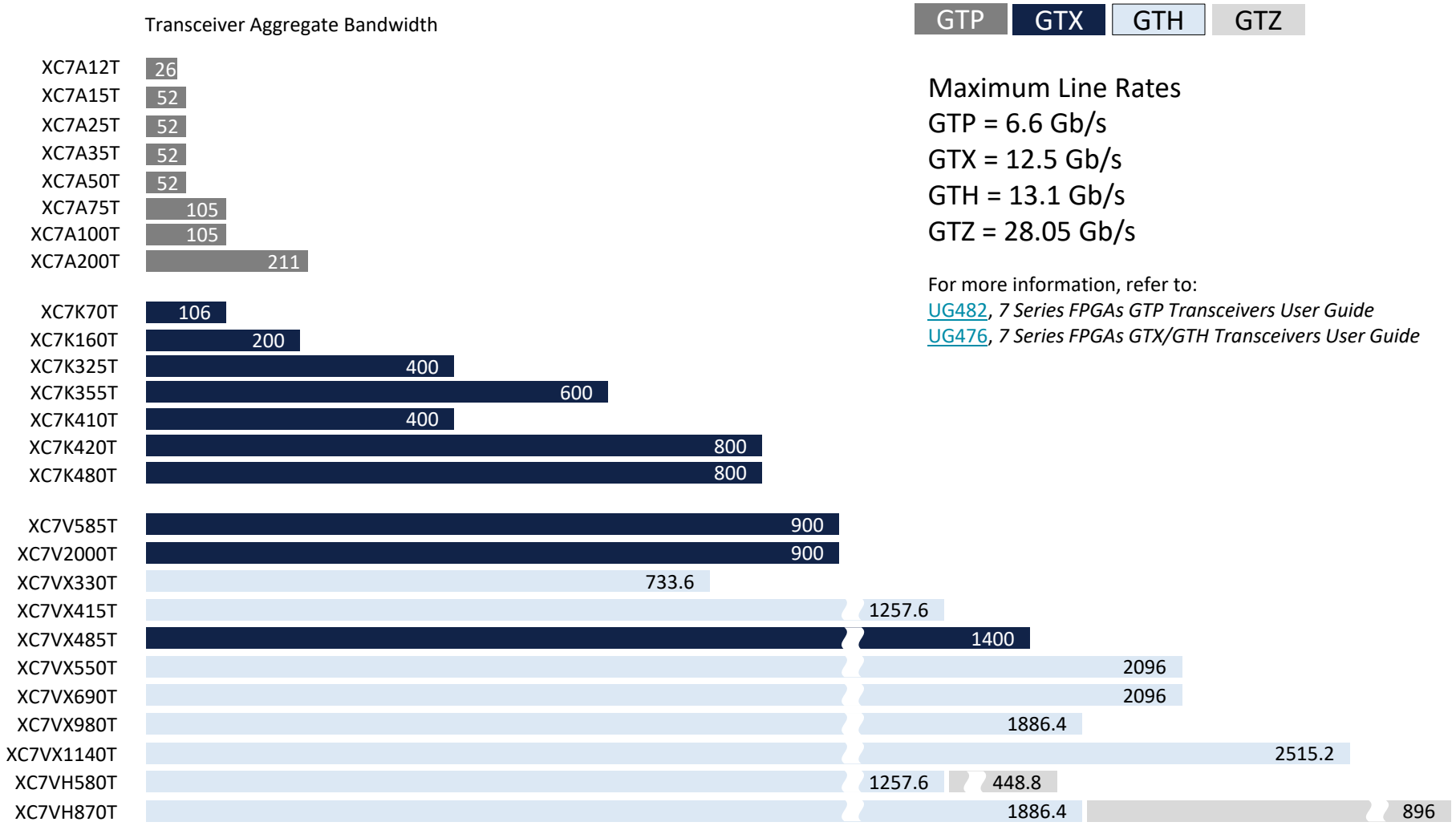
For more information, refer to:
UG482, *7 Series FPGAs GTP Transceivers User Guide*
UG476, *7 Series FPGAs GTX/GTH Transceivers User Guide*

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

XILINX

Transceiver Aggregate Bandwidth

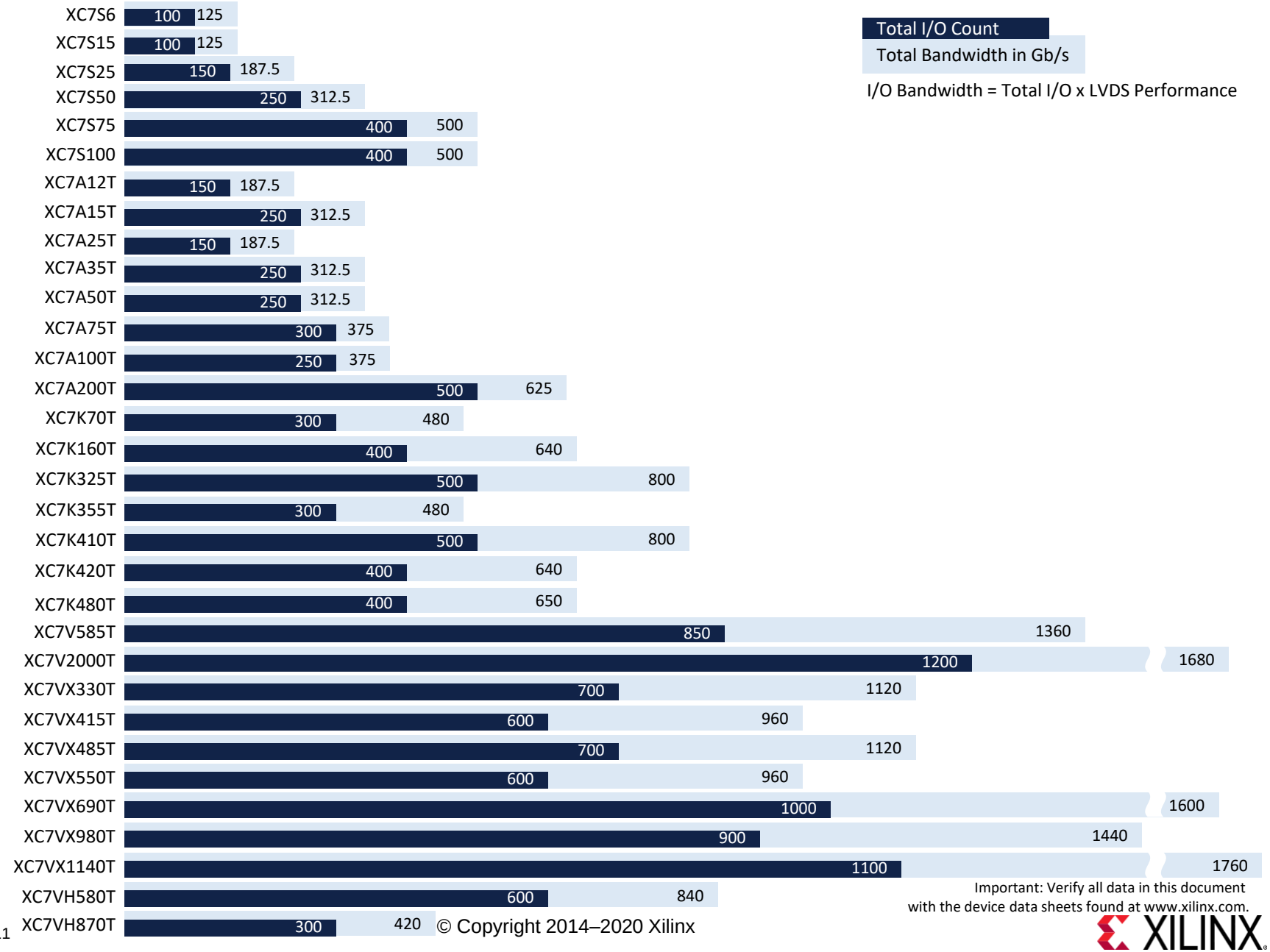
7 series devices provide a broad portfolio of transceivers for applications ranging from low-cost consumer products to high-end networking systems.



Maximum Line Rates
GTP = 6.6 Gb/s
GTX = 12.5 Gb/s
GTH = 13.1 Gb/s
GTZ = 28.05 Gb/s

For more information, refer to:
UG482, *7 Series FPGAs GTP Transceivers User Guide*
UG476, *7 Series FPGAs GTX/GTH Transceivers User Guide*

I/O Count and Bandwidth



Important: Verify all data in this document with the device data sheets found at www.xilinx.com.

References

DS180, *7 Series FPGAs Overview*

DS181, *Artix-7 FPGAs Data Sheet: DC and AC Switching Characteristics*

DS182, *Kintex-7 FPGAs Data Sheet: DC and AC Switching Characteristics*

DS183, *Virtex-7 T and XT FPGAs Data Sheet: DC and AC Switching Characteristics*

UG470, *7 Series FPGAs Configuration User Guide*

UG471, *7 Series FPGAs SelectIO Resources User Guide*

UG472, *7 Series FPGAs Clocking Resources User Guide*

UG473, *7 Series FPGAs Memory Resources User Guide*

UG474, *7 Series FPGAs Configurable Logic Block User Guide*

UG475, *7 Series FPGAs Packaging and Pinout User Guide*

UG476, *7 Series FPGAs GTX/GTH Transceivers User Guide*

UG479, *7 Series FPGAs DSP48E1 Slice User Guide*

UG480, *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS ADC User Guide*

UG482, *7 Series FPGAs GTP Transceivers User Guide*

UG483, *7 Series FPGAs PCB Design Guide*